As originally published in the IPC APEX EXPO Conference Proceedings.

Evaluation and Characterization of Molded flip-chip BGA Package for 28nm FPGA Applications

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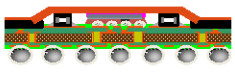
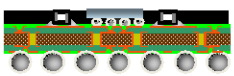
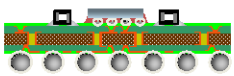
Abstract
As the FPGA device technology migrates to 28nm technology node and high performance applications, selecting the right package to meet the customer usability requirements and to achieve product reliability goals becomes important. The paper describes the process used in selecting and qualifying the molded flip-chip BGA for cost effective, high performance 28nm FPGA devices. A collaborative approach in partnership with the assembly manufacturer was employed to develop customer collateral that includes handling; reflow/rework and heat sink attach guidelines for the molded flip-chip BGA package. A detailed thermal modeling of the package was performed to characterize the thermal performance of the package. In addition, compressive loading characterization, component level and board level reliability tests were carried out to validate the long term reliability performance of the package in customer use conditions. The results of this study demonstrate that the molded flip-chip BGA package is a cost effective and high reliability solution for 28nm FPGA devices.

Introduction
Altera has introduced Arria®-V FPGA product family at 28nm technology node to deliver optimized balance of performance, cost and low power for mid-range applications. In order to meet the device performance and cost goals, selection of packaging technology has become important. The package selected must meet the customer usability requirements and achieve product reliability goals. This paper describes the process used in selecting and qualifying the molded flip-chip BGA package for cost effective, high performance 28nm FPGA devices. To match the low-power, high performance and low cost requirements of the 28nm Arria®-V FPGA's, a new package platform offered by Amkor Technology, Molded Flip-Chip BGA(Amkor acronym: FCmBGA, Altera acronym: TCFCBGA, Thermal Composite Flip-Chip BGA), was selected. Having an exposed die configuration, FCmBGA inherently offers a low profile form factor. Further the exposed die allows customers flexibility with respect to thermal dissipation solutions. Finally, the replacement of capillary underfill, CUF, with molded underfill, MUF, allows coverage of the 28nm FPGA family with a single package configuration.

In subsequent sections we will describe the methodology for package selection as well as various tests run to provide application guidelines for Customers using this package platform. Results for handling during shipping, SMT attach and rework results will be discussed. Heat sink attach/ rework and thermal modeling will also be reviewed. Compressive loading and well as component and board level reliability results will be summarized.

Package Selection
In order to make the decision about selecting the packaging platform for the 28nm FPGA application, a comprehensive matrix of package requirements was designed and the corresponding data was collected, Table 1.

Table 1 - Package Selection Matrix

Feature	Single Piece Lid	FCmBGA	Bare Die
			
Package Profile	GOOD	BETTER	BETTER
Room for Passives	GOOD	BEST	GOOD
Coplanarity	BEST	BETTER	GOOD
Bump Reliability	GOOD	BEST	GOOD
BGA Reliability	BEST	BEST	GOOD
Heat Sink Attach Surface	BEST	BETTER	GOOD
Thermal Performance with Heat Sink	BETTER	BEST	GOOD
Cost	GOOD	BETTER	BEST

Package profile is an important consideration, especially as more applications require thin form factors. Both FCmBGA and Bare Die packages offer thinner package profile form factor than a single piece lid package, however, as the package gets thinner Bare Die packages are limited on body size and die size. This is due to the Coplanarity requirement. FCmBGA adds additional support to the die by coupling the MUF to the substrate. This in turn helps control package warpage/Coplanarity and allows for thinner larger packages with larger die. Another gain from the molding compound around die is the package robustness compared to the bare die format. This advantage offers many benefits during component handling such as shipping, electrical test, board mounting, rework and heatsink attach. FCmBGA package is advantageous from the point of view of 28nm FPGA family coverage. Typically a range of die and body sizes are deployed with each new FPGA family. With FCmBGA package, one package type can cover the entire family. Another benefit of FCmBGA over single piece lid and Bare Die is keep out zones, KOZ, requirements. Both single piece lid and Bare Die packages use Capillary Underfill, CUF. CUF requires 2 to 3 mm KOZ between the die and on board passives. This is to prevent partial filling of the on board passive solder joints by the CUF, which can lead to solder joint fracture during temperature cycle condition B testing [1]. FCmBGA uses molded Underfill, MUF to encapsulate the on board passives and around the die. Thus, the KOZ for FCmBGA package is less restrictive, 0.6mm.

The FCmBGA mold cap is designed to be below the attached die height. This allows the thinnest bond line thickness, BLT, and thus the best thermal performance. Work was done with several commercially available heat sinks and TIM II materials to illustrate how heat sinks can be attached to FCmBGA. Rework of the heat sink was also performed to demonstrate the ruggedness of the molded package. Thermal performance was evaluated through FEM modeling.

Like with any new package platform, demonstrating that the package meets the customer reliability requirements is important. The industry standard component level and board level reliability tests were run to compare the FCmBGA performance to single piece lid and Bare Die control packages. The package performed well in direct head to head comparisons.

Collaboration to Develop Customer Collateral

With selection of new package type for the 28nm FPGA product family, it was essential to develop customer collateral to ensure that the package meets the customer usability requirements. The objective of customer collateral is to provide the guidance to the customers for component handling, board level assembly and rework and develop the heatsink attach and rework process. We collaborated to develop the customer collateral by running joint evaluations on the test vehicles assembled in the FCmBGA package. Additionally, accelerated component level and board level reliability testing was run to verify the package integrity in the customer use conditions.

Selection of Test Vehicles

In order to evaluate and characterize the FCmBGA package ahead of 28nm FPGA product release, test vehicles were required to be selected for evaluations. The criterion for the test vehicle selection was that the die size and package size of the test vehicle should be closer to the largest die/package size combination for the 28nm FPGA family.

After reviewing the number of test vehicles available for testing, a 90nm FPGA device was selected for assembly process, handling guidelines, heatsink attach, mechanical characterization and component level reliability tests. A full stack 40nm daisy chain test vehicle was selected for board reliability testing. The details of the test vehicles are outlined table 2.

Table 2. Characterization Test Vehicle Details

	Test Vehicle - 1	Test Vehicle - 2
Device	Full Stack 40nm Daisy Chain	90nm Altera FPGA
Die Size	22 x 19 mm^2	19.24 x 22.17 mm^2
Bump Pitch	170mm	225mm
Bump Alloy	Eutectic (Sn/Pb)	Eutectic (Sn/Pb)
Package	F1681 FCmBGA	F1508 FCmBGA
Package Size	42.5x42.5 mm^2	40x40 mm^2
Assembly	Amkor	Amkor
Rel Test	Altera	Altera

To carry out the board level characterization experiments, a development board representing typical customer assembly board was selected. The PCB was designed per IPC-9701 guidelines[(2)] with 330mmx114mm size, 2.3mm thickness, 8 layer stack up board as shown in figure 1.

Figure 1. Assembly and Characterization Development Board

FCmBGA Handling Characterization (Tray Drop Test)

FCmBGA packages do not require a tray design different than those already available for standard FCBGA bare die (lidless) packages. In fact, the same tray can be often used for an equivalent bare die and FCmBGA package since both packages are lidless and have roughly the same height due to identical package stack ups (though coplanarity is likely lower with a FCmBGA style package). The FCmBGA mold cap is below the die so it will not interfere with a standard JEDEC style tray design. In the below work, FCmBGA packages were tested for integrity after dropping them in bundled trays. After testing, both package and trays were inspected for damage. Three packages with three different body sizes were tested: 31, 35 and 40mm packages were tested. All packages shared the same die size.

Test Procedure

Five trays were fully populated with packages and a sixth tray was added as a cover tray. All trays were banded together three times with a standard polypropylene band, bagged in an antistatic band, and then boxed. The box was then dropped from a height of 120cm. The packages and trays were inspected before and after tray drop. The results of the tray drop tests are summarized in table 3. The visual inspection of the devices after tray drop testing showed no defects, as shown in figures 2a and 2b.

Tray Drop Test Results

Table 3. Tray Drop Test Summary and Results

Package Type	Body Size (mm)	Die Size (mm)	Package Damage	Tray Damage
FCmBGA	31	19 x 14	0/118	0/6
	35		0/120	0/6
	40		0/105	0/6

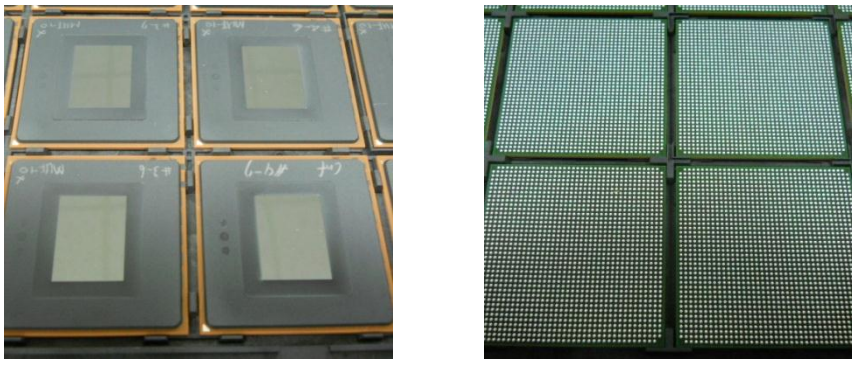


Figure 2a and 2b – Top (left) and bottom side (right) of package after the tray drop test

SMT Reflow Characterization

The SMT reflow characterization experiments conducted at a preferred SMT sub-contractor showed that the FCmBGA package follows the same SMT practices of single piece lid and Bare Die packages. The same PCB designs are used. Typical surface finishes e.g. organic solder preservative, OSP with eutectic or lead free solder paste may be used.

Like with other flip chip packages a proper thermal profile is required to achieve good BGA balls collapse. Calibrated thermocouples should be used to instrument a reflow profile board and use it to develop an optimized thermal profile of the package on board.

Figure 3 shows the typical reflow profile used for assembling the FCmBGA on the PCB. The comparison of the reflow profiles for FCmBGA and the lidded Flip-Chip BGA (Single Piece Lid SPL) package shows that the reflow profiles are quite similar and fall within the range of reflow parameters defined in table 5-2 of JEDEC standard J-STD-020[3].

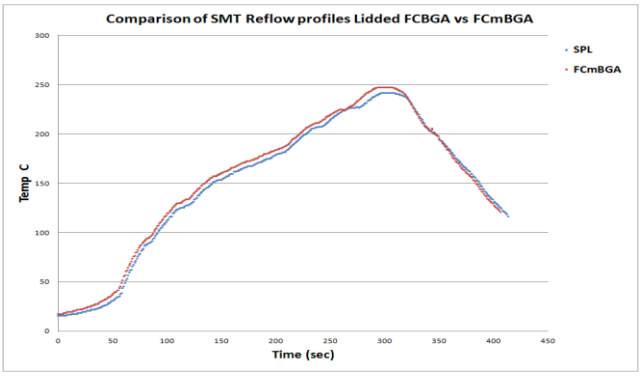
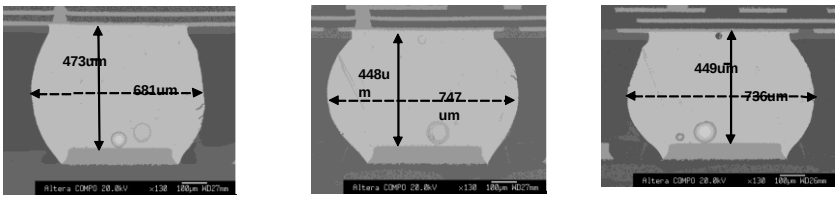


Figure 3. Reflow profiles of FCmBGA vs lidded-FCBGA

After the assembly process was completed, the mounted devices were inspected to verify solder joint integrity. Visual inspection of the solder joints along the package edge and corners showed well formed solder joints. One device was cross-sectioned along the package edge to determine the shape and the size of the solder joints formed during SMT. Figure 4 shows that the solder joints have consistent solder joint shape across the package edge and the center.



Package Corner Left | Package Center | Package Corner Right

Figure 4. FCmBGA solder joints after SMT reflow.

SMT Rework Characterization

Localized SMT rework of BGA components is typically performed by customers to replace defective parts or upgrade the device to latest version. Localized attach of FCmBGA packages is possible with industry standard BGA Rework machines. Like with SMT attach, a profile board with properly attached calibrated thermocouples is required to develop an optimized reflow profile.

The experiments conducted to develop the localized attach reflow profile showed that the reflow parameters were well with the parameters as defined in JEDEC standard J-STD-020. However, when compared with the lidded FCBGA, one significant difference was found. Since the FCmBGA package has exposed die surrounded by the mold cap, the heat transfer from the top heater through the package to the solder joints is uneven. Consequently, the ball collapse along the periphery of the package is difficult if only the top heater is used. However, the uneven heat transfer from the top of the package can be compensated by increasing the heat from the bottom heater of the rework machine. With optimized top and bottom heater settings, an optimized reflow profile for localized attach of FCmBGA package was developed in this study.

The devices attached with localized reflow process were visually inspected along the package edge and corners. The visual inspection shows well formed solder joints.

One device was cross-sectioned along the package edge to determine the shape and the size of the solder joints formed during localized reflow. Figure 5 shows that the solder joints have consistent solder joint shape across the package edge and the package center.

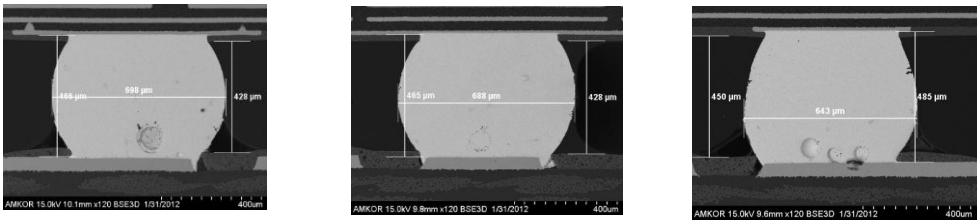


Figure 5. FCmBGA solder joints after localized attach.

Heat Sink Attach and Rework

The process of attaching a heat sink to the FCmBGA package and subsequently removing the heat sink (to rework the board) is identical to that of a standard bare die or lidded FCBGA package. In this characterization work, heat sinks were attached using two different thermal interface materials (TIMs): Double sided thermal tape and thermally conductive epoxy. Six packages were evaluated for each thermal interface material. After attach and removal steps were completed, visual and SAT inspection were used to inspect for damage to the die or delamination at the passivation or EMC layers. Results show that the heat sink can be attached and removed without damage to the package or die. In the FCmBGA package, the mold compound around the die offers additional surface area for increased adhesion and thermal conduction and no die chipping was observed in our evaluation.

Heat Sink Removal with Double Sided Thermal Tape

This particular adhesive tape is a popular double-sided thermally conductive adhesive tape. It is rates as reworkable by the supplier. Six heat sinks were attached and removed using the supplier's recommended method. All units were inspected with SAT imaging before and after testing. No failures or changes in package quality were detected. Figure 6 shows the process flow and the images of each process step during heat sink rework.

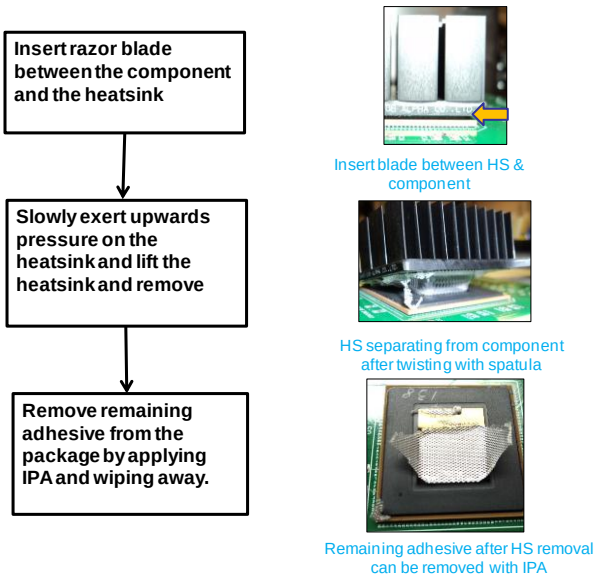


Figure 6. Thermal tape rework process flow

Heat Sink Removal with Thermally Conductive Epoxy

This TIM is a thermally conductive epoxy material. The heat sink attach and the removal process was found to be identical to the lidded FCBGA package. Figure 7 shows the process flow and the images of each process step during heatsink rework.

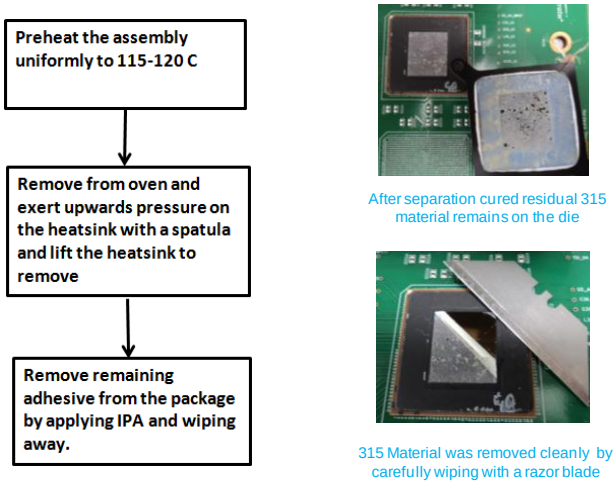
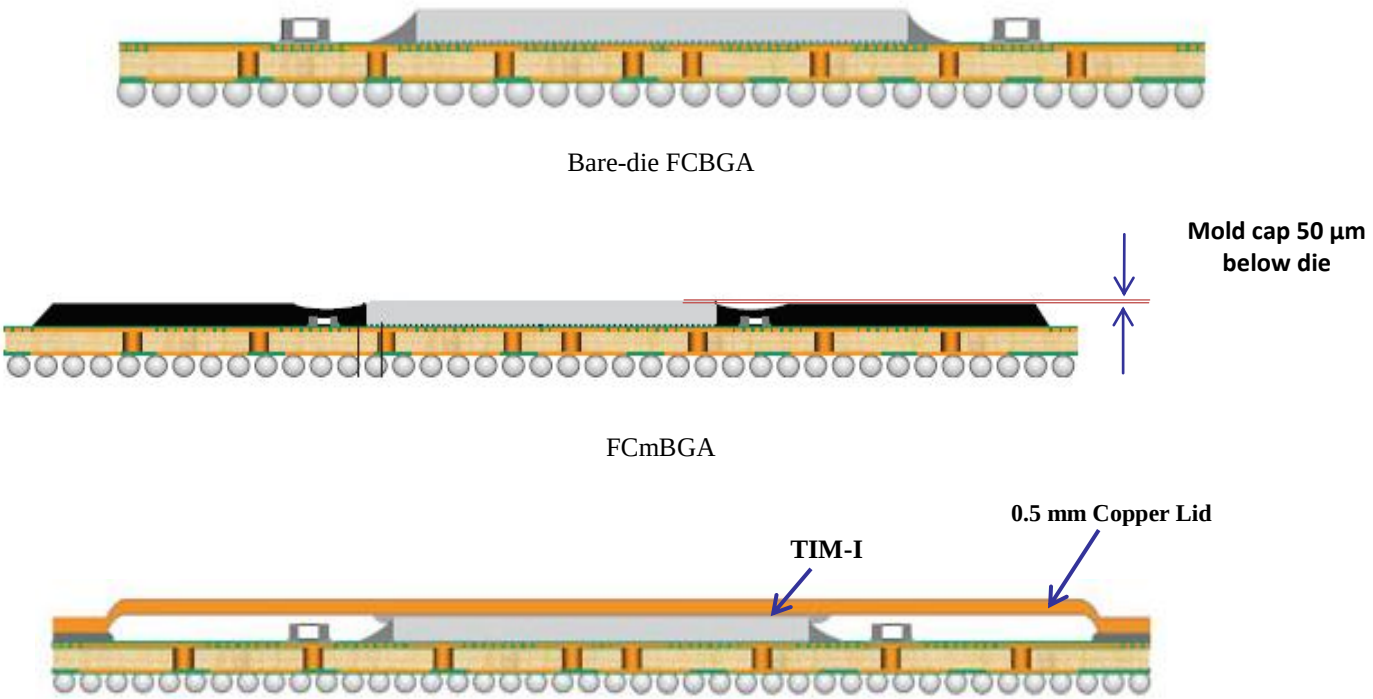


Figure 7. Thermal epoxy rework process flow

Thermal Modeling

Detailed thermal modeling of various flip-chip packaging options was performed using commercially available CFD tool. The analysis was performed to compare the thermal performance of the FCmBGA with bare die FCBGA and single-piece-lid FCBGA (FCLBGA). The package configurations are depicted in the Figure 8 below.



Bare-die FCBGA

FCmBGA

Lidded FCBGA

Figure 8. Flip-chip package configurations considered in this work

The package construction details used for the simulations are outlined in the below Table 4. The packages were mounted onto a JEDEC 1S2P board and the simulation boundary was assumed to be a JEDEC still air chamber. Also, the package top surface was interfaced with a thin sheet of Aluminum (100 x 100 x 1 mm^3) using a TIM-II material (0.5C-in^2/W thermal impedance). The simulation results are shown below in Table 5.

Table 4. Package construction details

Package Construction Details	
Body (mm)	40
Die Size (mm)	16 x 20 x 0.786
Substrate Construction	2-2-2
Cu Lid thickness for FCLBGA (mm)	0.5

Table 5. Thermal simulation results summary

Package	Mold Compound (W/mK)	Power (W)	TIM-II Material (Thermal Impedance)	Theta-JA (C/W)
Bare Die FCBGA	N/A	14	0.5 C*in^2/W	5.83
FCmBGA	0.7			5.70
	1.5			5.69
	3			5.66
FCLBGA	N/A			5.24

As seen from the above results, under the conditions assumed in this work, FCmBGA package thermal performance is slightly better than the bare-die package, but still not comparable to the FCLBGA package performance. The θ_{ja} of the FCmBGA package was about ~9% higher than that of FCLBGA. Also, thermally enhanced mold compounds did not have a significant impact on improving (lowering θ_{ja}) the FCmBGA package thermal performance. It is important to note that the simulation trends presented here are representative of the particular system thermal solution (TIM-II + Aluminum sheet) chosen in this work. The choice of TIM-II and the external heatsink significantly impact the overall package/system thermal performance. Detailed thermal measurements comparing the thermal performance of FCmBGA with FCLBGA are presented in the paper by Galloway et al.[4].

Compressive Loading Characterization

To verify package integrity, three FCmBGA units were surface mounted then tested in compression at 1480N (106 PSI) for a duration of 15 minutes at room temperature using an Instron mechanical tester. The test vehicles were 40mm packages with a 22 x 19mm die, surface mounted to a 2.3mm thick standard JEDEC style board. The acceptance criteria were the following: No damage to the die (either chip out or cracking), No damage to the mold compound (specifically cracking) and no BGA deformation leading to BGA shorting.

Compression Load Test Setup

To assure equal loading across the package, a thick steel fixture was placed between the crosshead and package topside. Double sided thermal tape was applied between the package and steel fixture to further promote equal distribution of compressive stress, as shown in figure 9.

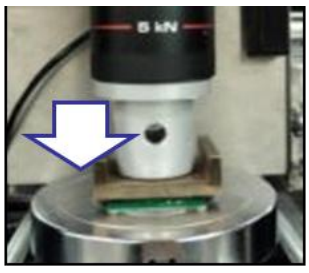


Figure 9 – Photo of the compression test setup

Compression Test Results

Table 6. Compression Test Summary and Results

Inspection Location	Inspection Method	Force	Dwell Time	Sample Size	Result
Die Surface	SAT and Visual	1500 N	15 minutes	3	Pass
Die Active Layers	SAT				
EMC to Passivation	SAT				
EMC to Package	SAT				
BGA's	X-RAY/Visual				

No damage to the test vehicles were detected using the inspection methods listed in table 6. Visual inspection was carried out either with a microscope or an ERSA scope for BGA inspection. The SAT inspection areas include: The die surface, die active layers, the EMC adhesion to the passivation, the EMC adhesion to the package under the die as well as the die surface.

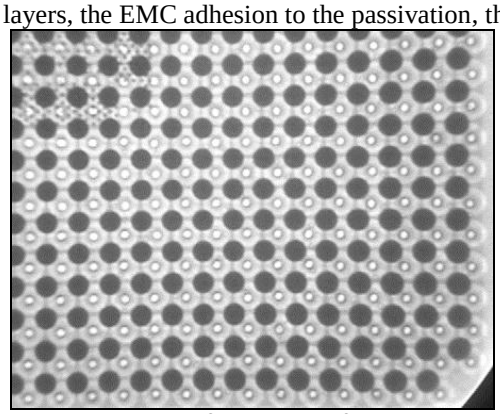


Figure 10. XRAY of the BGAs after compressive loading shows no signs of shorting

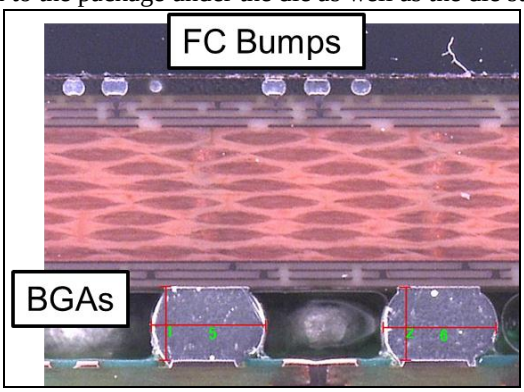


Figure 11. Cross section of a sample confirms there is no shorting after compressive loading.

Additionally, all BGAs of all samples were inspected X-ray imaging(Figure 10). No anomalies were detected between the BGA solder balls. No measureable differences were observed as a result of the compressive loading. For further confirmation, a unit was cross sectioned to the bump and BGA plane (Figure 11). BGA solder balls were confirmed not to have been shorted together or significantly deformed.

Even though the compression test results show that the package can withstand one time application of compressive force up to 1480N, it is recommended that the customers follow heatsink manufacturer's recommendations for application of compressive force for heatsink attach.

Component and Board Level Reliability

The 28nm FCmBGA devices were subjected to component level and board level reliability test to ensure that package meets our package level and second level reliability requirements. We has defined the reliability test plan[5] in conformance with the industry standards defined by JEDEC and IPC organizations. A 28nm FPGA device was used to perform the component level reliability tests and a full stack daisy chain test vehicle was used for the board level reliability tests.

The FCmBGA packages were subjected to preconditioning at MSL3 level and a reflow cycle at 260 ^{o}C to simulate the component assembly conditions. The devices were electrically tested at intermediate readout points to detect early failures. The parts subjected to board level temperature cycle were continuously monitored to check resistance changes in the daisy chains during temperature cycling. Table 7 summarizes the results of the component level and the board level reliability tests.

Table 7. 28nm FPGA Reliability Test Results

Device	Package Size (mmxmm)	Die Size (mmxmm)	Pin count	Solder Ball	MSL	Reflow Temp C	Number of lots	Sample Size/lot	Reliability Test Results			
Altera 28nm FPGA Device	35x35	18.8x14	1152	Pb-free	3	260			Temp Cycle Condition B -55/125 °C(Cycles)			
									200	500	700	1000
							3	30	0/90	0/90	0/90	0/90
									Bake at 150 °C (Hrs)			
									48	168	500	1000
							3	25	0/75	0/75	0/75	0/75
									Unbiased HAST 130 °C, 85% RH (Hrs)			
									96			
							3	30	0/90			
									Lifetest 1.2xVcc, Tj = 125 °C (Hrs)			
									200	500	1000	
							3	24	0/72	0/72	0/72	
									Temp Humidity Biased 85 oC/85% RH (Hrs)			
									500	1000		
							3	30	0/90	0/90		
Altera 28nm FPGA Device	40x40	18.8x14	1517	Pb-free	3	260			Temp Cycle Condition B -55/125 °C(Cycles)			
									200	500	700	1000
							3	30	0/90	0/90	0/90	0/90
									Unbiased HAST 130 °C, 85% RH (Hrs)			
									96			
							3	30	0/90			
									Temp Humidity Biased 85 °C/85% RH (Hrs)			
									500	1000		
							3	30	0/90	0/90		
Daisy Chain TV	42.5x42.5	22x18	1681	Pb-free	N/A	260			Board Level Temp Cycle (0-100 °C)			
									# of cycles completed		# of Failures	
							1	30	3500		0/30	
Daisy Chain TV (w/HS)							1	10	3500		0/10	

The results of the component and board level reliability tests show that the 28nm FPGA in the FCmBGA package meets the industry standard reliability test requirements. To confirm that there were no latent defects in the package after the reliability tests, detailed construction analysis was performed to check the condition of the bumps, substrate and the die. The construction analysis showed no defects in the substrate, Silicon low dielectric layers and the bumps.

Conclusions

Our joint collaboration has resulted in the developing the valuable customer collateral for the FCmBGA package selected for 28nm FPGA device family. The customer usability of the FCmBGA package is shown to be equivalent to the lidded flip-chip BGA package while offering advantages of a low profile package. The reliability tests show that the 28nm FPGA device in FCmBGA package meets the component and board level reliability requirements in compliance with the IPC and JEDEC standards. The results of this collaborative study show that the FCmBGA package offers advantages of high performance and low cost essential for the 28nm FPGA product family.

Acknowledgements

We would like thank to the Altera and Amkor management for their support for this study. Our special thanks to Vadali Mahadev, John Xie, Yuan Li, KB Lim, PB Lam from Altera and Mike Young from Betatron for their valuable contributions.

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