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Embedded System Access - a Paradigm Shift in Electrical Test

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Abstract

Throughout a product's life cycle it may need to be tested various times. New product designs need to be validated during the prototyping phase, manufacturing defects need to be detected and diagnosed during the production phase, and products may need to be tested and/or updated while they are in use at the end customer, while defective units returned from the field need to be retested. This paper discusses different test access methodologies and elaborates on Embedded System Access (ESA) strategies in particular, with examples for its use in practice.

1. Introduction

Test strategies for electronic circuits are graded by how close they come to the elusive ideal test solution that doesn't add any cost to the product under test, neither during the design nor during production. Most of us agree that product testing is absolutely necessary, as part of design validation, as a quality indicator for manufacturing process control, and for the detection of defective products prior to shipping them to a customer. Industry trends give cause for concern, though, considering that the cost of test today can be a significant part of the overall development and manufacturing cost. Responsible for this development are primarily circuit complexity, high-speed designs, and the lack of available test access on many of today's printed circuit board assemblies (PCBAs). The combined forces of these characteristics result in systematic changes in the balance of product design and product test. We start to see a correlation between problems seen in chip test and those seen in board test. While boards look more like integrated circuits (IC) due to the loss of access to internal circuit nodes, the rapid development of three-dimensional (3D) ICs with multi-die integration results in structures that are similar to boards and systems. 3D boards with very little physical access seem to be looming on the horizon. At the same time, the combination of new packaging and integration technologies result in hitherto unaccustomed complexity. While several years ago multiple boards were necessary to create complete system designs, today some such systems can be realized in integrated circuits as System-On Chip (SOC) or System-In Package (SIP) designs. As a result, board size can be minimized and new possibilities are available to create super-complex systems. No matter how a design is arranged, however, from the perspective of test engineering the fundamental question is how such highly complex systems can be tested appropriately and efficiently and how one can take advantage of synergies between chip test and board test approaches.

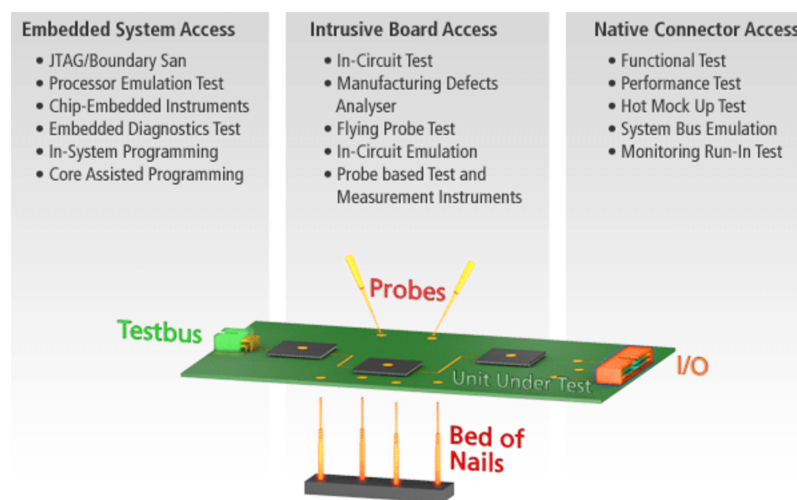

Figure 1: Classes of test access strategies

1.1. Transition to design integrated pin-electronics

We can differentiate three principle classes of test access strategies (figure 1):

- Native Connector Access (access through design integrated I/O interfaces),
- Intrusive Board Access (access through physical test nails and probes), and
- Embedded System Access (access through design integrated test bus).

While these classes are not mutually exclusive in their practical utilization, the applicability of an actual combination of these access strategies depends on the individual capabilities of the chosen automated test equipment (ATE) platform. "Divide and conquer" is a wise strategy that is also well suited for the test arena. Partitioning circuit structures into testable elements is a prerequisite for a successful test strategy. This is one of the reasons why in-circuit test (ICT) became so successful for board level tests. ICT approached circuit test structurally and tests components individually, however, the required bed-of-nail based invasive test access is becoming a big dilemma with modern boards. Test access problems were predictable quite some time ago, which resulted in the creation of IEEE Std 1149.1 in 1990 [1]. Developed by the Joint Test Action Group (JTAG), this standard moves the so-called pin-electronics of a tester into the unit under test (UUT) in order to enable non-invasive test access without bed-of-nail adapters. This design integrated pin-electronics is controlled through the JTAG test bus (figure 2), which needs to be incorporated into the unit under test by the board designer, making test access available implicitly rather than being an afterthought.

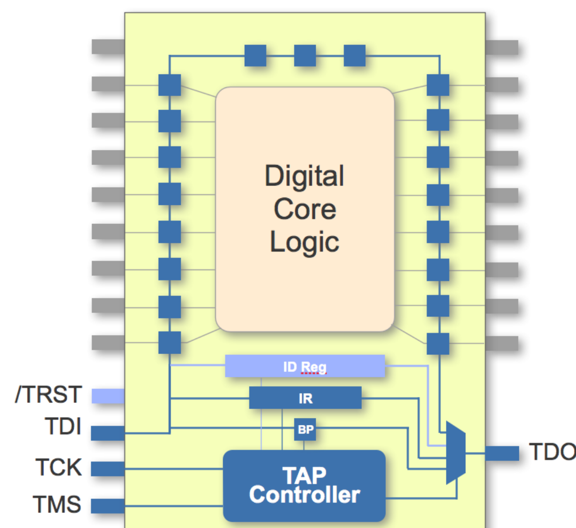

Figure 2: A boundary-scan enabled device
(digital core logic is surrounded by boundary-scan cells)

The key to success for IEEE Std 1149.1 was the open expandability of its register architecture combined with the universal test bus interface (Test Access Port, TAP) and its protocol definition. These properties allowed IEEE Std 1149.1 to become the base technology for new non-intrusive methodologies and standards for testing, debugging, programming, and emulation. And to keep up with the times, IEEE Std 1149.1 is currently being revised, with an updated version expected to be available in 2013.

1.2. Paradigm Change - a New Era Begins

A look at the qualitative development of trends for the various access strategies (figure 3) reveals interesting facts, including a long adoption period of IEEE Std 1149.1 as the first representative of Embedded System Access (ESA) technology.

Only four years ago has the boundary-scan industry reached annual sales of around 29 Million US Dollars, while sales of automated test equipment based on intrusive access strategies was in the range of 500 Million US Dollars [2] (it is important to keep in mind that the cost of boundary-scan test systems typically is much lower (by an order of magnitude) than that of in-circuit test and flying probe test equipment, for example). However, we now see the manifestation of a rapid transition from intrusive access strategies to embedded system access.

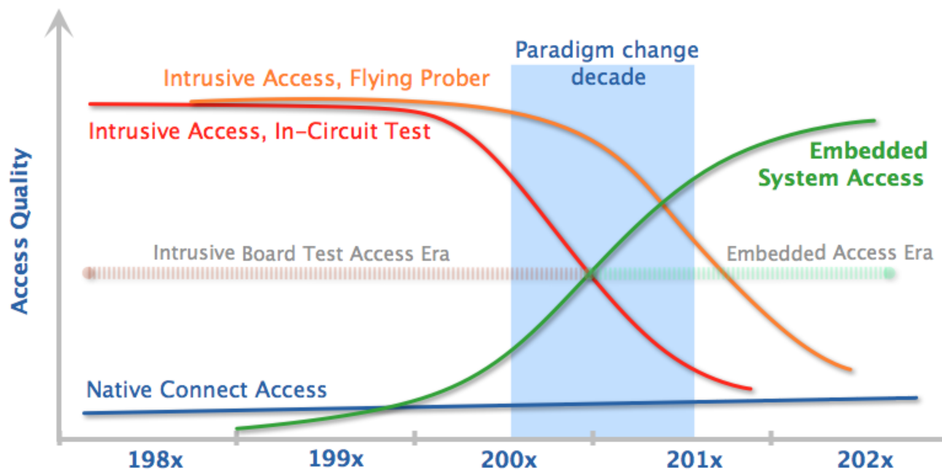

Figure 3: The rise of Embedded System Access

The accelerated adoption of embedded system access in the market is primarily owed to the fact that it is now a class by itself (as illustrated earlier in figure 1), encompassing a variety of non-invasive access technologies, including:

- Boundary-Scan Test (IEEE Std 1149.1, 1149.4, 1149.6, 1149.7),
- Processor-Emulation Test (PET),
- Chip-Embedded Instrumentation (IJTAG, IEEE P1687),
- In-System Programming (ISP),
- Core-Assisted Programming (CAP),
- FPGA-Assisted Test (FAT),
- FPGA-Assisted Programming (FAP), and
- System JTAG (SJTAG).

In addition, there are a number of other technologies and standards relying on on-chip resources, such as On-Chip Emulation (OCE) for software validation, and IEEE Std 1149.8.1 (combining boundary scan with test methodologies based on capacitive coupling sensors).

The electrical access embedded in the target system allows ESA strategies to work without invasive test nails and probes. In principle, every ESA technology utilizes task specific pin-electronics controlled by the test bus and, as a result, can directly execute test functions and programming routines in the target system. This target system can be an individual chip, a board, or a complete system assembly - ESA can be utilized throughout the entire product life cycle.

2. Embedded System Access (ESA) Technologies

A detailed analysis of key ESA technologies at the board level reveals considerable differences in operation and goals. Table 1 reflects the complementary character of the various technologies and, as the following discussion will further explain, it becomes clear how important it is for ATE platforms to support all these ESA technologies alike.

2.1. JTAG / boundary scan

Boundary scan utilizes so called boundary-scan cells, combined into a boundary-scan register, as primary access points for a target system's circuit nodes (see also figure 2). The boundary-scan register is accessed and controlled through the Test Access Port (TAP). All vectors are scanned serially. The test bus is comprised of four mandatory signals and a fifth optional reset signal. Boundary scan is a structural methodology and provides excellent fault diagnostics, especially for connectivity tests on BGA devices, for example [3]. However, since boundary-scan tests are static in nature, dynamic defects usually cannot be detected, let alone be diagnosed. In addition to IEEE Std 1149.1, various related standards have been created or are in development.

Processor Emulation Test

Processor Emulation Test (PET) utilizes the debug interface (implemented in many microprocessors for software validation) to transform the processor core temporarily into a native test controller (figure 4). The processor and its system bus interface become the pin-electronics used as access points for the connected circuitry in the target system. Remote-controlled through the JTAG interface or some other debug interface, the processor core utilizes write and read access to the system bus with respective test vectors in order to manipulate and test the connected internal and external resources and components. No operating system or firmware is necessary to accomplish this.

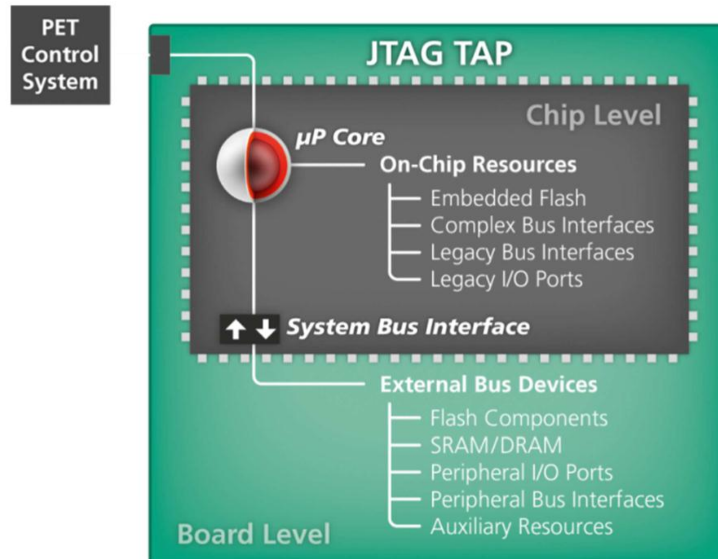

Figure 4: Principle of processor emulation test (PET)

PET can detect both static and dynamic defects; however diagnostics are limited due to the functional test approach. Complementing boundary scan very well, PET enables or improves especially the test of dynamic components such as DDR-SDRAM, Gigabit interfaces, and other non-scanable circuitry.

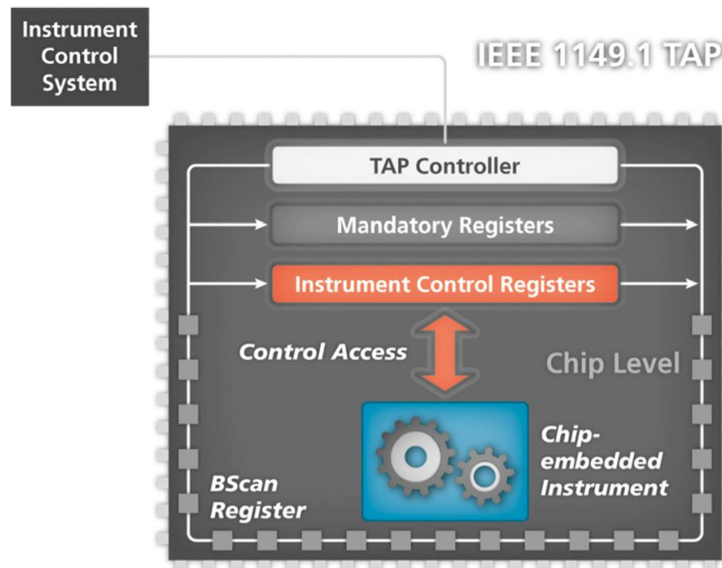

Figure 5: Principle of chip-embedded instrumentation

2.2. Chip-embedded Instrumentation

Chip-embedded instruments are test and measurement intellectual property (IP) blocks integrated into ICs, often accessible through the JTAG port (figure 5). The functionality of chip-embedded instruments is completely open and ranges from simple sensors, over complex signal processing and data collection, all the way to complete analysis instruments and programming engines. The IP is either integrated permanently in the chip (hard macro), or it can be temporarily instantiated and configured (soft macro) in Field Programmable Gate Arrays (FPGA).

As a result, the pin-electronics is unrestricted in principle and can provide a wide variety of functionality, within the technological capabilities of the respective host device, of course. Also noteworthy is the fact that such chip-embedded instruments in principle can be active during normal system operation, which enables interesting test and debug applications.

2.3. FPGA Assisted Test and FPGA Assisted Programming

In particular FPGA-embedded instruments have enjoyed strong interest recently. By enabling strategies such as FPGA Assisted Test (FAT) and FPGA Assisted Programming (FAP) they provide enormous flexibility for the adaptation to individual test and measurement requirements. Chip-embedded instruments have been utilized for years in chip test, for example in form of built-in self-test (BIST) IP. However, access to these instruments has not been standardized in the past, something that will be changed with the new IEEE P1687 (also known as IJTAG).

One of the most interesting technologies for in-system programming (ISP) of Flash devices, referred to as FPGA Assisted Programming (FAP), is based on FPGA-embedded instruments. In this case the embedded instrument is a programming engine (programmer) soft macro, typically provided by a tool vendor and temporarily downloaded into the FPGA. Depending on the architecture of the programmer IP and the performance of the external control system, drastic improvements in programming speed compared to boundary-scan based ISP are possible.

Table 1 – Comparing ESA technologies relevant to board level test

Property	Boundary-scan test	Processor emulation test	Chip-embedded instruments	FPGA assisted test
Test type	structural	functional	depends on implementation	depends on implementation
Test speed	static	dynamic	depends on implementation	depends on implementation
Access method	boundary-scan IC	processor core	IJTAG IC	FPGA
Pin-electronics	boundary-scan register	system bus	IP interface	IP interface
Configurable IP	no	no	depends on implementation	yes
Fault coverage	static	dynamic	depends on implementation	depends on implementation
Level of diagnostics	pin	net / pin	depends on implementation	depends on implementation
Related IEEE standard	IEEE Std 1149.x	IEEE Std 1149.7, ISTO 5001 / Nexus	IEEE Std 1149.1, IEEE Std 1149.7, IEEE P1687	IEEE Std 1149.1, IEEE Std 1149.7, IEEE P1687

2.4. In-System Programming

The important area of device programming, too, benefits from a number of different ESA technologies. By utilizing primarily the same infrastructure as the previously discussed test solutions, a high degree of synergy between test and programming applications can be obtained.

In-system programming (ISP) is a collective term for the programming of Flash and serial EEPROM devices via boundary scan and for the programming of PLD/FPGA devices through their Test Access Port (TAP) and built-in programming registers, while the devices are mounted on the printed circuit board. For in-system programming of PLD/FGPA, special standards exist, such as IEEE Std 1532, JESD-71 (STAPL), and an industrial standard called Serial Vector Format (SVF).

2.5. Core-Assisted Programming

The premise of the core-assisted programming (CAP) strategy is similar to processor emulation test. The processor core is controlled through its native debug interface in a way that allows Flash or FPGA (design permitting) connected to the system bus to be erased, programmed, and verified (figure 6).

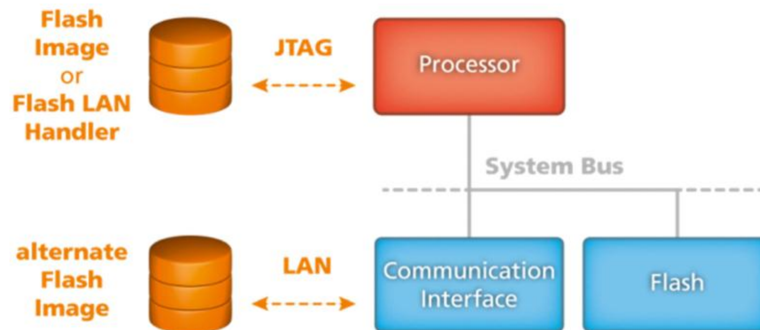

Figure 6: Principle of core-assisted programming (CAP)

In the case of Flash it does not matter whether it is integrated in the processor / micro controller unit (on-chip Flash) or connected as external, discrete Flash device(s). Furthermore, it is possible to load only the Flash handler / programming engine via JTAG into the processor and to download the Flash data image through a high-speed communication interface on the processor [4]. CAP technology provides much higher in-system programming speed than boundary-scan based device programming.

Table 2 – Comparing ESA technologies relevant for device programming

Property	In-system PLD programming	In-system Flash programming	Core assisted programming	FPGA assisted programming
Target device	PLD / FPGA	Flash	MCU / Flash	Flash
Speed	medium - high	low - medium	high	high
Access method	PLD / FPGA	boundary-scan IC	processor	FPGA
Pin electronics	ISP register	boundary-scan register	system bus	IP interface
Configurable IP	no	no	no	yes
Related IEEE standards	IEEE Std 1149.1, IEEE Std 1532, (JESD 71)	IEEE Std 1149.1, IEEE Std 1149.7	IEEE Std 1149.1, IEEE Std 1149.7	IEEE Std 1149.1, IEEE Std 1149.7, IEEE P1687

2.6. System-level Test

The last access technology in this discussion is referred to as system-level JTAG. While remote control through an external controller is possible, this technique typically employs a central test control unit integrated directly into the system design. As illustrated in figure 7, test vectors are usually stored locally on the system and a separate IC is commonly used as the test bus controller (although, there is also the possibility to integrate the test bus controller function in an IC that also performs other functions in the system design). As the name implies, this method can be employed not only for individual boards but also for systems comprising multiple boards and modules. The SJTAG initiative is looking at standardizing system level JTAG [5].

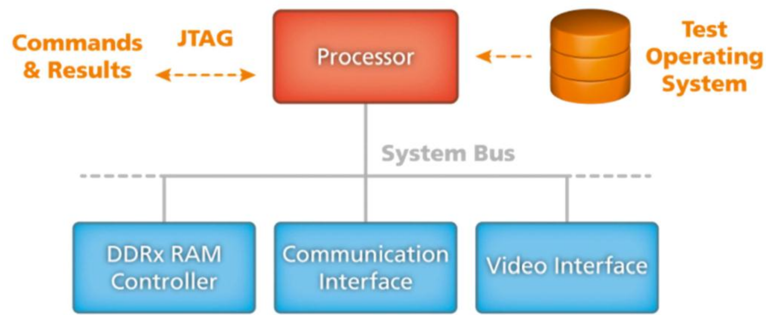

Figure 7: Principle of system-level JTAG controlled test

3. Embedded System Access (ESA) Example Applications

Figure 8 illustrates a number of possible applications made possible by embedded system access technology introduced on the previous pages. These applications are discussed at a high level in the following sections.

Figure 8: Example ESA applications

3.2. JTAG scan chain

Typically the first test created and executed in the context of JTAG / boundary scan is the scan chain integrity test, or infrastructure test. This test verifies that the scan chain (the test bus) functions properly, test pattern can be transmitted, and the correct boundary-scan devices are mounted on the unit under test (UUT).

3.3. Connection test

The connection test, or interconnect test, verifies connectivity between boundary-scan enabled devices on the unit under test. This test focuses on the detection of open pins, shorted circuit nodes, and stuck signal levels, utilizing pin control provided by the boundary-scan cells in IEEE 1149.x compliant devices. The connection test often includes so called transparent circuitry, such as buffer devices, logic gates, and in-line resistors.

3.4. Buffer test

Buffer devices, especially bi-directional transceivers, and glue-logic circuitry on the UUT often are tested more extensively in so called cluster tests. While the connection test discussed above may test some aspects of these types of circuit clusters, additional test pattern are often needed for a thorough test and to detect and diagnose most defects inside such clusters.

3.5. DDR SDRAM test

DDR SDRAM, as well as other memory devices, can generally be tested with access from boundary-scan enabled devices, as long as access to all required memory pins is available (including clock signals). Due to the pseudo-static nature of boundary-scan test vectors, though, such memory access tests cannot really be considered dynamic, which means that certain defects may not be detected. Also, the test execution time is relatively long (compared to connection test, for example). Very few memory devices have IEEE 1149.1 features implemented, which means that boundary-scan based memory access tests rely on writing pattern to certain memory addresses and then reading the pattern back. This write and read access happens at a much slower speed with boundary-scan access than what one would see during normal, functional access. This is one example where processor emulation test or chip-embedded instrumentation can enhance the fault coverage and the test execution speed compared to boundary scan. Processor emulation can be used to write and read the memory at functional speed, while still providing the same diagnostic detail obtainable with boundary-scan access, and chip-embedded instrumentation may provide built-in self-test (BIST) features for high-speed test of memory interfaces, for example.

Interesting to note in this context is the availability of IEEE Std 1581 - a fairly new standard defining a low-cost method for testing the interconnection of discrete, complex memory ICs.

3.6. Digital I/O test

Some signals may go to peripheral connectors on the UUT. Such connector pins cannot be tested for open defects, unless additional test resources are utilized, such as I/O modules wired to the connector, or capacitive coupling sensors if the UUT signals support IEEE Std 1149.8.1. With such additional resources, or even with a simple loop-back connector, such peripheral I/O can be included in boundary-scan connection tests.

An alternative approach may utilize processor emulation or chip-embedded instrumentation on the UUT and configurable digital I/O modules connected to the peripheral interface. With appropriate control sequences, such a setup can offer more dynamic fault coverage than what would be possible with boundary scan only.

3.7. USB and LAN Interface tests

USB, Ethernet/LAN, and similar communication interfaces often cannot be tested with boundary scan because the necessary access is not available (no boundary-scan cells connected to the signals required to control the respective interfaces) or because boundary-scan access cannot satisfy the interface timing requirements. In these cases, processor emulation or chip-embedded instrumentation, accompanied with additional tester resources connected to the interface ports, are key to obtaining test coverage.

3.8. Display and LED test

LCD displays and LEDs, or other optical indicators, can be included in boundary-scan based test strategies if the operator is visually inspecting the display element to verify that it behaves as expected under control of the boundary-scan resources connected to it, or if the test system is utilizing a camera setup for automated optical inspection, synchronized with test pattern applied by the boundary-scan resources involved in the test.

3.9. Button test

Similar to a display test, an operator or an automated actuator can push a button or switch while connected boundary-scan resources test the UUT for the expected signal change(s).

3.10. Gigabit I/O test

Similar to USB or LAN interface tests, Gigabit I/O tests require processor emulation or chip-embedded instrumentation for proper and thorough testing. Specifically, bit error rate testing comes to mind.

3.11. BGA debugging

Sometimes the most urgent need is not a complete set of test programs but rather the ability to stimulate and observe specific UUT signals. Boundary scan is a perfect resource for such debug tasks. The target device can be put into boundary-scan test mode, offering simple access to and control over the I/O pins on the device, and allowing selective and targeted stimulus to be applied to - and responses to be observed and returned from - the UUT circuitry. Both the standardized SAMPLE and EXTEST instructions are useful for such debug applications.

3.12. Voltage measurement

If the UUT includes A/D converters (ADC) and the digital interface is accessible by boundary-scan resources, then this access can be utilized to measure analog voltages on the signals the analog interface(s) are connected to. If boundary-scan access is not available, processor emulation can be a good alternative access methodology. Some micro controllers and mixed-signal FPGAs may even include on-chip ADCs that can be accessed and controlled through the component's JTAG interface, allowing for respective mixed-signal tests.

3.13. Frequency measurement

While boundary-scan access can be utilized to detect whether a clock signal is toggling or not, due to the nature of boundary scan this methodology does not allow an actual clock frequency measurement. However, a device may have chip-embedded counters that can be accessed through its JTAG interface. In the case of an FPGA, for example, one can load the FPGA with an IP that allows actual clock frequency measurement by essentially bypassing the boundary-scan register and using the JTAG interface only for IP download and control, and for retrieval of the measurement results.

3.14. Temperature measurement

Discrete temperature sensors often provide a serial control interface (e.g. I2C or SPI) that may be accessible from a boundary-scan enabled device. In such a case, boundary-scan access can be utilized to read out the measured temperature. Certain micro controllers, processors, ASICs, or FPGAs may feature embedded ambient or spot temperature sensors that are accessible through the JTAG interface, allowing direct measurement and retrieval of temperature values.

3.15. Analog I/O test

Similar to digital I/O test, analog I/O test relies on external tester resources or a loopback between UUT integrated D/A converter (DAC) and ADC circuitry. If boundary-scan access is available to the digital interface of the analog circuit cluster, a boundary-scan controlled test can be suitable; otherwise one may turn to processor emulation or possibly other embedded system access strategies.

One option to keep in mind for analog and mixed signal test in general is IEEE Std 1149.4. While seemingly not in wide use today, this standard defines test resources for mixed-signal boundary scan testing.

3.16. PLD/FPGA programming

PLD, FPGA, and configuration PROM devices typically are programmed through their respective JTAG interface. Such devices have embedded programming engines and registers that are accessible through their JTAG interface and typically don't rely on any other resources on the UUT (other than power, of course).

3.17. MCU high-speed programming

Micro controller units (MCU) often have embedded Flash memory to store boot code and firmware. This Flash memory typically can be programmed through the MCU's JTAG port or some other debug interface.

3.18. High-speed programming for Flash / serial EEPROM

Both serial EEPROM and parallel NAND and NOR Flash devices typically can be programmed through boundary-scan access from some other device on the UUT (such as a micro controller, CPLD or FPGA, or DSP, for example). However, this boundary-scan controlled in-system programming takes a long time compared to the functional programming speed of the target devices. Therefore, it is more desirable to utilize core-assisted or FPGA-assisted in-system programming access, allowing a much higher programming speed.

4. Transformation to the System-Integrated Tester

The transition from traditional invasive test access and techniques to embedded system access is not a marginal change in the handling of test and programming vectors but rather a fundamental technological metamorphosis. Characteristics of these changes include:

- Integration of test electronics in the system under test,
- Inseparable coupling of functional and test circuitry in the system design,
- Forming of partitioned test centers with various features,
- Significantly wider range of test and programming strategies,
- Possible utilization throughout the entire product life cycle,
- Flexibility of re-configurable pin-electronics with FPGAs, and
- Availability of completely new instrumentation platforms.

In practice, ESA represents a transformation from a purely functional design into a functional design with integrated test capabilities, a combination of unit under test and tester, so to speak. Depending on the actual implementation of ESA, a wide variety of applications is possible. Currently, FPGA-based test in particular is a technology driver for progressively more complex test and measurement functions, including applications such as voltage measurements, frequency measurements, temperature measurements, Bit Error Rate Tests (BERT) for high-speed signals, event counters, logic scopes, and many more. As a result, extensive design validation is possible in the lab or even at the designer's desk through one central communications and control channel.

One big advantage of this methodology is that signals are accessible and measurements are taken directly inside the circuitry, avoiding artificial interference and distortion caused by mechanical probes, cables, and additional electrical loads, for example. With ESA the test and measurement results are not only more accurate but also more reproducible. Of course, for an efficient application of ESA techniques respective external instrumentation is needed.

5. Multi-dimensional Requirements for Tester Instrumentation

In this paper, we have primarily talked about JTAG as the test bus interface. However, there are also a number of proprietary bus interfaces used in the industry, in particular for debug interfaces on processors, such as Serial Wire Debug (SWD), Spy-Bi-Wire (SBW), or Background Debug Mode (BDM). For test equipment vendors this means that their test bus controllers need to provide the required flexibility to support any of such interfaces; even a mix of different test bus interfaces in multi-processor applications should be supported. Furthermore, the various ESA technologies must be supported by powerful software tools and must be made available to the user in intuitive graphical user interfaces. In this context we need to consider not only the independent use of individual ESA methods, but also the potentially interactive application of various ESA technologies in order to gain extra benefits (such as improved fault coverage, for example).

This last requirement directly leads to another important topic: the combination of embedded system access with other access technologies, such as Invasive Board Access (IBA) and Native Connector Access (NCA), allowing embedded system access to be migrated into already existing test systems.

In order to support this level of interactivity, ESA test equipment needs to provide very good integration features and must be available for all important integration platforms. Functional test in particular will play an important role, considering the continued rise of very powerful and open test and measurement platforms (such as PXI and LXI).

In the end, the transition to embedded system access with all its facets requires a completely new class of JTAG / boundary-scan instrumentation, putting enormous pressure on ATE vendors. Solutions are available in form of multi-dimensional JTAG / boundary-scan platforms. The term "multi-dimensional" reflects the support of the various dimensions and complexities of parameters, structures, functions, interactions, applications, and access technologies that come with embedded system access. One of the first such platforms is based on SCANFLEX hardware [6] and SYSTEM CASCON software [7].

6. Conclusion

The trend of employing non-invasive test access strategies, initiated in 1990 with the ratification of IEEE Std 1149.1, has spawned a number of new technologies and methodologies which combined have given birth to the category of embedded system access techniques. The essence of embedded system access is the provision of test pin electronics in the target system itself. Activating ESA results in a temporary transformation of the respective system, allowing it to be tested in partitions by means of embedded test centers under control of the integrated test bus. Key elements of this infrastructure include boundary-scan devices, microprocessors, FPGAs and devices (such as ASICs) with chip-embedded instruments. The transition to embedded system access enables the observation and stimulation of signals directly in the circuitry, without signal distortion created by cabling and probing, making ESA a perfect foundation for the test of high-speed signals. At the same time, ESA provides enormous potential for completely new test and measurement applications, which require a new generation of ATE solutions. Pioneers in this arena are multi-dimensional JTAG / boundary-scan instrumentations platforms with capabilities for interaction with other test access technologies.

Further developments in embedded system access will be influenced by new standards related to the test bus interface, such as IEEE Std 1149.7, and by the control of chip-embedded instruments as defined in IEEE P1687 and through features defined in the latest revision of IEEE Std 1149.1. In addition, especially new instrument IP - either as hard macros or as FPGA embedded soft macros - will drive the innovation in test, measurement, and programming applications and will continue to blur the lines between chip test and board test.

We don't expect the industry as a whole to suddenly change direction to embedded system access as the strategy of choice within the next few years; migration strategies and combinations of access techniques will be the key, since invasive test access will remain widely used during this decade.

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