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Embedded Components: A Comparative Analysis of Reliability Part II

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Abstract
In light of new process and product technologies in the field of embedded components, questions arise with respect to advantages and potential disadvantages to standard SMT component placement when considering reliability.

This paper is the second part in a progressively complex series of comparative analyses, testing the reliability of standard SMT components in comparison to their embedded counterparts.

In the initial round of comparative tests, we analyzed passive components. In this second part we will compare the performance of similarly specified embedded dies and standard surface mounted CSPs which are designed to simulate an active component ("dummies") in terms of interconnectivity
The applied reliability tests shall include:

- Drop Test per JEDEC JESD22-B111: 1500g / 0.5ms
- Thermal cycle testing (TCT) per JEDEC JESD22-A104: -40°C / +125°C
- Bend Testing – Based on the IPC/JEDEC 9702 (Monotonic Bend Characterization of Board-Level Interconnects)

With these tests, as with the initial paper on embedded passives, we aim to define possible limitations, advantages, disadvantages and areas of functional application which are relevant to this direct comparison. With the addition in this study of one mechanical bend test we hope to introduce a more well-rounded picture of the reliability one should expect for different instances and component placement methodologies.

As the usage, as well as fields of application, of embedded components increases in part due to more stable and refined methods of manufacturing, it is worthwhile to examine them based on industry norms and standards as a source of comparison to traditional manufacturing methods. Part of this analysis is therefore to investigate the feasibility of employing such standards in the context of embedded components. This investigation, in turn, should offer us a holistic perspective to other current industry projects, such as the EU-funded "Hermes".

Introduction

The decision to carry out such comparative analysis on active components was a logical step after testing passives in the first instance. Given the initial results on passive components someone might question new technologies in embedding in combination with bigger components. What advantages/disadvantages would be apparent when compared to the "traditional" method of surface mount technology (SMT)? Would there be any reliability differences between passives versus actives?

Of course to explore all performance indicators (electrical, mechanical, thermal) and all possible interactions between various materials and components would deserve a more intensive research program, such as the HERMES project (an European Union funded multi-company project), but in this instance the target was to find a more practicable approach to a tangible problem: connective reliability under stress.

Drop test and thermal cycle test (TCT) were chosen as two indicative (albeit not exhaustive) reliability test-methods as in the first paper [1]. Additionally we introduced one mechanical stress test to perform a more well- rounded picture of the overall performance. The test vehicle (a more detailed description can be found in the paper) was designed to be as "standard" as possible and the components chosen were selected based on their commonplace application in the SMT world. Furthermore the test board, by including the SMD (Surface Mount Device) and embedded components on the same vehicle, was designed to ensure that both sets of components were subjected to the same stress elements during testing. This also allows a direct comparison to the initial paper.

The hypothesis of the experiment was twofold:

- Drop test – Due to the locative nature of the embedded components, i.e. embedded between layers of pre-preg in the PCB core and therefore closer to the center point of the PCB construct, and the plastic nature of the resin surrounding the component, it was hypothesized that the drop test performance would exceed that of the standard SMT component, which was exposed to higher energy potentials on the outer layer.

- TCT – It was hypothesized that the TCT performance of the embedded components (EC) would at least be par to if not exceed that of standard SMT components.

- Bend Test- Introducing mechanical stress and referring to the neutral axis model, embedded components reliability should outperform standard SMT

The results, as the paper will demonstrate, essentially cover the original hypotheses and therefore may serve as a basis of understanding the EC concept and some possible applications. Furthermore, the results may be seen as a basis for additional and more complex investigation (comparative or singular).

In terms of orientation, the paper is divided into three basic sections: Test Preparation, Reliability Testing and Evaluation.

Test Vehicle

As there is currently no standard test vehicle for testing reliability of embedded components, an attempt was made to base the vehicle as much as possible on the standard JEDEC drop test vehicle design (figure 1).

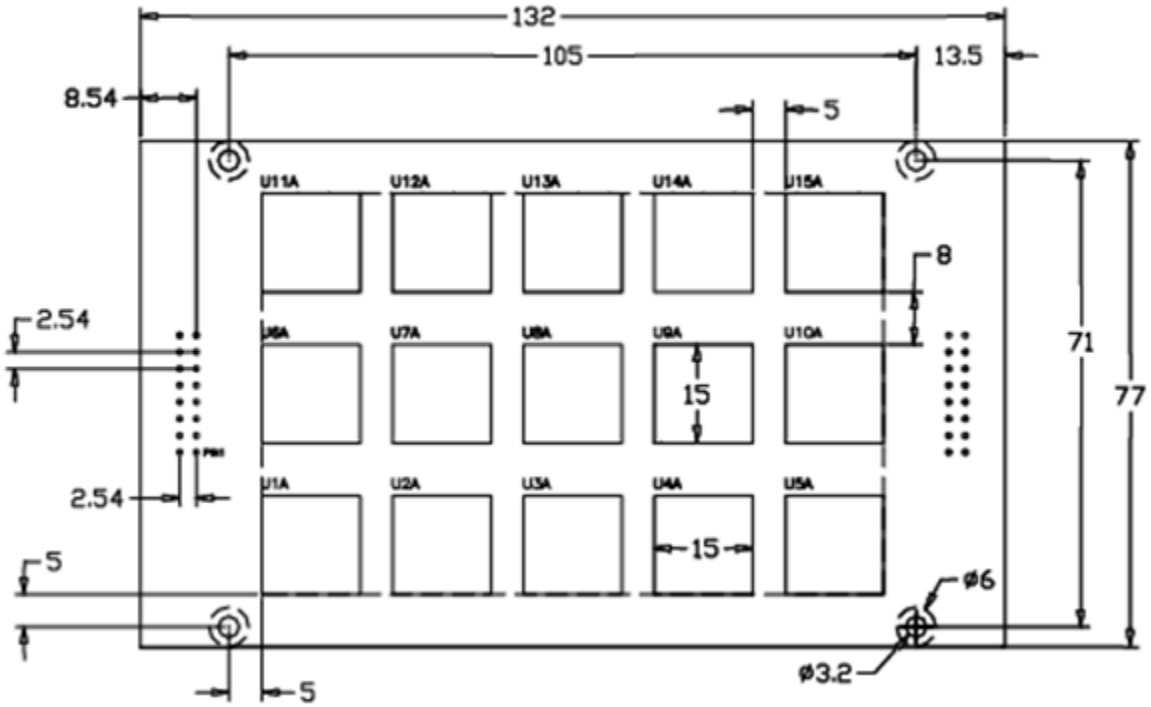


Figure 1 – JEDEC Standard no. 22-B111 Chapter 5.2.1 "Preferred board construction, material and design"

The embedded components test board (we will refer to as ITE2000EC) retains the same outer dimensions (132mm x 77mm) and thickness (1mm) as the standard JEDEC vehicle. There were changes made to accommodate for some of the features of our test. This includes changing the standard BGA test pattern to a multi- terminal contact pad configuration to account for the mounting of active components instead of BGA components.

The circuit patterns were configured to supply a daisy-chain test pattern in order to offer better event traceability during and after testing (figure 2). This pattern is essentially mirrored on the inner layer embedded pattern, but with the one distinction the daisy chain 9 and 11 on the outer layer and daisy chain 4 and 6 on the embedded layer were not superimposed over each other in order to assess any possible performance influence between components stacked over one another (figure 3). The 16 PTH test terminals at each end of the board were left in the design, but not all were utilized as illustrated in figure 3.

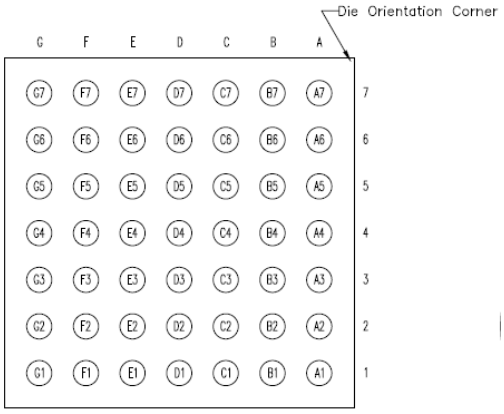


Figure 2 – Daisy chain test pattern on ITE2000EC

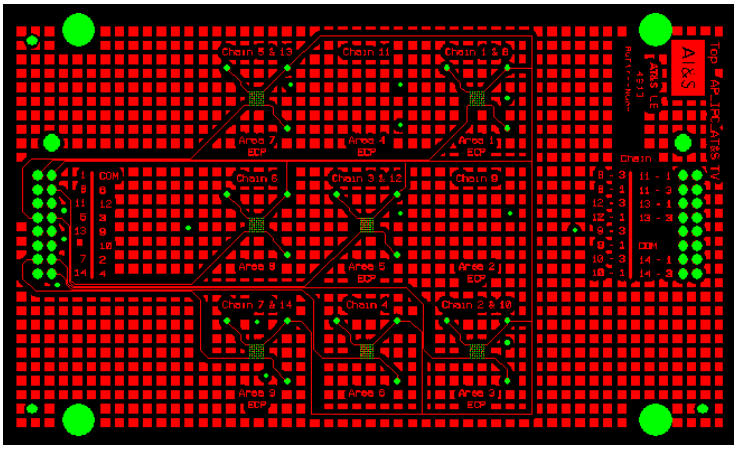


Figure 3 – Outer layer circuit pattern of ITE2000EC

The build for the PCB was an 8 layer multi-layer (figure 4). The unused copper on all inner layers was "hatched", which means they were not full copper surfaces. This is standard practice in PCB design to achieve stable thermal and therefore thermo-mechanical performance (i.e. warpage control). The material chosen for the PCB was a halogen free epoxy resin based prepreg. This material reflects a standard material in HDI application and is by no means a material with specialized characteristics for embedding components.

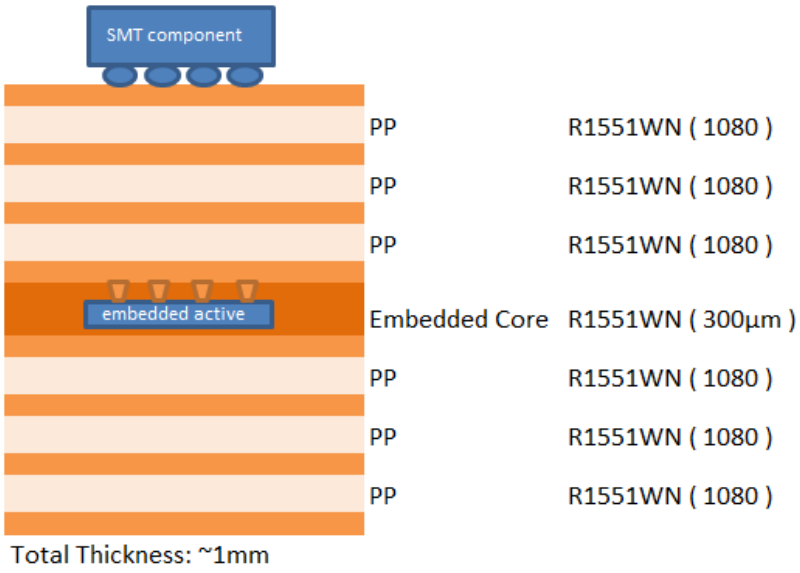


Figure 4 – Board Build up

Components
In general, it was decided to create this vehicle using active daisy chain components (CSP in this case) due to the ease of testing without excessive manufacturing performance variability. In other words, active components generally carry additional testing and performance aspects which require a more devoted research scope and a broader array of test types and participants. Such research is certainly ongoing elsewhere (e.g. with the EU- funded HERMES project, as mentioned above), but the target of this experiment was to set up a practical illustration using as many standards (tests, material, design, etc) as possible. Therefore we used a typical daisy chain set up instead of full functional active components.

Standard daisy chain components with 7x7 I/Os were used due to their commonality in both SMT manufacturing and the current embedded component manufacturing at the facility where the test vehicle was produced. The choice should represent a practical application, but is certainly not the only choice which could have been made.

The embedded components are similar active daisy chains in terms of the x and y axis (figure 5) and the electrical function matches that of the SMD component. The Z-axis differs in that it is thinner than the standard SMD (figure 6); SMD height of 550µm vs. an embedding height of 165µm as shown in figure 5. The same component manufacturer was used for both SMD and embedded components in order to exclude any additional variability.

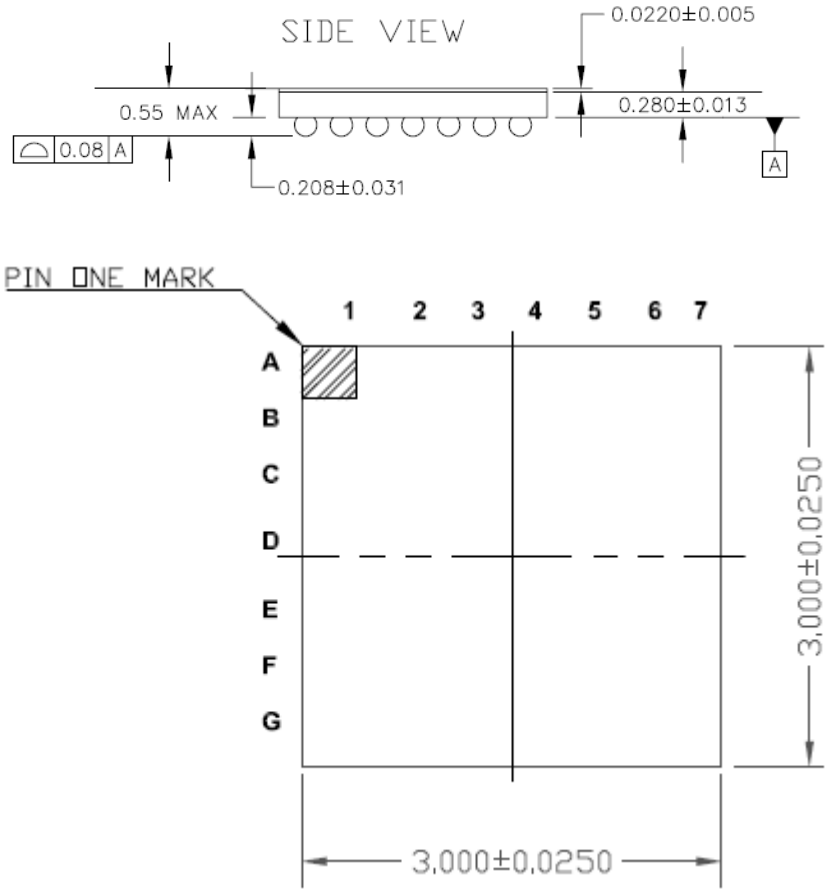


Figure 5 – EC and SMD have same x and y axis dimensions

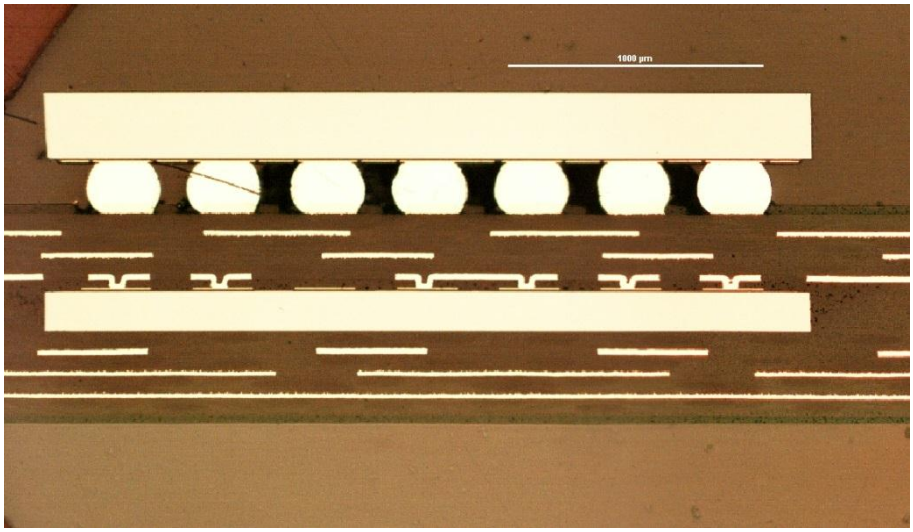


Figure 6 - EC and SMD vary in z-axis dimension

Due to the nature of the varying methods of achieving connectivity, the terminals of the components also vary. The SMD component is supplied with solder spheres for the SMT assembly process, whereas the EC has copper terminals. The background and application of the copper terminals will be evident in the "Production" section of this paper.

Production

Production of the test vehicle used in this experiment was carried out in Austria, using the company facility for embedded PCB manufacturing and a contract manufacturer for SMT assembly.

The embedded actives were assembled at the core layer of the build and are essentially encased in prepreg. The core copper layers were subsequently processed with photo dry-film and DES (Develop Etch Strip) to reveal the final core layer circuit patterns.

Connectivity to the copper plane and therefore the test circuitry to the PTH test terminals was achieved by forming laser vias (µ-vias) from the copper cladding of the core to the copper terminal of the embedded component and copper plating the µ-via subsequently (see figure 7). The diameter of the vias is 80µm.

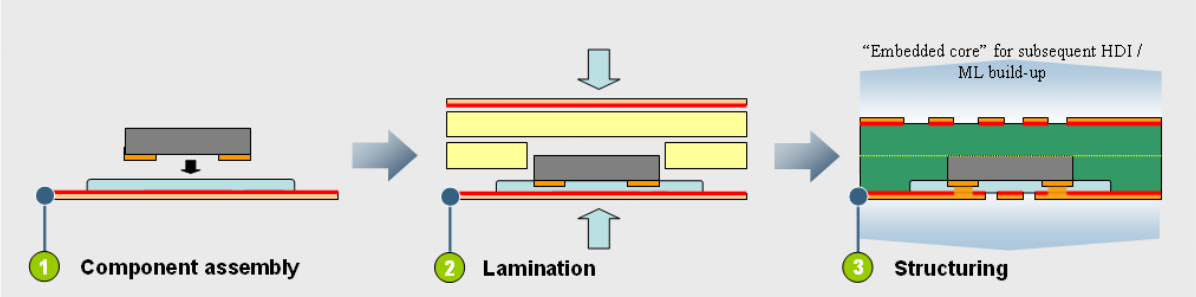


Figure 7 – Basic assembly method of the embedded core

This laminated "embedded core" underwent three further standard pressing cycles to achieve the final 8 layer construction.

Reliability Testing

One of the more obvious characteristics of embedded components (pertaining to the manufacturing method discussed here) is the fact that they are encased within the PCB, therefore surrounded by the resin and glass fiber of the prepreg. Any external stress would theoretically be distributed within the whole construct and less on the component itself, as opposed to an SMD component and solder joint system, which being on the outer layer is directly exposed to a stress source. The central location of the embedded components is also more neutral when considering mechanical stresses to the planar rigidity of the PCB. Furthermore, the mode of connectivity present in the applied manufacturing method (see Production) would theoretically be less stratified in metallurgical terms (compared to a component/solder alloy/copper pad system as present in SMT).

Drop test, TCT and Bend Tests were chosen as possible verifying reliability test methodologies of this hypothesis due to their common usage within the PCB manufacturing and OEM industries. In this section we will handle each test separately and supply the results accordingly.
The evaluation of the results shall follow in the "Evaluation" section of the paper.

Drop Test

The drop test specification was based on the JEDEC JESD22-B111 (see table 1). The test vehicle ITE2000EC was soldered at the test terminal PTHs as demonstrated in figure 8 below. Test events were monitored online as opposed to post testing and verification.

Table 1: Drop Test Specifications

DT Device	
Company Spec	TI.GR.PH-LAB-33EG
IPC	JEDEC JESD 22B111
Acceleration	1500g ± 10%
Pulse Duration:	0.5ms ± 10% (peak width at 10% of maximum pulse height)
CPK:	>1.3
Measurement Current:	1.0mA
Voltage	1.0V
Resistance:	1000 Ohm
Tested Structures:	SMD and EC – daisy chains (assembled cards)
Pass/ Fail – Criteria	Minimum acceptance criterion for components is 10 drops of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.

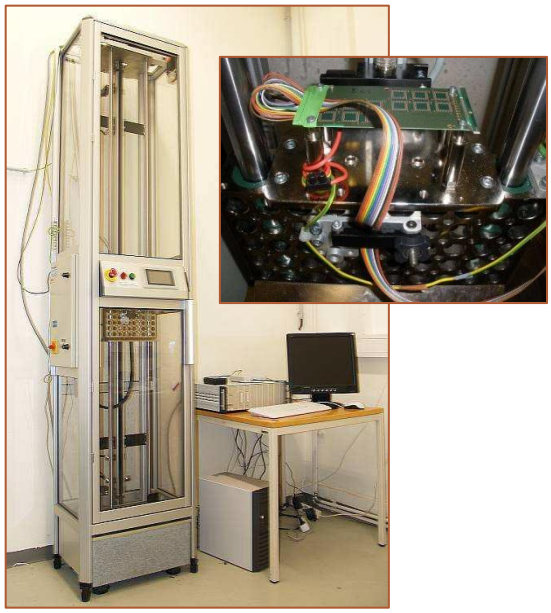


Figure 8 – Drop Test Device and Test Terminal Set-up

The test vehicle was not prepared in any other relevant manner beyond the soldering of the test terminals to the event recording wire bundle. Ten cards were tested according to the above mentioned test specifications (table 1). The cards were dropped until a resistance value of >1000 Ohm was registered (an "event"). Thereafter, approximately five additional drops were carried out to verify the >1000 Ohm resistance change. Once verified, the location of the exact component (SMD or EC) was determined using the terminal PTHs and the test pads. Once the component was identified, cross section analysis was carried out to determine the failure mode.

Drop Test Results

The results of the drop testing yielded the following results, which are also depicted in table 2. Four out of fourteen test

vehicles revealed SMD related defects before 1,000 drops. The earliest drop failure was recorded at 792 drops. Table 2 provides an overview of the drop test results. Figure 9 displays the positions of the component daisy chains and highlights the failure areas per chain: red depicts embedded only, yellow embedded and SMD and dark grey SMD only. Light red frames indicate the failed daisy chain location (figure 9).

Table 2 – Drop Test Failure Occurrence Overview: SMD vs. EC (red indicates earliest failure)

		SMD							ECP						
Card	First Failure	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1															
2			798												
3															
4															
5															
6	792				792										
7															
8		912					852								
9															
10															

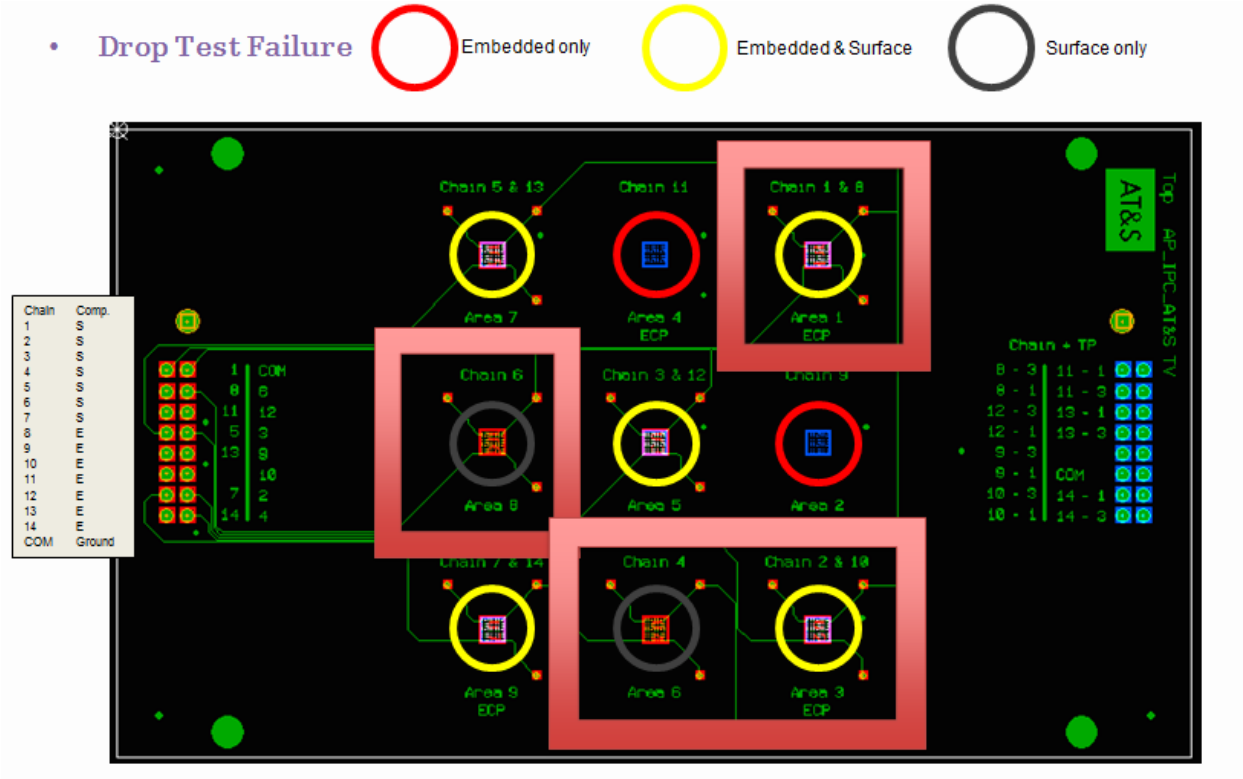


Figure 9 – Overview of component positions: Solid circle indicates failures.

One can see a prevalence of failure in SMD chain 1, 2, 4 and 6 (marked in red in figure 9). A possible mechanism behind this failure frequency will be discussed in the "Evaluation" section of this paper.

Drop Test Failure Modes

As discussed above, the SMT variant demonstrated a comparatively low drop test performance versus the ECs. There was one basic failure mode for the SMT failures: solder cracking near the component side of the solder joint. The solder crack occurred on all 4 daisy chains and is consistently located on the upper area of the solder ball close to the component side of the solder joint (figure 10).

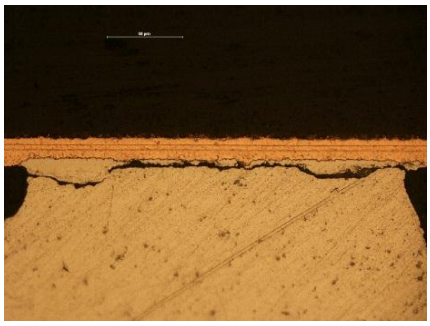


Figure 10 – Examples of drop test failure mode "solder cracking"

TCT (Thermal Cycle Test)
The TCT specification was based on the JEDEC JESD22-A10$ (see table 3). The test vehicle ITE2000EC was soldered at the test terminal PTHs. Test events were monitored online as opposed to post testing and verification (figure 11).

Table 3 – TCT specifications

TCT Device	
Company Spec	TI.GR.PH-LAB-51EG
IPC	JEDEC JESD 22-A104C,Test Condition G,2,C
Chamber	One chamber design
Chamber parameter	<table><tr><th>Step per cycle</th><th>Chamber</th><th>Sample Temperature</th><th>Min. Soak Time</th><th>Cycle count[3]</th></tr><tr><td>1</td><td>Cold</td><td>-40 +0/-10℃</td><td>5min</td><td rowspan="4">1000</td></tr><tr><td>2</td><td>Heat-up</td><td>-</td><td>-</td></tr><tr><td>3</td><td>Hot</td><td>+125 +15/-0℃</td><td>5min</td></tr><tr><td>4</td><td>Cool-down</td><td>-</td><td>-</td></tr></table>The heating and cooling rate has to be set in such a way that in total 2 cycles per hour are achieved.
Measurement system	Event detection 4-point measurement
Test structures	Assembled cards
Resistance for fail event	≥1000 Ohm
Pass/ Fail – Criteria	Assembled cards: Minimum acceptance criterion for components is 500 cycles of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.

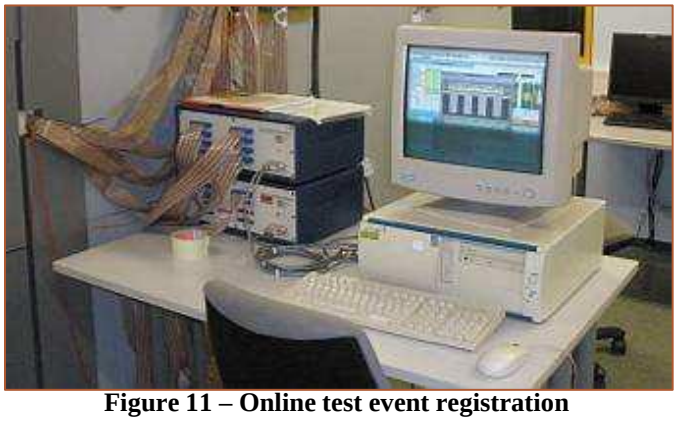


Figure 11 – Online test event registration

The test vehicle was not prepared in any other relevant manner beyond the soldering of the test terminals to the event

recording wire bundle. Ten cards were tested according to the above mentioned test specifications (table 3). The cards were cycled until a resistance value of >1000 Ohm was registered (an "event"). Once verified, the location of the exact component (SMD or EC) was determined using the terminal PTHs and the test pads. Once the component had been identified, cross section analysis was carried out to determine the failure mode.

The boards were subjected to a constant change in temperature in the range of -40°C ↔ +125°C in a chamber test device. The amount of cycles deemed as target was 1,000 cycles.

Figure 12 – TCT Test Results

Sample ID	Card	Structure No.	failed at cycle	Surface/Embedded
ITE2000_18_str4	18	4	684	S
ITE2000_20_str6	20	6	764	S
ITE2000_16_str6	16	6	786	S
ITE2000_15_str6	15	6	803	S
ITE2000_20_str4	20	4	818	S
ITE2000_11_str6	11	6	835	S
ITE2000_14_str4	14	4	853	S
ITE2000_19_str4	19	4	900	S
ITE2000_15_str4	15	4	999	S

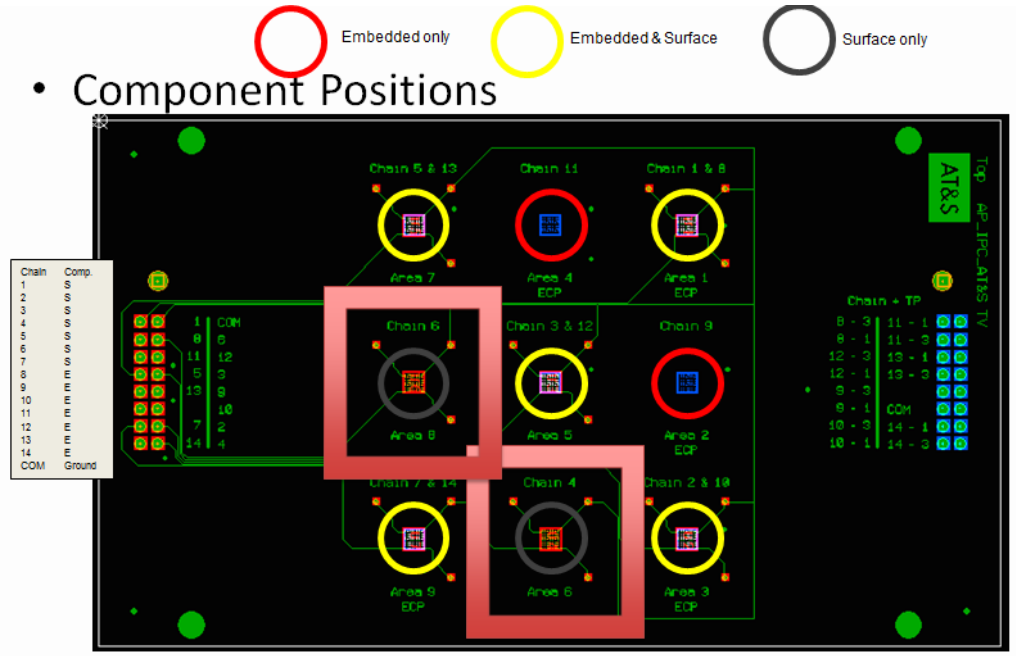


Figure 13 – TCT Failure Location description

TCT Test Failure Modes:
An event is registered as a failure after demonstrating a resistance change of >1,000 Ohm. In all constellations (SMD and EC) the test vehicle failed 1000 cycles on the SMD part. In all 10 test vehicles we detected failures on Location 4 and 6 (SMD only, see figure 12). TCT failure locations have been marked with a light red frame in figure 13. The results themselves as shown in figure 14 reveal the SMD failure mode being solder cracks, similar to the drop test failure mode.

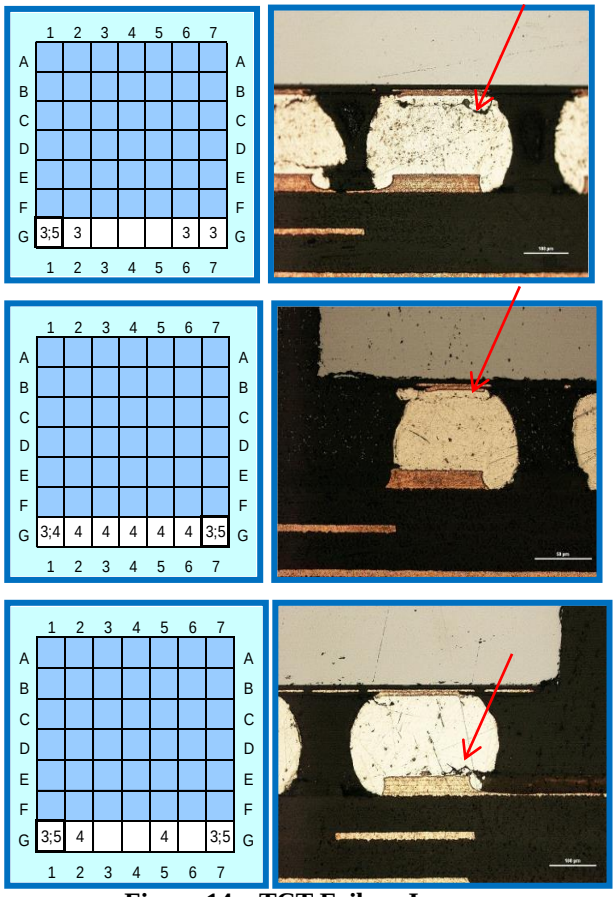


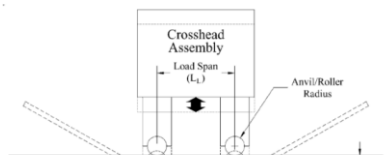
Figure 14 – TCT Failure Images

Bend Test:

The bend test specification was based on the JEDEC 9702 (see table 4). The test vehicle ITE2000EC was soldered at the test terminal PTHs. Test events were monitored online as opposed to post testing and verification (figure 15).

Table 4 – Bend Test specifications

Bend Testing	
Company Spec	**TI.GR.PH-LAB-51EG**
IPC	**IPC/JEDEC-9702**
Loading Rate	**2mm/min**
Test structures	**Assembled cards**
Load Span	**28mm**
Support Span	**65.5mm**
Pass/ Fail – Criteria	**Assembled cards: resistance increase for Ro while applying strain and force**



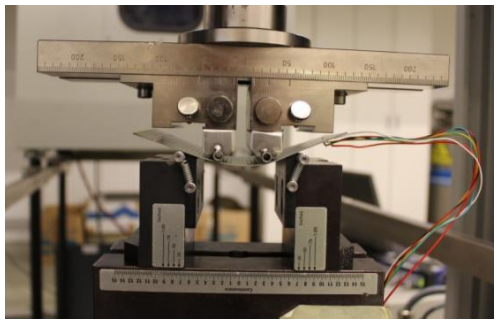


Figure 15 – Bend Test Set up

The test vehicle was not prepared in any other relevant manner beyond the soldering of the test terminals to the event recording wire bundle. Nine cards were tested according to the above mentioned test specifications (table 4). The cards were bent until a resistance change was registered (an "event"). Once verified, the location of the exact component (SMD or EC) was determined using the terminal PTHs and the test pads. Once the component had been identified, cross section analysis was carried out to determine the failure mode.

Bend Test Results

Bend testing yielded the following results, which are also depicted in table 5. One out of nine test vehicles revealed a SMD related defect. The earliest resistance change was recorded after 3.71 sec. Table 5 provides an overview of the bend test results. Figure 16 displays the positions of the component daisy chains and highlights the failure areas per chain: red depicts embedded only, yellow embedded and SMD and dark grey SMD only. Light red frames indicate the failed daisy chain location (figure 16). Chain 4 (only SMD) indicated a slight solder crack during analysis as shown in figure 17.

Table 5 – Bend Test Set up

Specimen	1	2	3	4	5	6	7	8	9
Channel 1	1	1	1	1	1	1	1	1	1
Channel 2	1	1	1	1	1	1	1	1	1
Channel 3	1	1	1	1	1	1	1	1	1
Channel 4	1	1	3.71	1	1	1	1	1	1

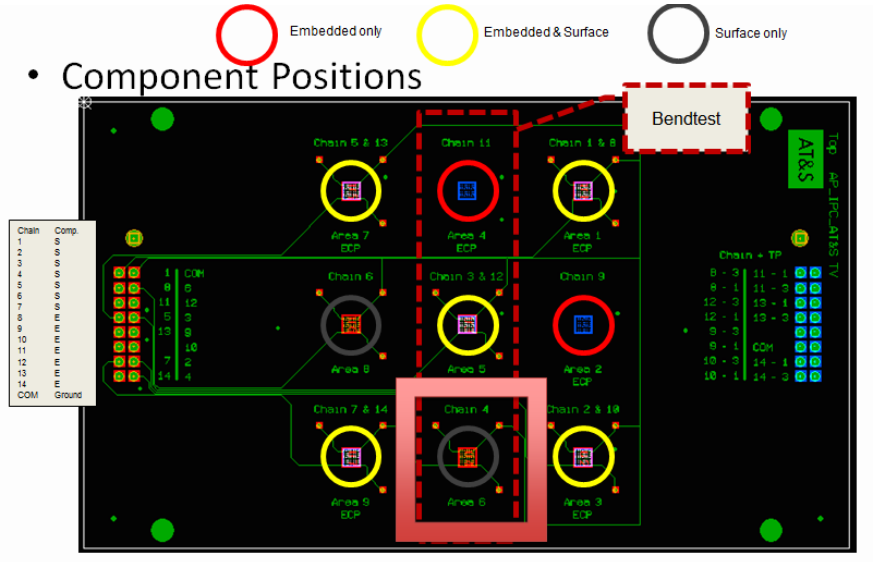


Figure 16 – Failure Location and Bend test overview

Bend Test Failure Modes:

Analysis performed on this one failed card revealed a SMT failure which was a solder crack near the component side of the solder joint The solder crack occurred on the upper area of the solder ball close to the component side of the solder joint: first row second pad (figure 17).

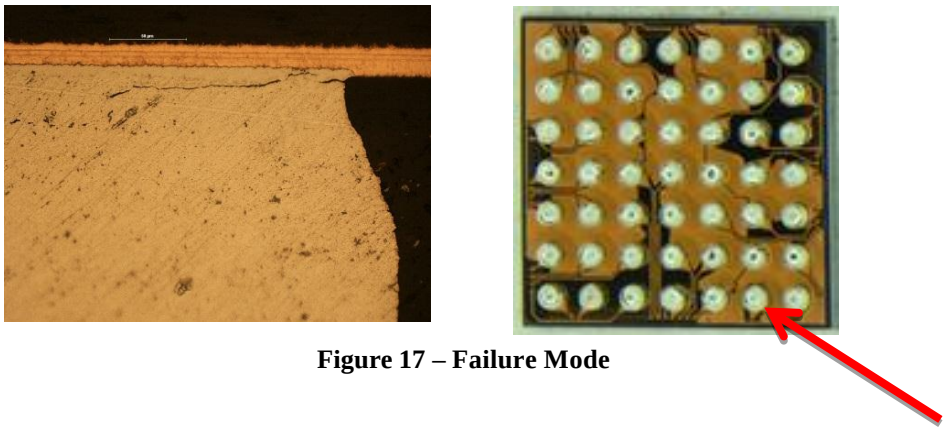


Figure 17 – Failure Mode

Evaluation

Many efforts were made in this experiment to base the board design, test methods and components on existing standards to achieve increased objectivity and comparability. In parallel the idea was to keep the board and test method as close to the initial Part I design as possible. This allows us a direct comparison of passive versus active results. Considering the aim to identifying general performance variations in reliability between the traditional SMT and embedded components (manufactured in such a form as described here), the test vehicle design and test methodology proved effective. Certainly improvements to board and test design must and will be considered in further steps.

The overall test results were in line with our expectations, considering the mechanics of the tests itself and the location of the embedded component within the PCB. In PCB level drop testing there is no impact on a hard surface (as with some device level drop testing), rather the board is suspended on the four corners and accelerated towards a halting point. This being considered it is clear why the SMD daisy chains) could have demonstrated the lowest performance. When the board reaches the nadir of its fall in the test device, the four suspended corners remain fixed and the board center exhibits a downward expansion. The position of the SMD chain is at the most extreme curvature of this tension. In other words, the outermost point during the mechanical stress (where the SMD chain is found) is farthest from the neutral axis, whereas the ECs remain closer to this axis (figure 18).The risk for SMD components as seen in this paper is related to solder joints being stressed much higher, while a copper plated laser connection on the EC part remains low risk.

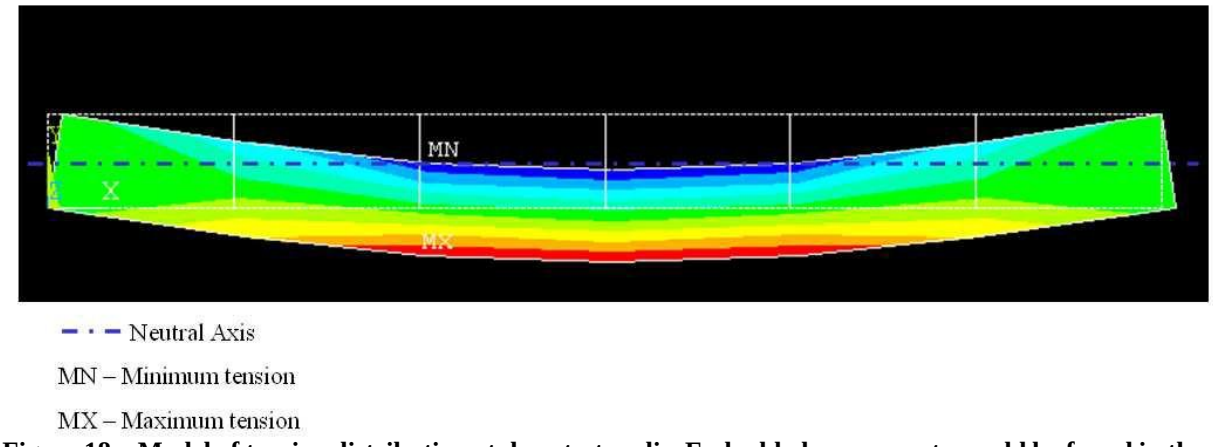


Figure 18 – Model of tension distribution at drop test nadir. Embedded components would be found in the area indicated with green.

The solder crack noted in the drop test results section of this paper are also likely a product of similar stresses. A drop test with actual surface impact, of course, may reveal varying results in regards to component breakage, but it remains clear that the component deviation to the neutral axis in not advantageous when the rigid PCB is subjected to planar modifications.

The root cause for the failure at 792 drops being solder crack indicates that a component placement close to the neutral axis is of advantage. Thus the embedded components in this experiment provided clear superiority in terms of reliability under board level drop testing conditions.

It could be extrapolated that the usage of such components may provide certain advantages to SMDs given a PCBAs or

device’s exposure to similar environments as those simulated in the drop test.

Regarding the results of the TCT testing, as a final statement the SMDs solder connection proved to be the weakest part and therefore be the number one cause for failures. This statement may be further drawn out to conclude the compatibility of both components towards one another in the same PCB construction; i.e. ECs are for this particular test result detrimental to the success of SMDs during testing. This however cannot be a general statement and needs to be investigated further.

As the TCT test is mainly used to test reliability during thermal fluctuations (automotive, aerospace, industry, etc.), the CTE match of material and components is certainly a criterion for the successful withstanding of the test. The larger the component is and the larger the number of interconnects between component and PCB, the more influence the CTE is as well as the SMT process of the individual constituents. As the active component has forty-nine interconnect terminals (compared to the passives with only two), one may expect more component relevant failures in general. Someone might argue that certain design elements and surface finishes might influence the result. For this paper we used OSP as the surface finish in combination with solder mask defined pads.

Bend test results confirmed the Drop test and TCT analysis. Adding one additional mechanical stress factor to balance and potentially question the two initial methods, proved to be a viable addition.

To summarize, there were visible reliability advantages for embedded components under the production and testing methods described. These advantages, at least with these components and array, are mainly found in the reduction of deviation to a rigid board’s neutral axis. In terms of thermal reliability we did see clear advantages for ECs versus SMD.

References

1. Christopher Michael Ryder, A comparative analysis_of_reliability, IPC APEX Conference, 2011.