The Effect of Reflow Profiling on the Electrical Reliability of No-Clean Solder Paste Flux Residues

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Abstract

An estimated 80% of all SMT assembly in the world is performed with a no-clean soldering process, largely due to the predominance of consumer-type electronics. The continuing trend of increasing miniaturization that dominates modern electronics devices requires no-clean flux residues to be as benign and electrically resistive as possible. Solder pastes with a IPC J-STD-004 [1] classification of ROL0 or ROL1 rely heavily on two basic mechanisms to render the flux residue as "no-clean": (1) the encapsulating properties that the rosin provides and (2) the heat activation/decomposition of the chemicals in the flux, commonly known as "activators." The latter is generally known in the industry, but is rarely taken into consideration for reflow profiling in SMT assembly. Optimization of a reflow profile often focuses on mitigating defects such as voiding, tombstoning, graping, slumping/bridging, etc. However, little thought is given to the reflow profile's effect on the electrical reliability of the no-clean flux residue. Because of the wide variation in size and thermal density of SMT components and PCBs, achieving a reflow profile that equally heats the entire assembly can be challenging and often impossible. The temperature under a large component, such as a BGA, is often markedly cooler than a smaller component, such as a passive resistor or capacitor. This paper will discuss an experiment that studied the effect of reflow profiling on the electrical reliability of no-clean flux residues that can be measured using IPC J-STD-004[1] surface insulation resistance (SIR) testing. Both a halogen-free (ROL0) and a halogen-containing (ROL1) Pb-free no-clean solder paste, exposed to various reflow profiles, were used in this study.

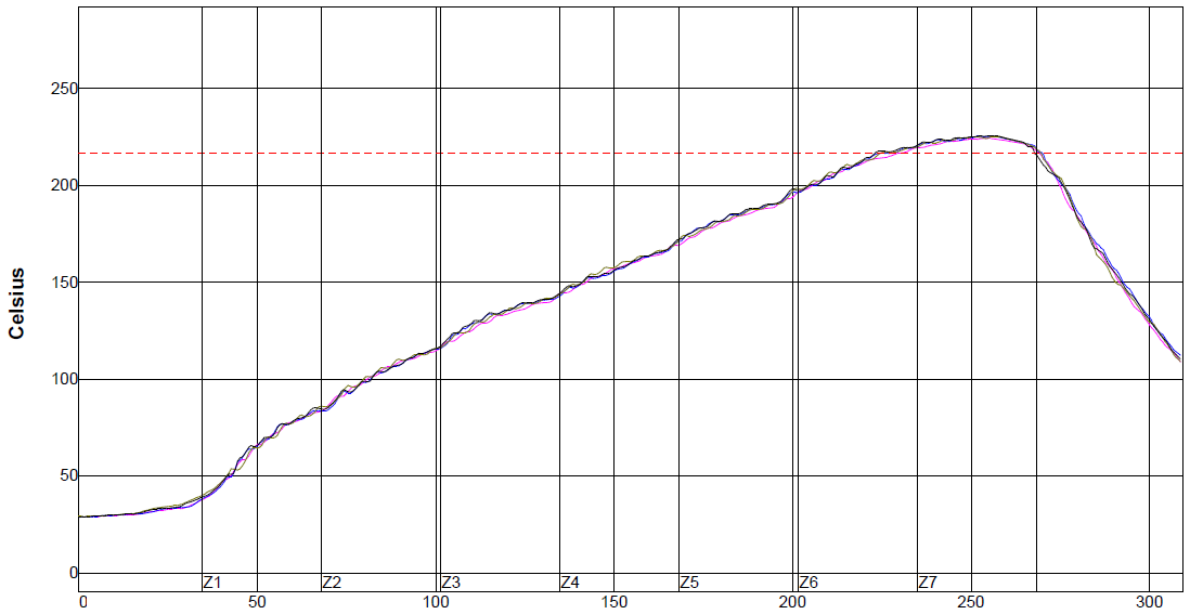
Introduction

Prior work had exposed the impact on SIR values of entrapping a solder paste flux residue under a component body or RF shield. What was unclear in that work, is the impact of the reflow profile. Invariably, flux underneath a device does not get exposed to the same heat that an exposed flux does. So, performing an experiment that focused solely on the effect of heating seemed pertinent.

Experimental

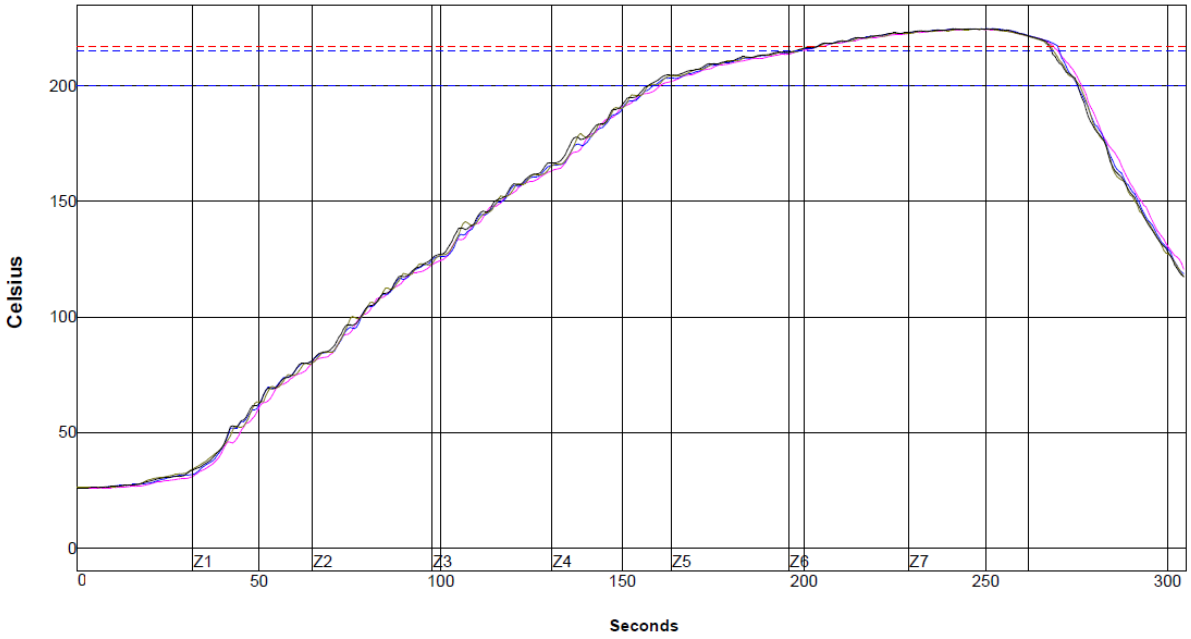
In this experiment, a total of 8 reflow profiles were used for each solder paste; one paste being ROL0 and the other being ROL1. Both solder pastes used are standard commercially available products. All boards were reflowed in a standard convection belt furnace type reflow oven with an air environment. The reflow profiles consisted of 4 different peak temperatures: 225°C, 235°C, 245°C and 255°C. For each peak temperature, reflow profiles representing a "ramp to peak" and "soak" profile were created. (Figures 2 through 9.) The purpose of creating both a ramp to peak and a soak profile was to see if and how, not only the peak temperature, but also the "shape" of the profile, has an impact on SIR performance. For the sake of this work, the "soak" is defined as the period during which the PCB is between 200°C and 215°C. Figure 1 shows the SIR (IPC-B-24) test coupon used for profiling and the location of the thermocouples. All SIR board preparation, materials and processes were in accordance with IPC-TM-650 2.6.3.3 and 2.6.3.7
Table 1 shows a compilation of the averaged parameters for each reflow profile scenario.

Figure 1 - IPC-B-24 SIR Test Coupon with Thermocouples Attached



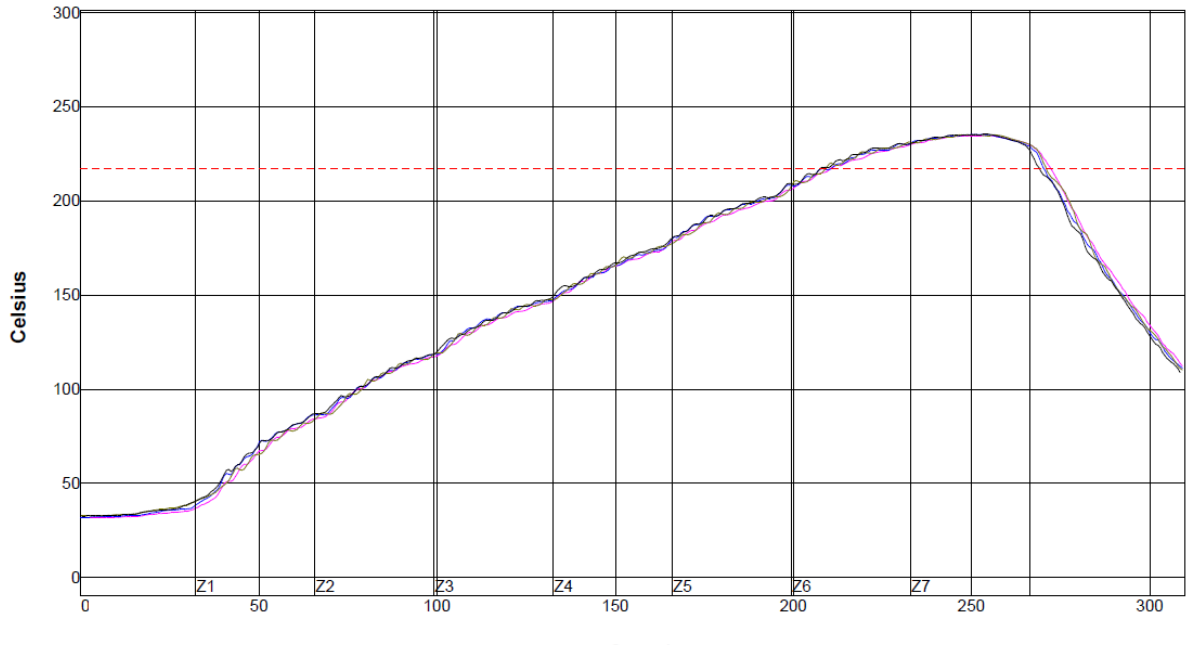
PWI= 78%	Max Rising Slope		Reflow Time /217C		Peak Temp		Slope1 (25-217C)	
2	1.72	-56%	37.69	-74%	224.44	-78%	1.03	-31%
3	1.83	-34%	40.63	-65%	225.50	-72%	1.02	-32%
4	1.69	-62%	44.60	-51%	225.39	-73%	1.02	-32%
5	1.79	-41%	44.54	-52%	225.73	-71%	1.01	-33%
Delta	0.14		6.91		1.29		0.02	

Figure 2 – 225°C Ramp to Peak Reflow Profile



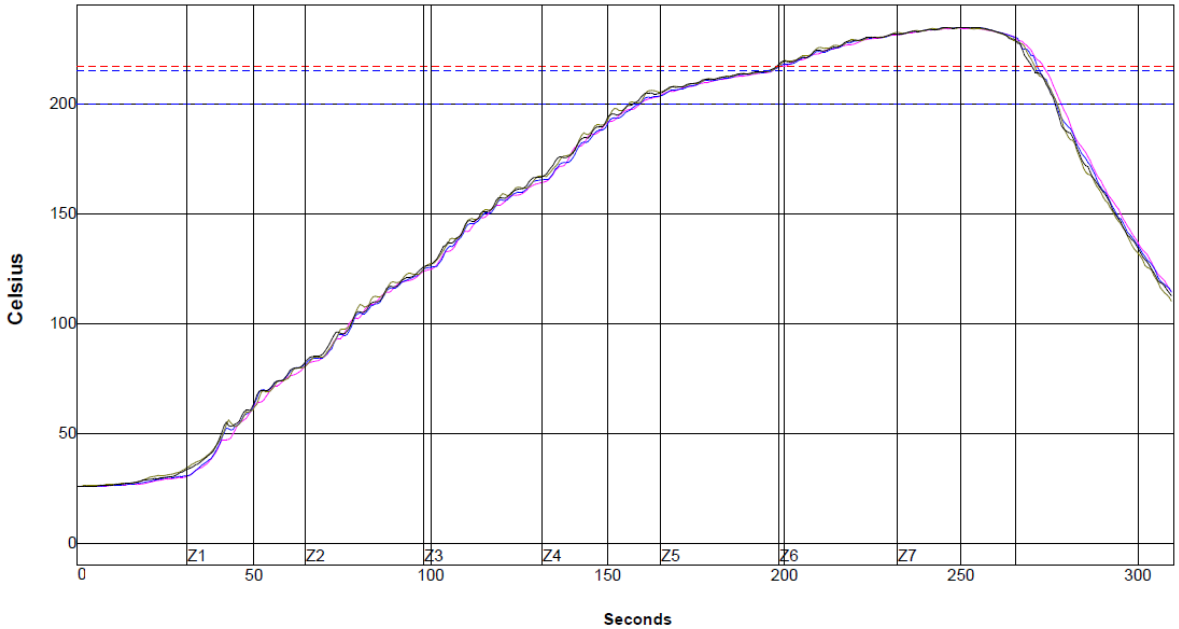
PWI= 83%	Max Rising Slope		Soak Time 200-215C		Reflow Time /217C		Peak Temp		Slope1 (30-217C)	
<TC2>	1.79	19%	37.79	-83%	65.05	17%	224.61	-65%	1.35	35%
<TC3>	1.87	25%	39.42	-79%	66.38	21%	224.83	-64%	1.35	35%
<TC4>	1.72	14%	41.43	-75%	64.79	16%	224.62	-65%	1.34	34%
<TC5>	1.75	17%	40.09	-78%	64.00	13%	224.78	-64%	1.35	35%
Delta	0.15		3.64		2.38		0.22		0.01	

Figure 3 – 225°C Soak Reflow Profile



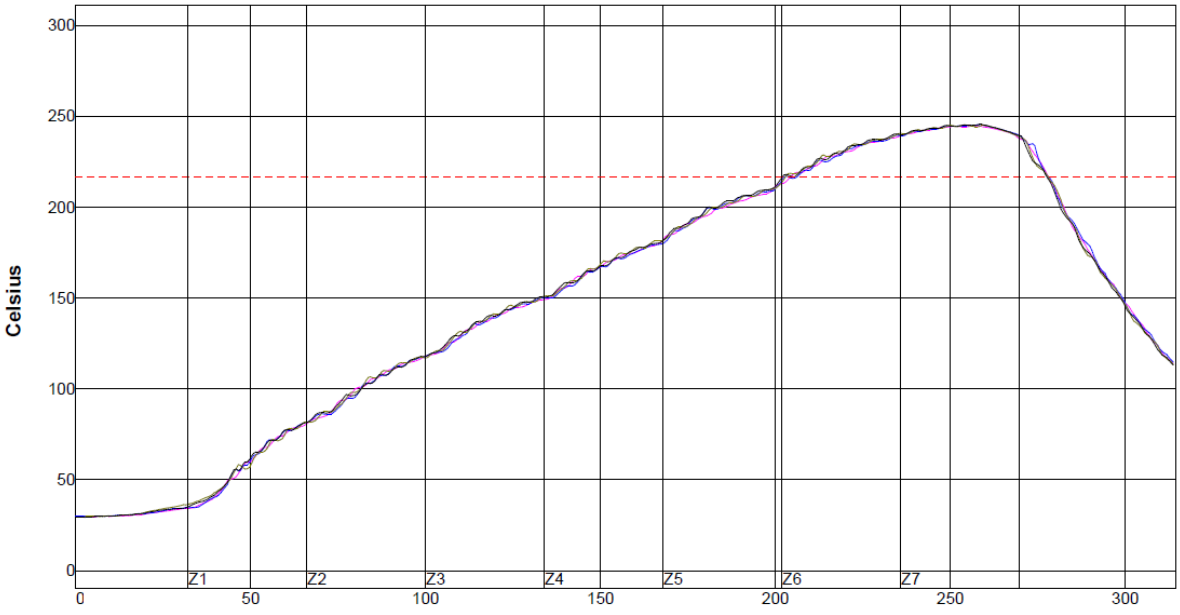
PWI= 66%	Max Rising Slope		Reflow Time /217C		Peak Temp		Slope1 (25-217C)	
2	1.76	-48%	62.06	7%	234.84	-26%	1.09	-28%
3	1.81	-38%	60.84	3%	235.44	-23%	1.08	-28%
4	1.67	-66%	62.09	7%	235.28	-24%	1.08	-28%
5	1.69	-61%	61.81	6%	235.61	-22%	1.07	-29%
Delta	0.14		1.25		0.77		0.02	

Figure 4 – 235°C Ramp to Peak Reflow Profile



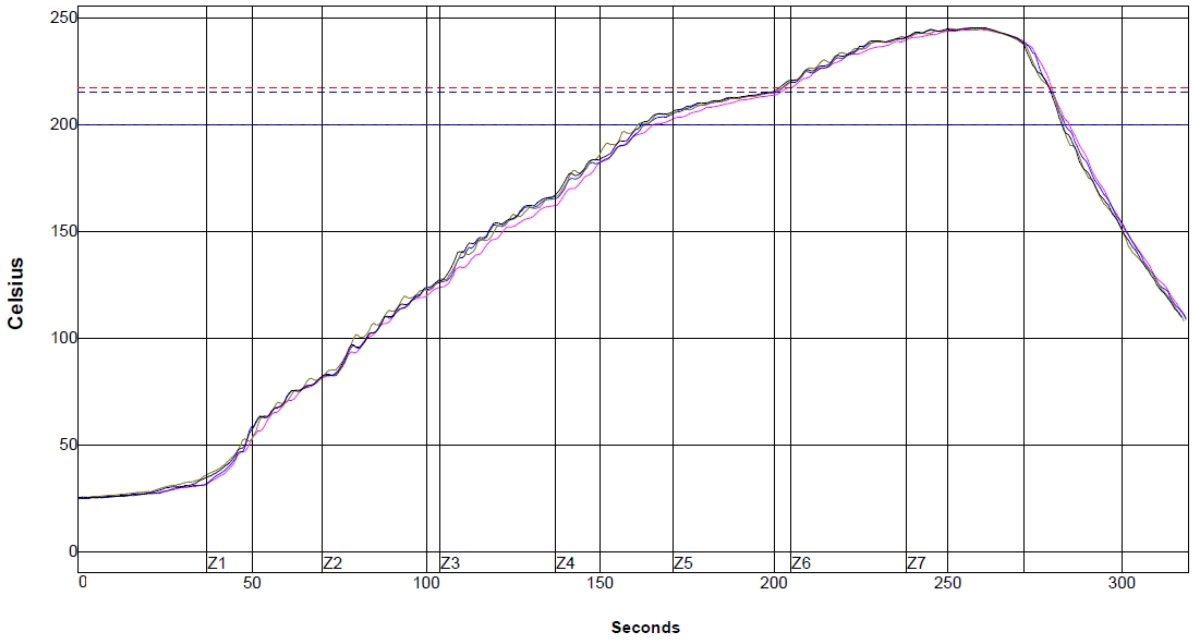
PWI= 84%	Max Rising Slope		Soak Time 200-215C		Reflow Time /217C		Peak Temp		Slope1 (30-217C)	
<TC2>	1.83	22%	37.50	-83%	74.41	48%	234.62	-18%	1.35	35%
<TC3>	1.95	30%	37.41	-84%	73.03	43%	234.93	-17%	1.36	36%
<TC4>	1.72	15%	40.01	-78%	72.77	43%	234.84	-17%	1.36	36%
<TC5>	1.77	18%	37.92	-82%	72.37	41%	234.88	-17%	1.35	35%
Delta	0.23		2.60		2.04		0.31		0.01	

Figure 5 – 235°C Soak Reflow Profile



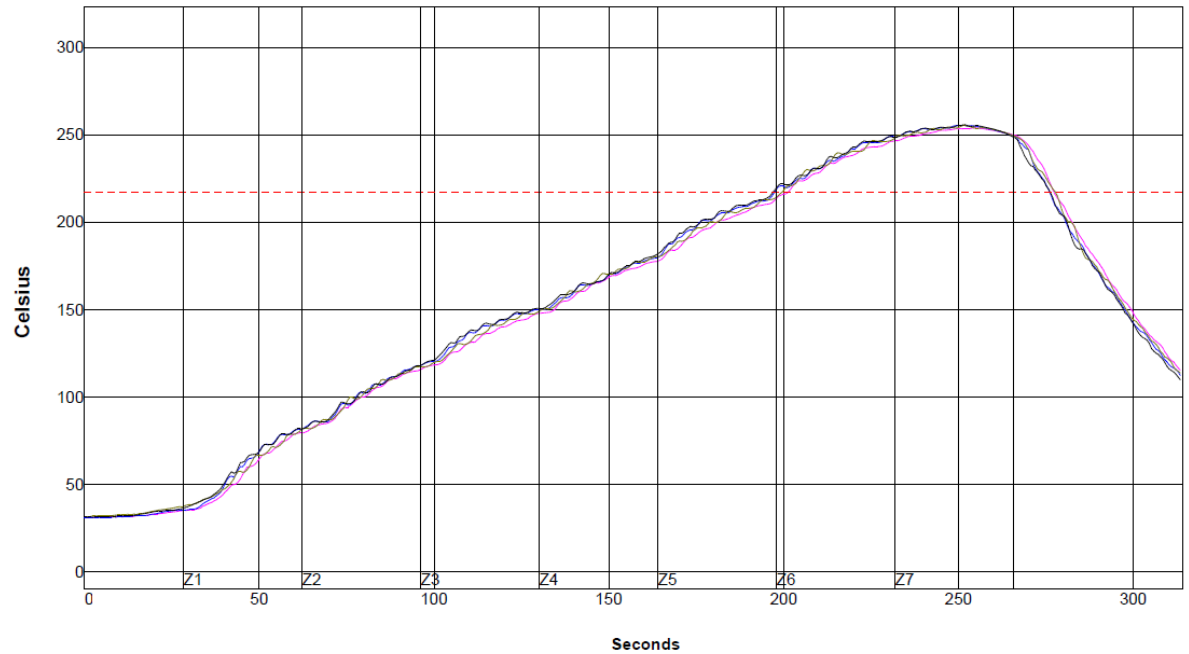
PWI= 61%	Max Rising Slope		Reflow Time /217C		Peak Temp		Slope1 (25-217C)	
2	1.78	-44%	73.58	45%	244.89	24%	1.14	-24%
3	1.84	-31%	72.20	41%	245.55	28%	1.14	-24%
4	1.70	-61%	74.93	50%	245.40	27%	1.13	-24%
5	1.78	-44%	74.46	48%	245.56	28%	1.13	-25%
Delta	0.14		2.73		0.67		0.01	

Figure 6 – 245°C Ramp to Peak Reflow Profile



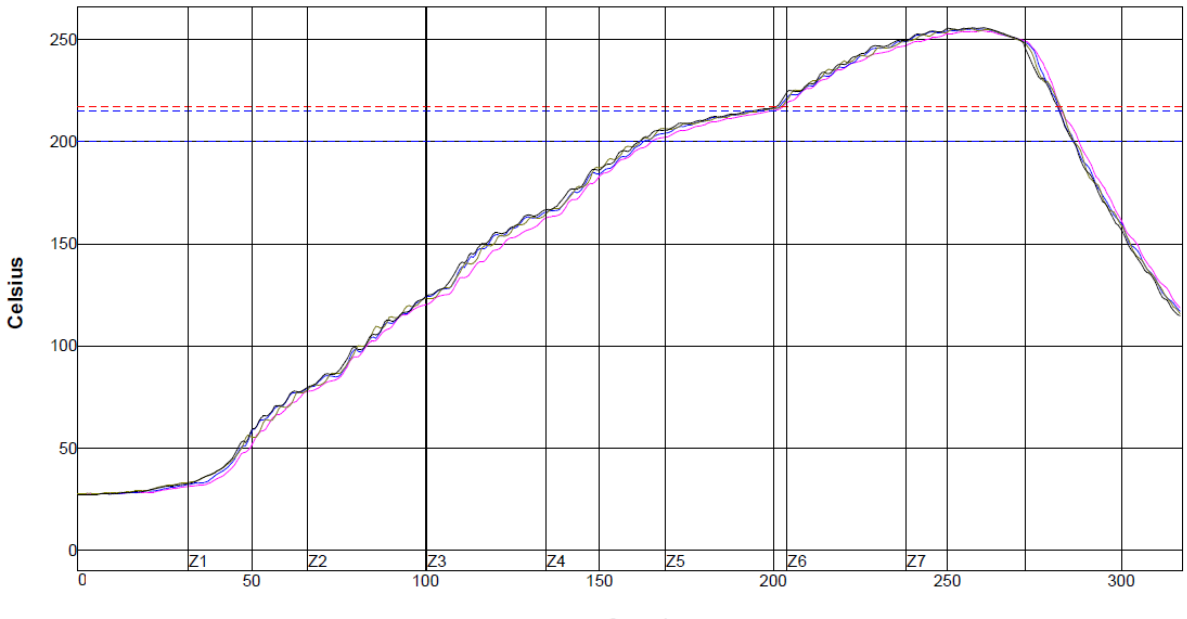
PWI= 86%	Max Rising Slope		Soak Time 200-215C		Reflow Time /217C		Peak Temp		Slope1 (30-217C)	
<TC2>	1.78	19%	36.27	-86%	76.05	53%	244.49	28%	1.33	33%
<TC3>	1.91	27%	36.77	-85%	76.79	56%	245.22	31%	1.34	34%
<TC4>	1.74	16%	39.64	-79%	76.68	56%	245.06	31%	1.34	34%
<TC5>	1.83	22%	36.95	-85%	77.67	59%	245.28	32%	1.34	34%
Delta	0.17		3.37		1.62		0.79		0.01	

Figure 7 – 245°C Soak Reflow Profile



PWI= 79%	Max Rising Slope		Reflow Time /217C		Peak Temp		Slope1 (25-217C)	
2	1.73	-53%	76.22	54%	254.02	70%	1.12	-25%
3	1.86	-28%	78.86	63%	255.48	77%	1.12	-25%
4	1.67	-66%	78.44	61%	255.40	77%	1.11	-26%
5	1.79	-43%	79.33	64%	255.81	79%	1.11	-26%
Delta	0.19		3.11		1.79		0.01	

Figure 8 – 255°C Ramp to Peak Reflow Profile



PWI= 97%	Max Rising Slope		Soak Time 200-215C		Reflow Time /217C		Peak Temp		Slope1 (30-217C)	
<TC2>	1.80	20%	34.02	-91%	79.62	65%	254.28	73%	1.33	33%
<TC3>	1.91	28%	33.37	-93%	80.16	67%	255.33	78%	1.33	33%
<TC4>	1.74	16%	34.60	-90%	80.41	68%	255.59	79%	1.34	34%
<TC5>	1.85	23%	31.13	-97%	81.14	70%	255.84	81%	1.33	33%
Delta	0.17		3.47		1.52		1.56		0.01	

Figure 9 – 255°C Soak Reflow Profile

Table 1 – Compiled Reflow Profile Parameters

Peak Temperature	Profile Type	Ramp Rate	Soak Time (200 - 215C)	Time above 217C
225C	Ramp to Peak	1.02C/s	N/A	41.9s
225C	Soak	1.35C/s	39.7s	65.1s
235C	Ramp to Peak	1.08C/s	N/A	61.7s
235C	Soak	1.36C/s	38.2s	73.1s
245C	Ramp to Peak	1.14C/s	N/A	73.8s
245C	Soak	1.34C/s	37.4s	76.8s
255C	Ramp to Peak	1.12C/s	N/A	78.2s
255C	Soak	1.33C/s	33.3s	80.3s

As mentioned at the beginning of this paper, two no-clean solder pastes were tested with these various reflow profiles. Both were Pb-free, containing SAC305 as the alloy. One was halogen-containing and the other was halogen-free. The purpose of the 2 different chemistries was to see if halogen-containing and halogen-free solder pastes responded differently to the reflow profiles in terms of their SIR performance. A total of 2 SIR test coupons were prepared and tested for each solder paste/reflow profile scenario. (Table 2.) Because the SIR chamber had a limited capacity of 20 boards per test, the boards were tested in two groups. The results of the SIR testing are shown in the following section.

Table 2 – Solder Paste/Reflow Profile Matrix

Solder Paste	Peak Temp	Profile Type	Boards	Run
Halogen Containing	225	Ramp	2	1
		Soak	2	1
	235	Ramp	2	1
		Soak	2	1
	245	Ramp	2	2
		Soak	2	2
	255	Ramp	2	2
		Soak	2	2
Halogen Free	225	Ramp	2	1
		Soak	2	1
	235	Ramp	2	1
		Soak	2	1
	245	Ramp	2	2
		Soak	2	2
	255	Ramp	2	2
		Soak	2	2
Controls			4	1, 2
Total			36	

Results and Discussion

Figures 10 through 26 show the SIR results obtained from each scenario mentioned in the experimental section. A discussion of the SIR results can be found beginning after Figure 26.

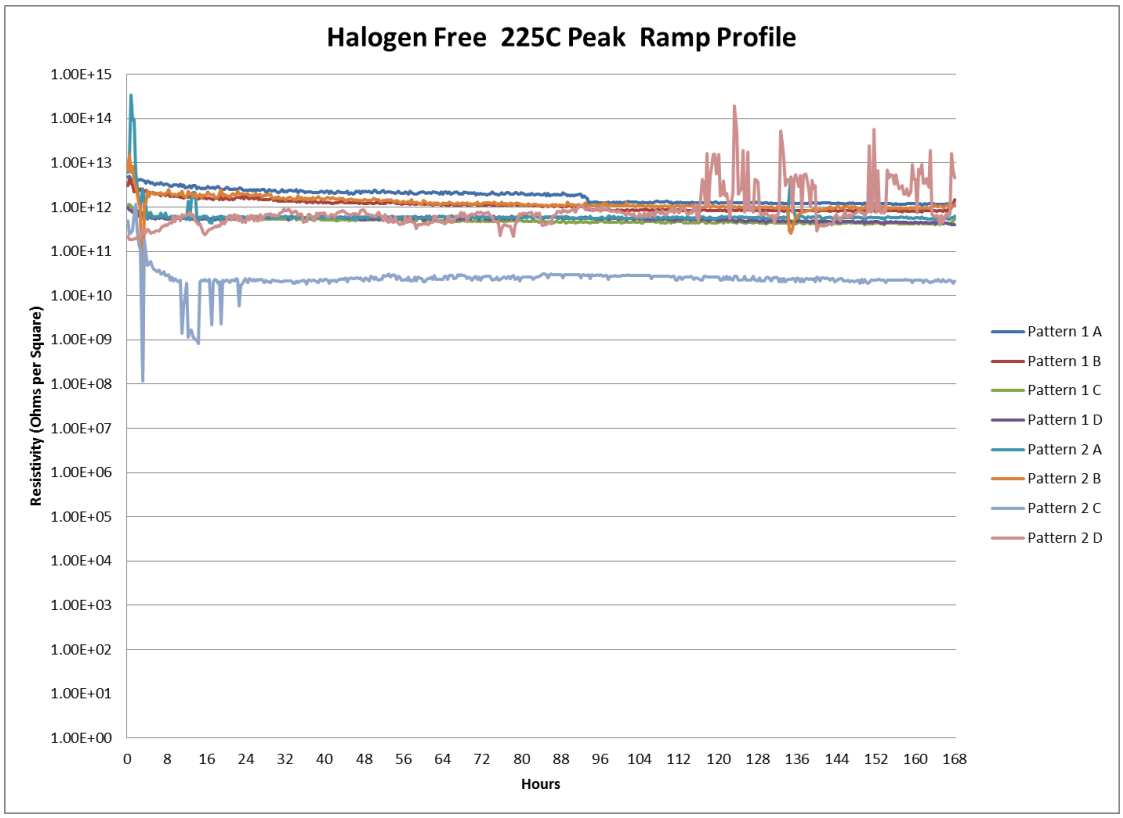


Figure 10 – Halogen-Free Solder Paste, 225°C Peak Temperature Ramp Profile (Run 1)

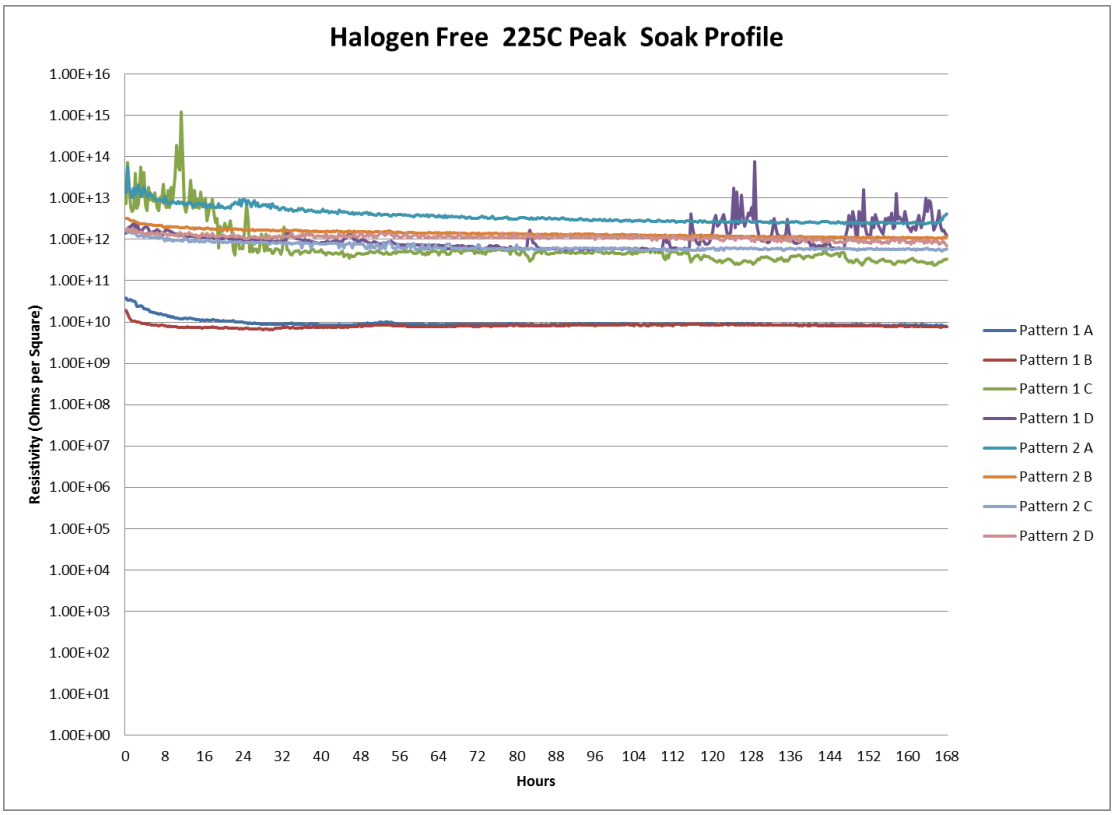


Figure 11 – Halogen Free Solder Paste, 225°C Peak Temperature Soak Profile (Run 1)

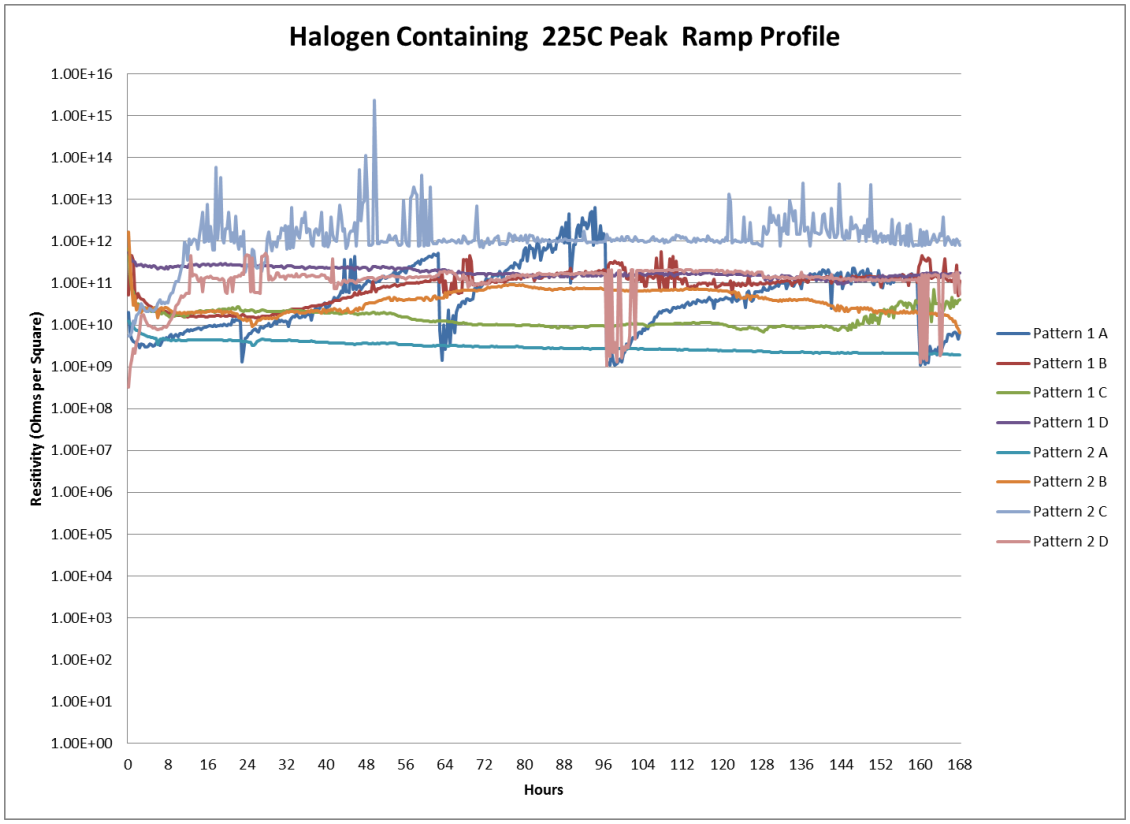


Figure 12 – Halogen-Containing Solder Paste, 225°C Peak Temperature Ramp Profile (Run 1)

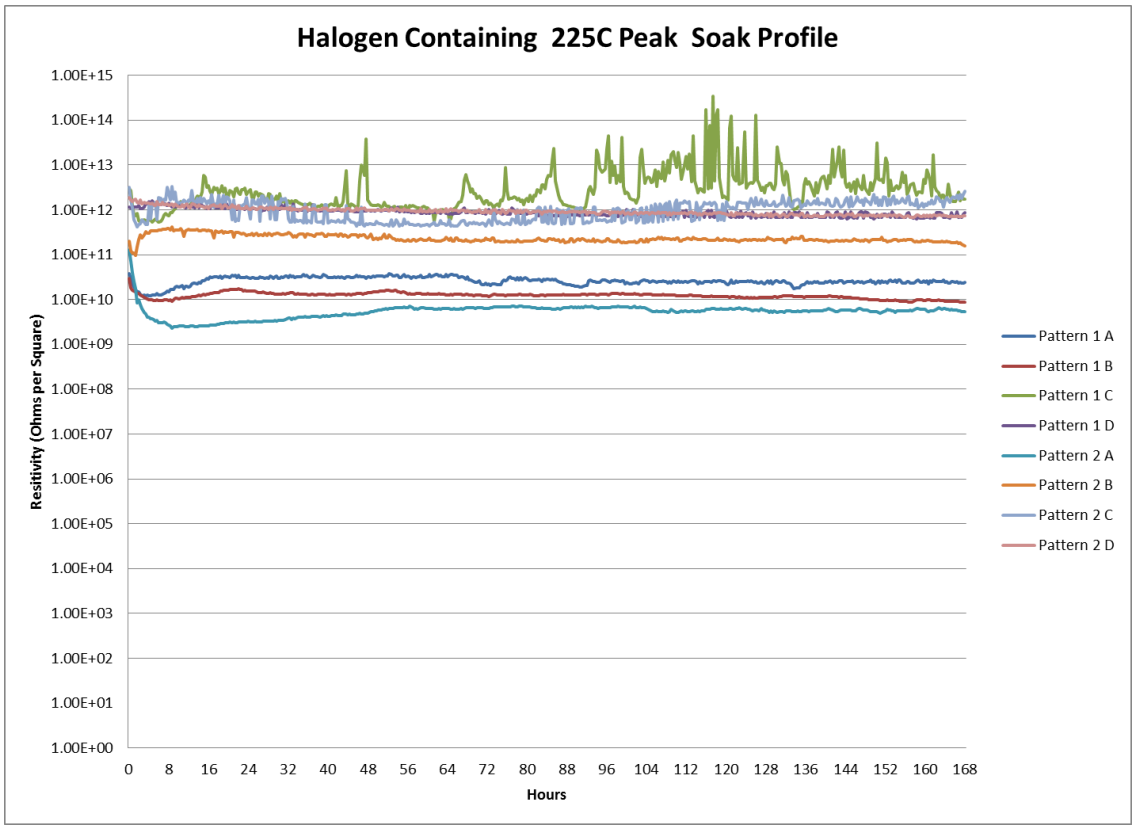


Figure 13 – Halogen-Containing Solder Paste, 225°C Peak Temperature Soak Profile (Run 1)

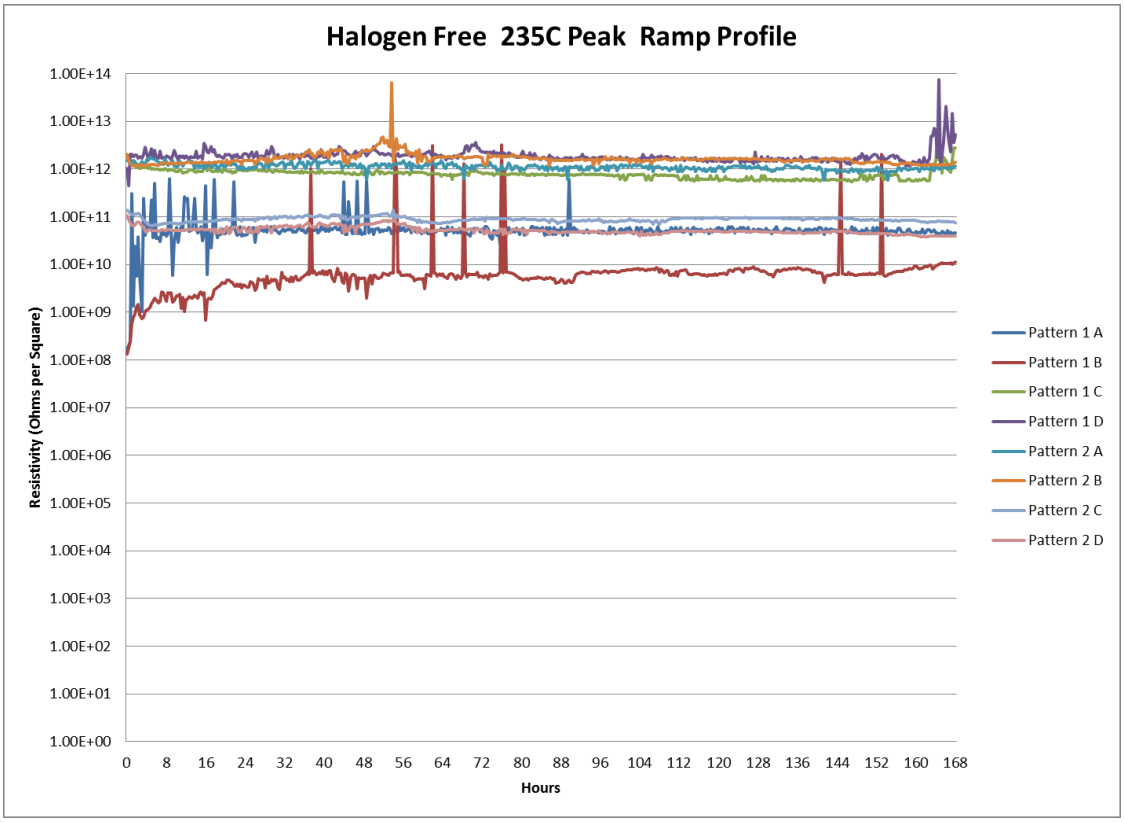


Figure 14 – Halogen-Free Solder Paste, 235°C Peak Temperature Ramp Profile (Run 1)

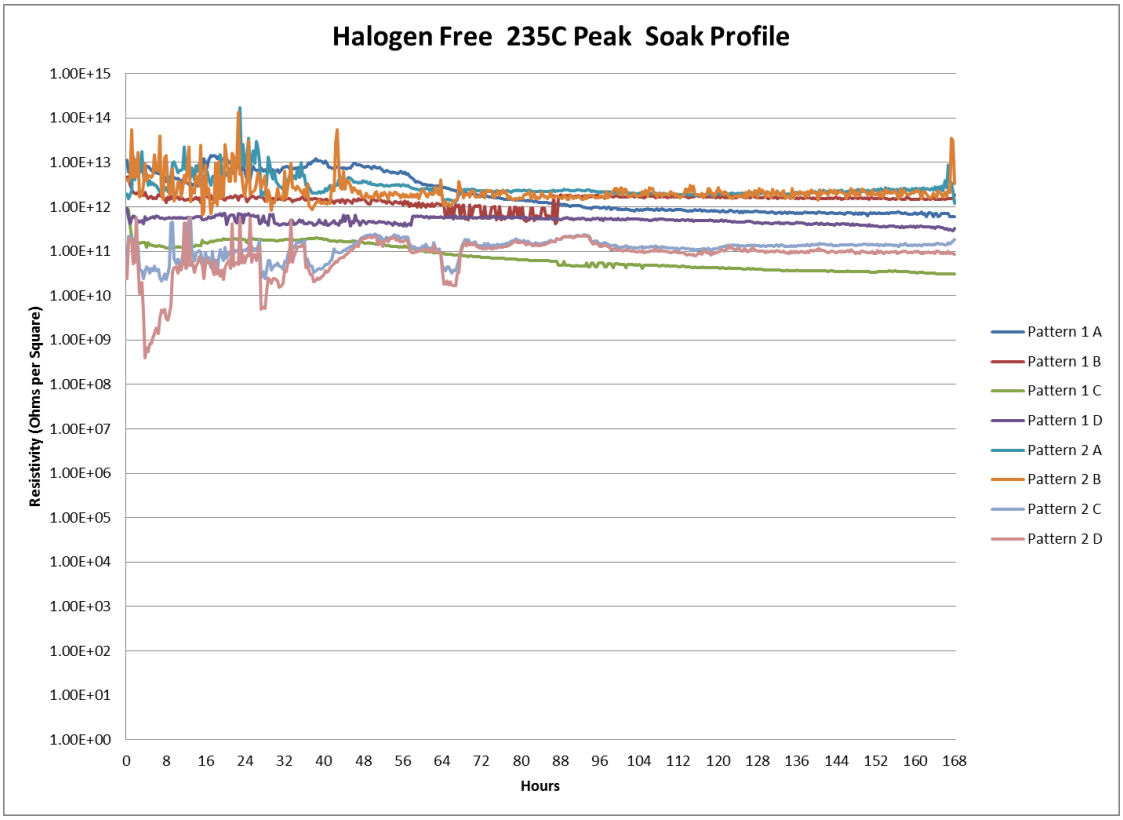


Figure 15 – Halogen-Free Solder Paste, 235°C Peak Temperature Soak Profile (Run 1)

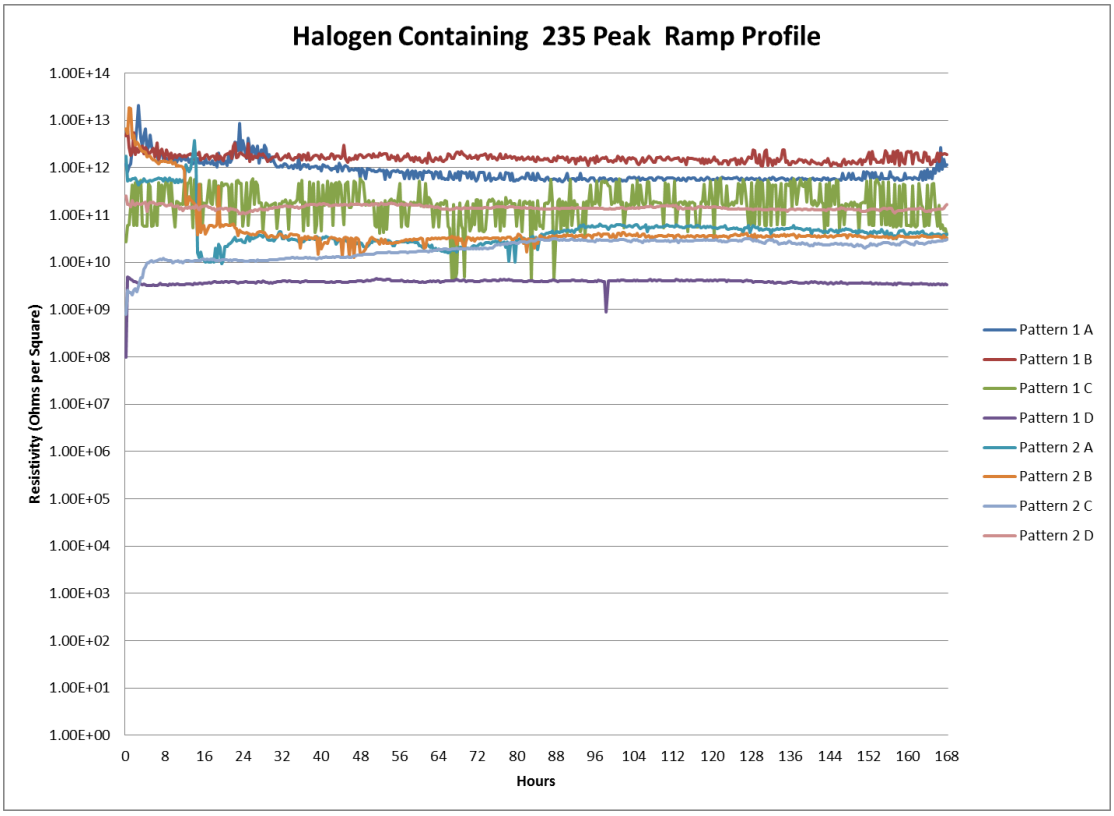


Figure 16 – Halogen-Containing Solder Paste, 235°C Peak Temperature Ramp Profile (Run 1)

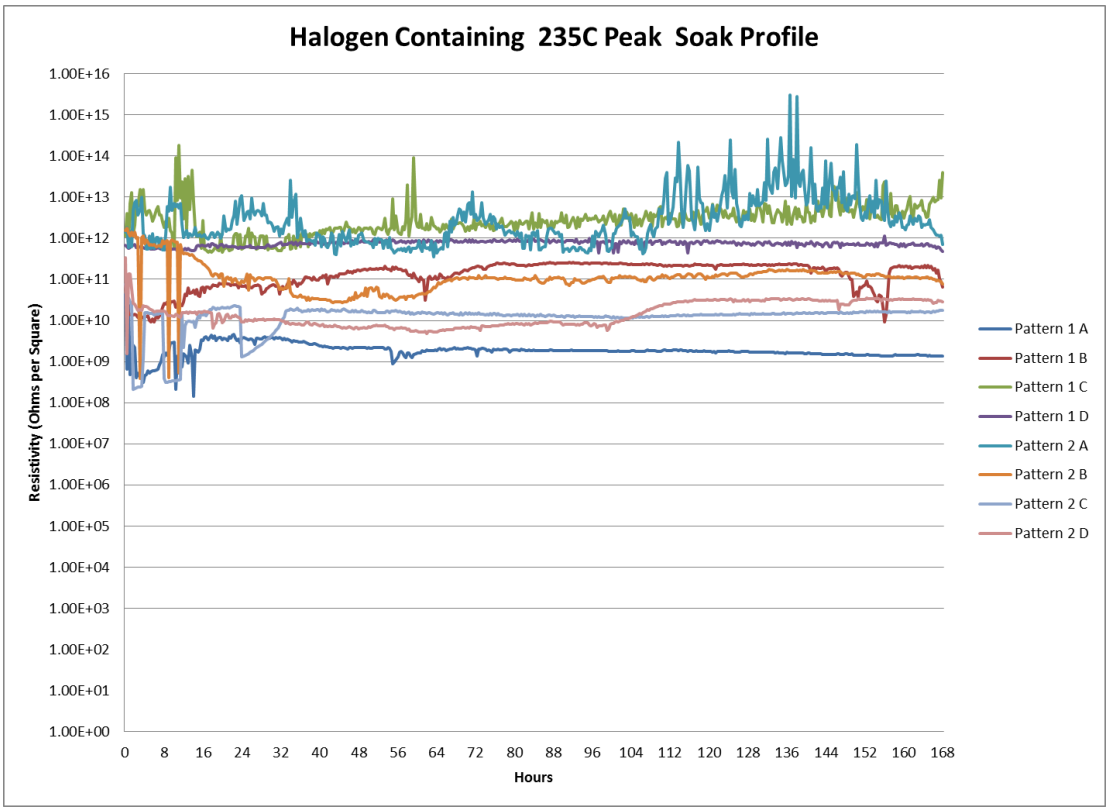


Figure 17 – Halogen-Containing Solder Paste, 235°C Peak Temperature Soak Profile (Run 1)

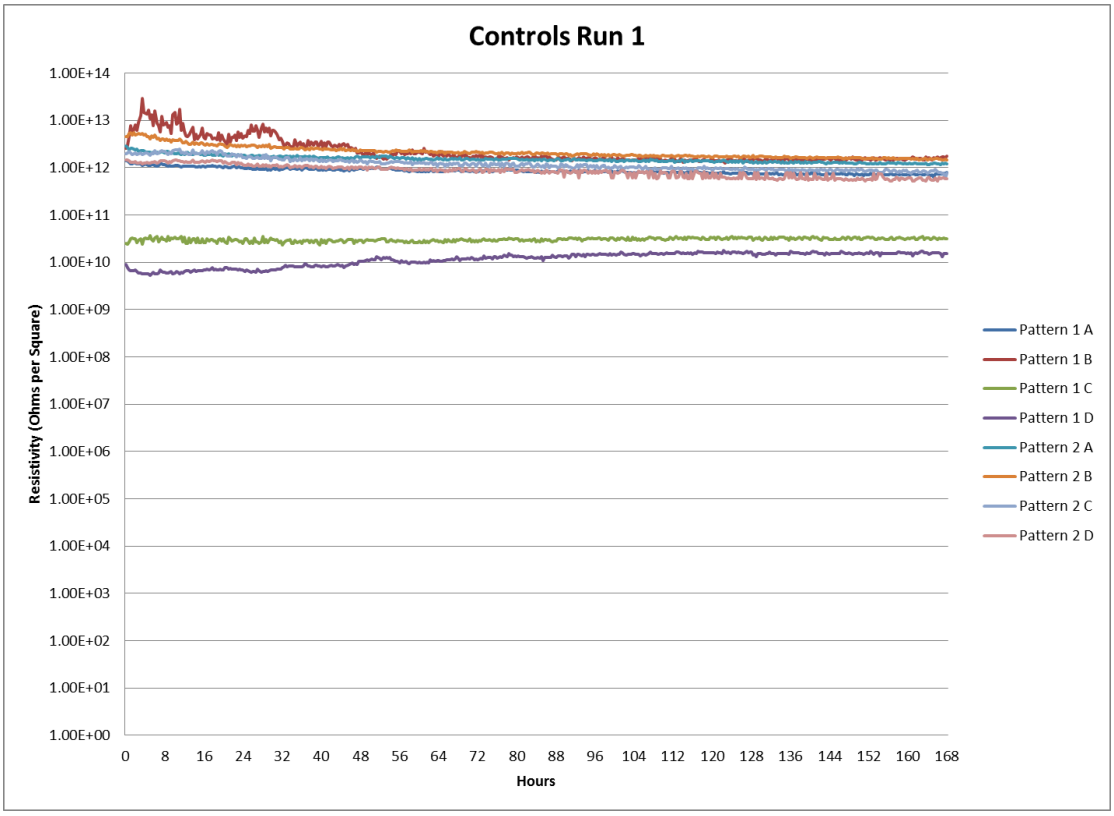


Figure 18 – Controls (Run 1)

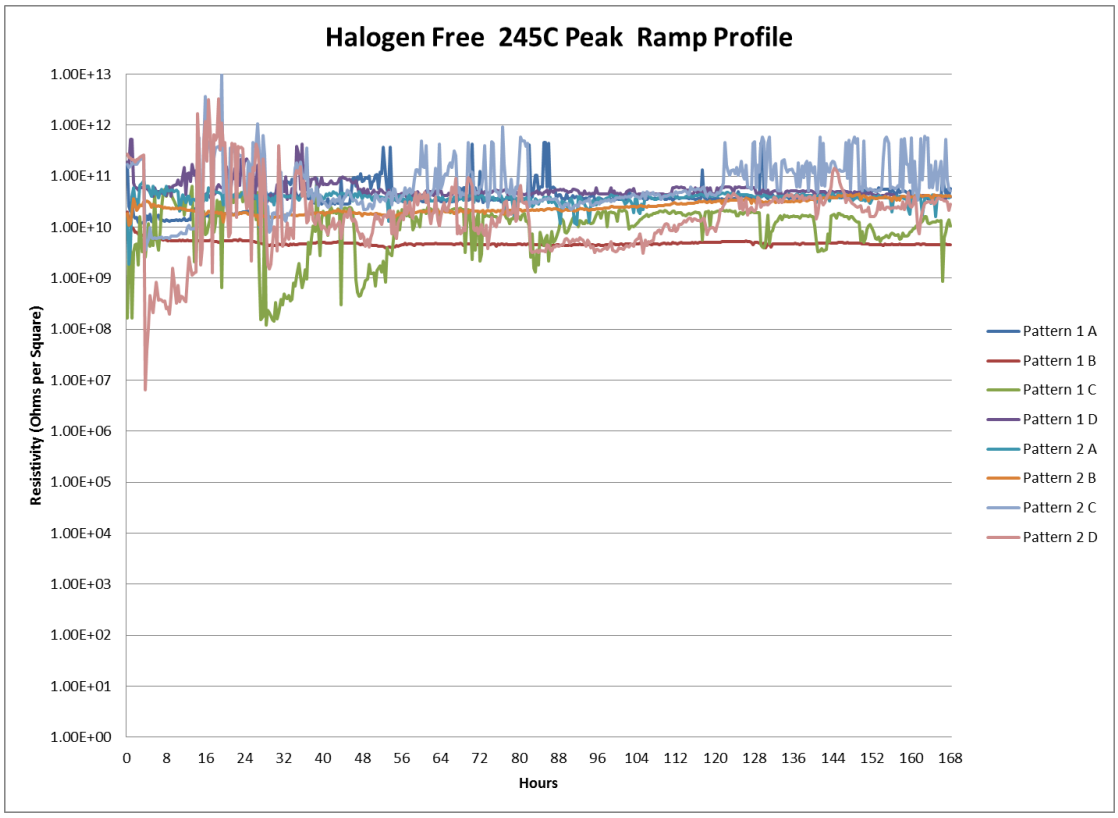


Figure 19 – Halogen-Free Solder Paste, 245°C Peak Temperature Ramp Profile (Run 2)

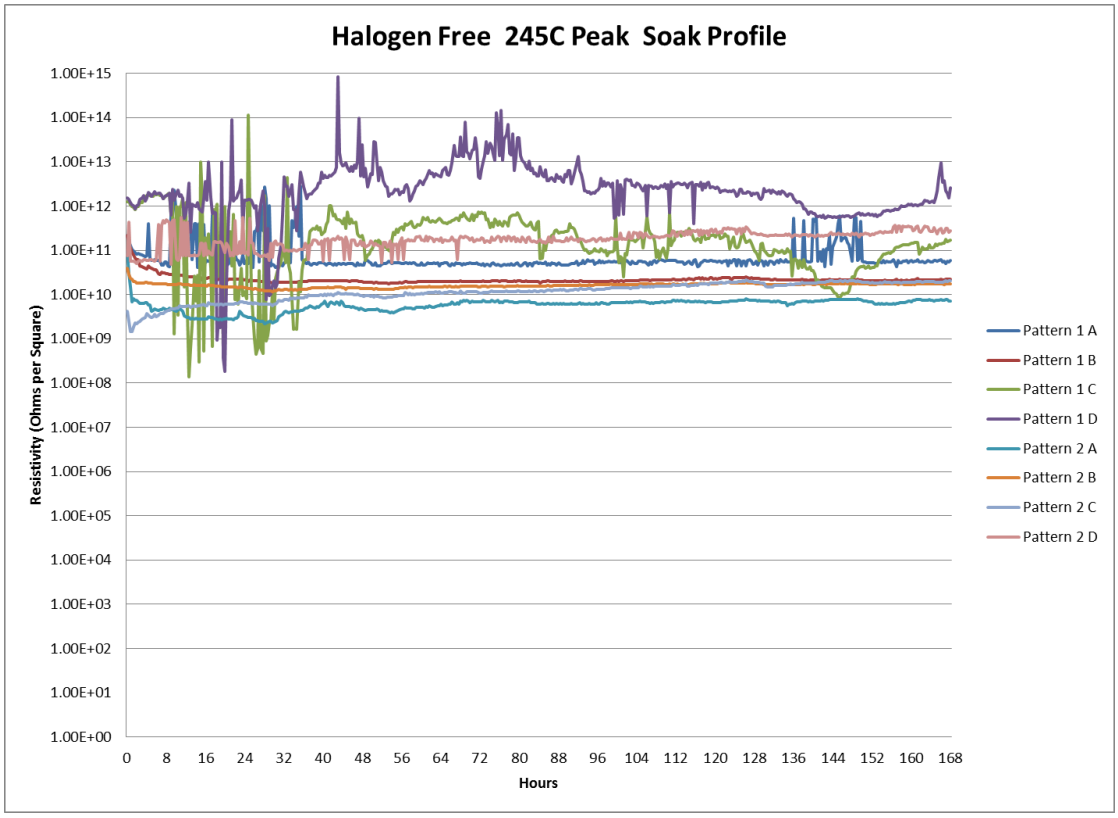


Figure 20 – Halogen-Free Solder Paste, 245°C Peak Temperature Soak Profile (Run 2)

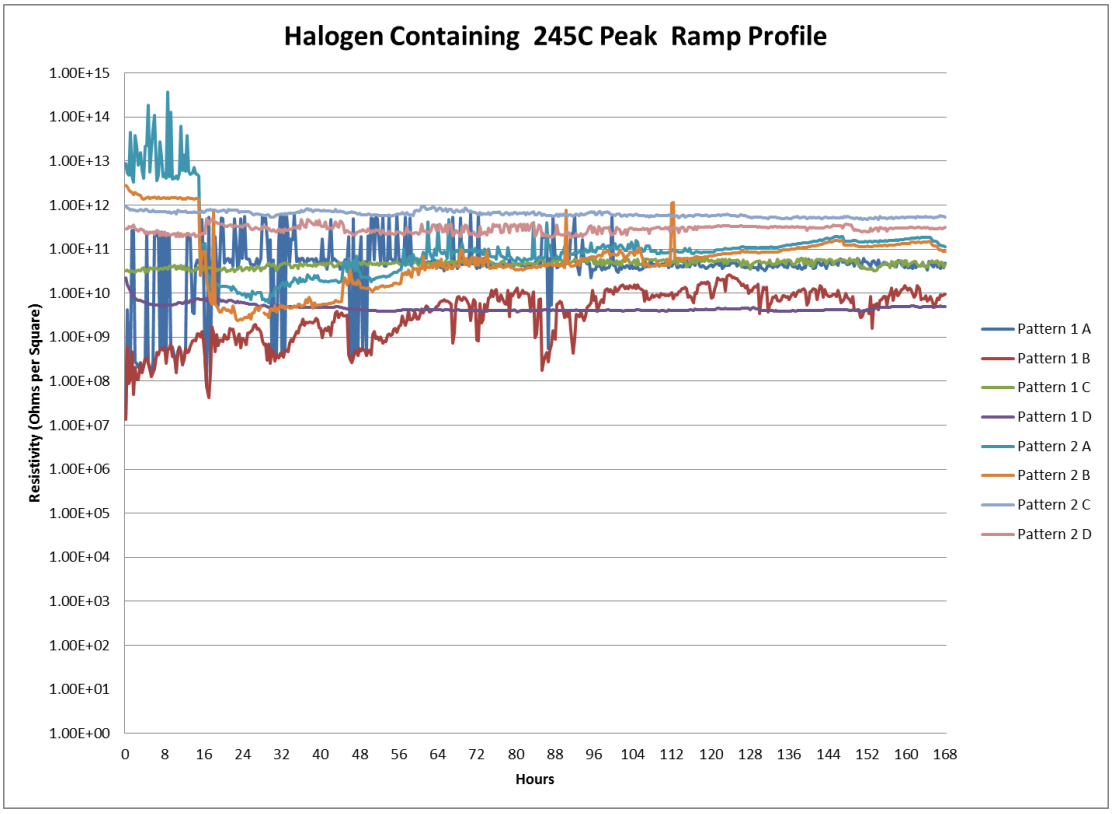


Figure 21 – Halogen-Containing Solder Paste, 245°C Peak Temperature Ramp Profile (Run 2)

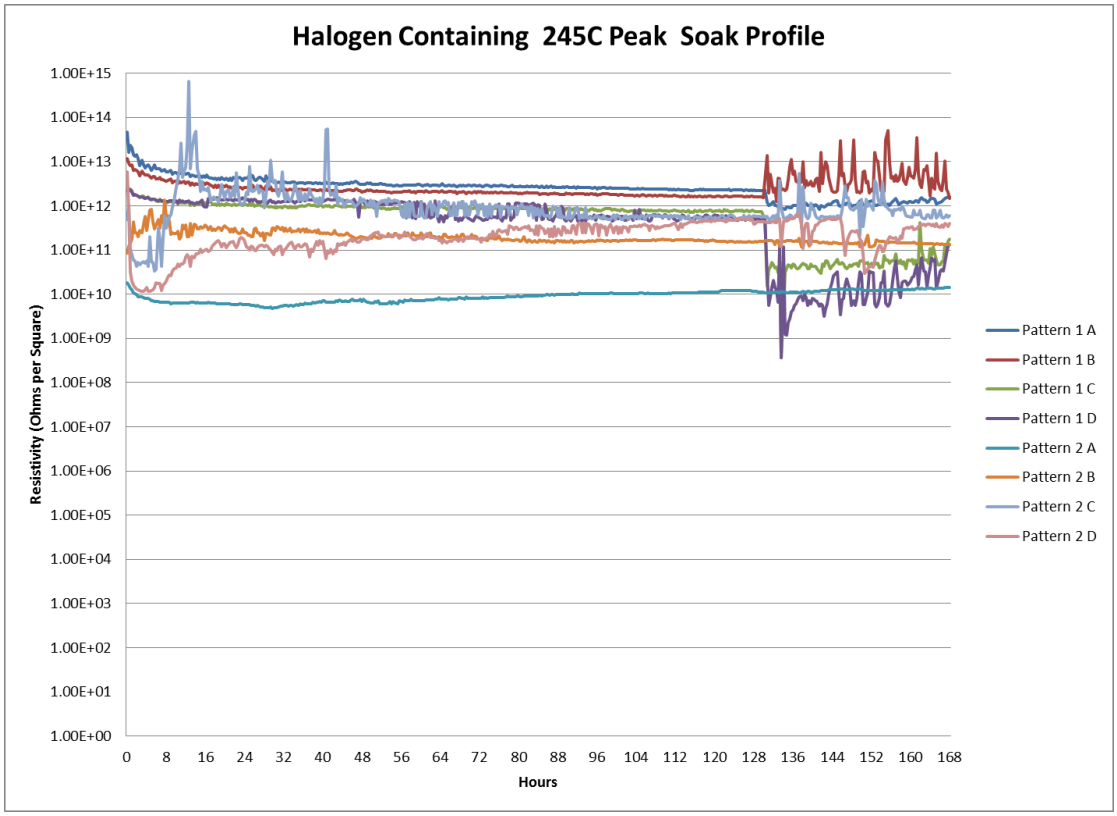


Figure 22 – Halogen-Containing Solder Paste, 245°C Peak Temperature Soak Profile (Run 2)

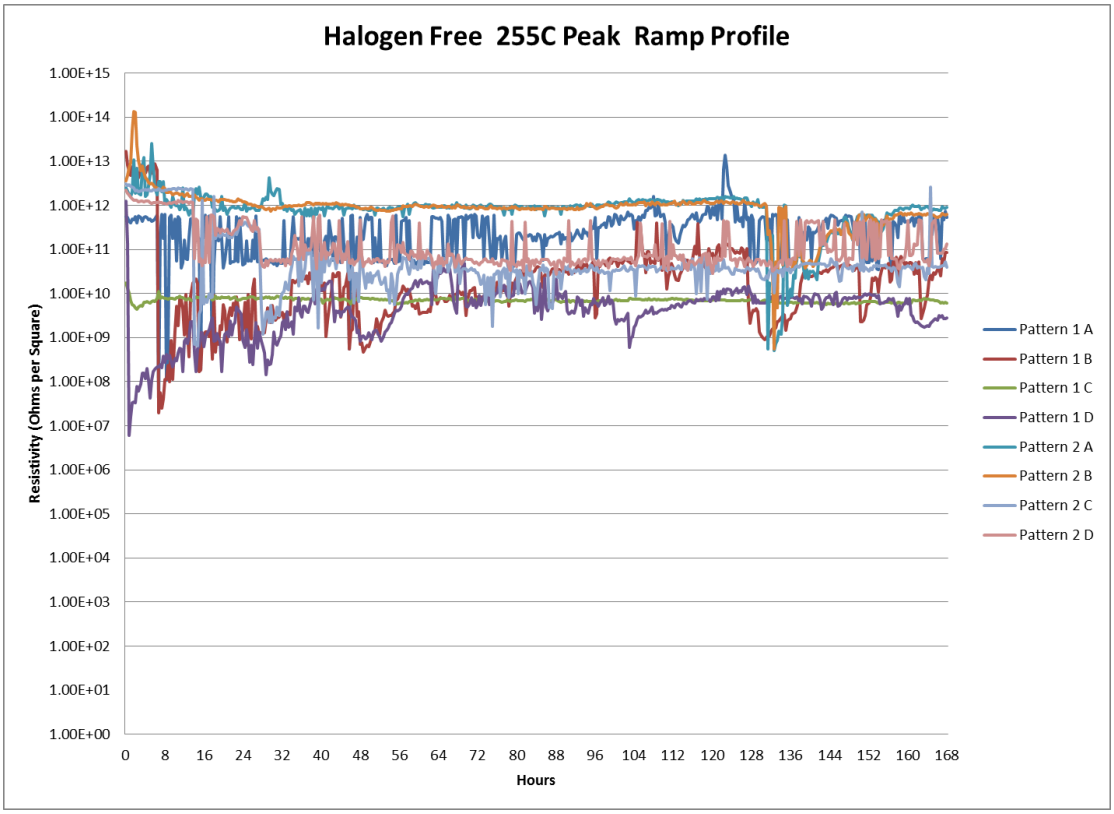


Figure 23 – Halogen-Free Solder Paste, 255°C Peak Temperature Ramp Profile (Run 2)

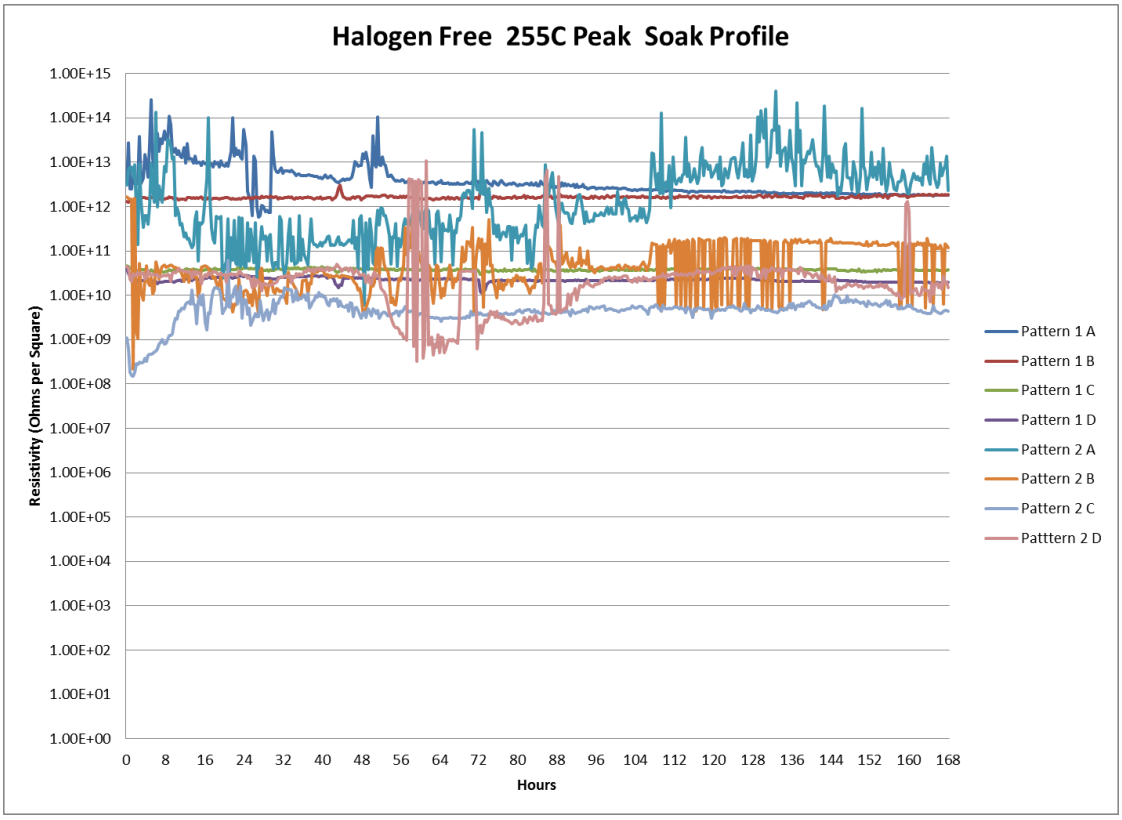


Figure 24 – Halogen-Free Solder Paste, 255°C Peak Temperature Soak Profile (Run 2)

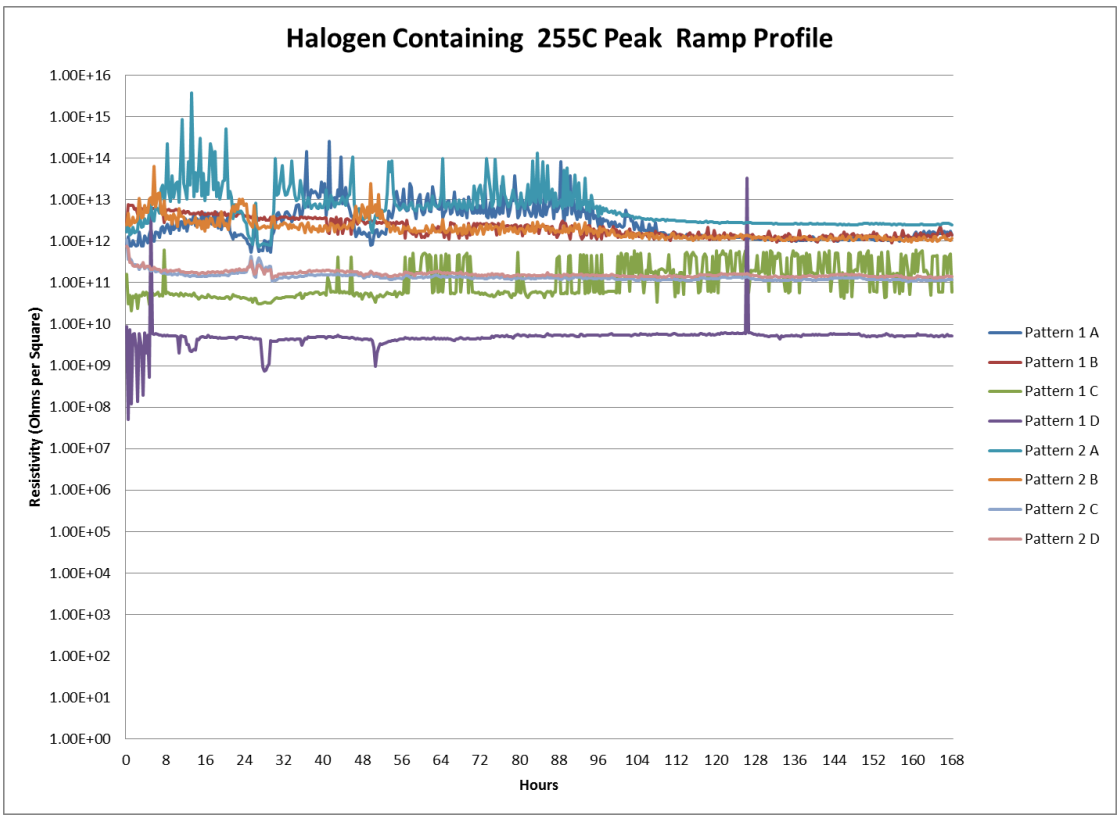


Figure 25 – Halogen-Containing Solder Paste, 255°C Peak Temperature Ramp Profile (Run 2)

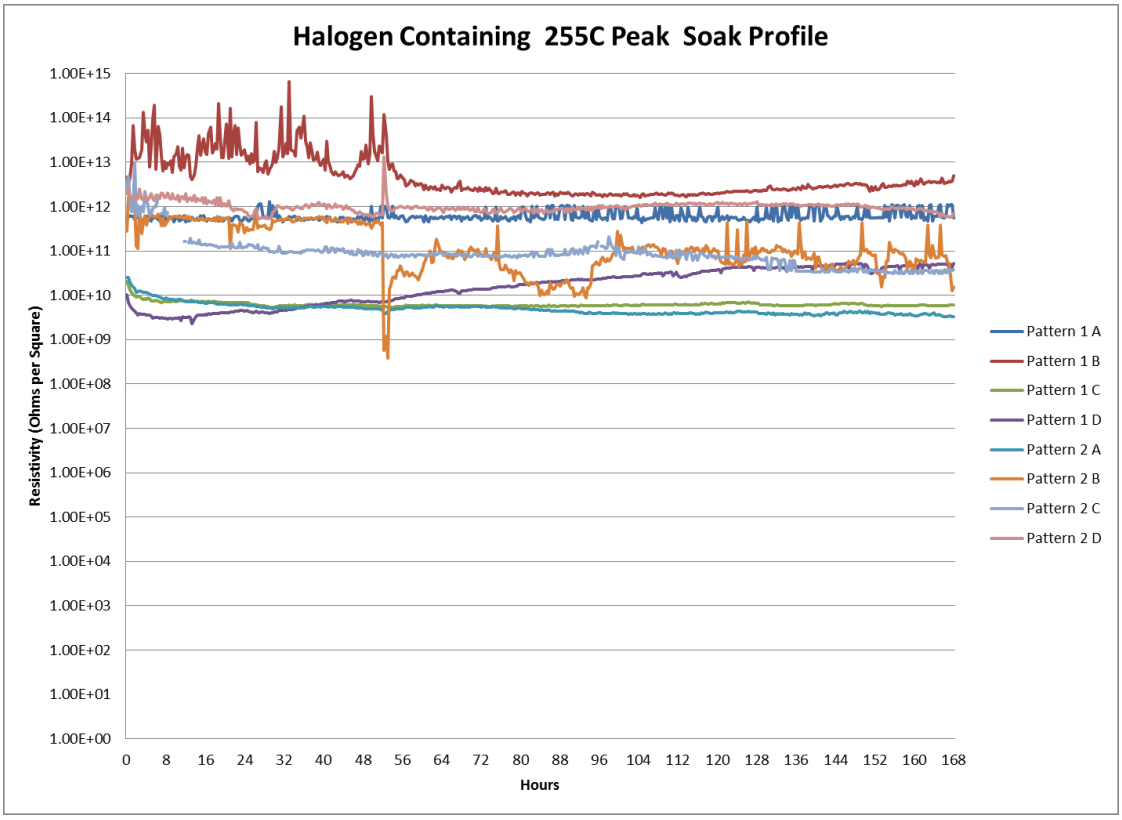


Figure 25 – Halogen-Containing Solder Paste, 255°C Peak Temperature Soak Profile (Run 2)

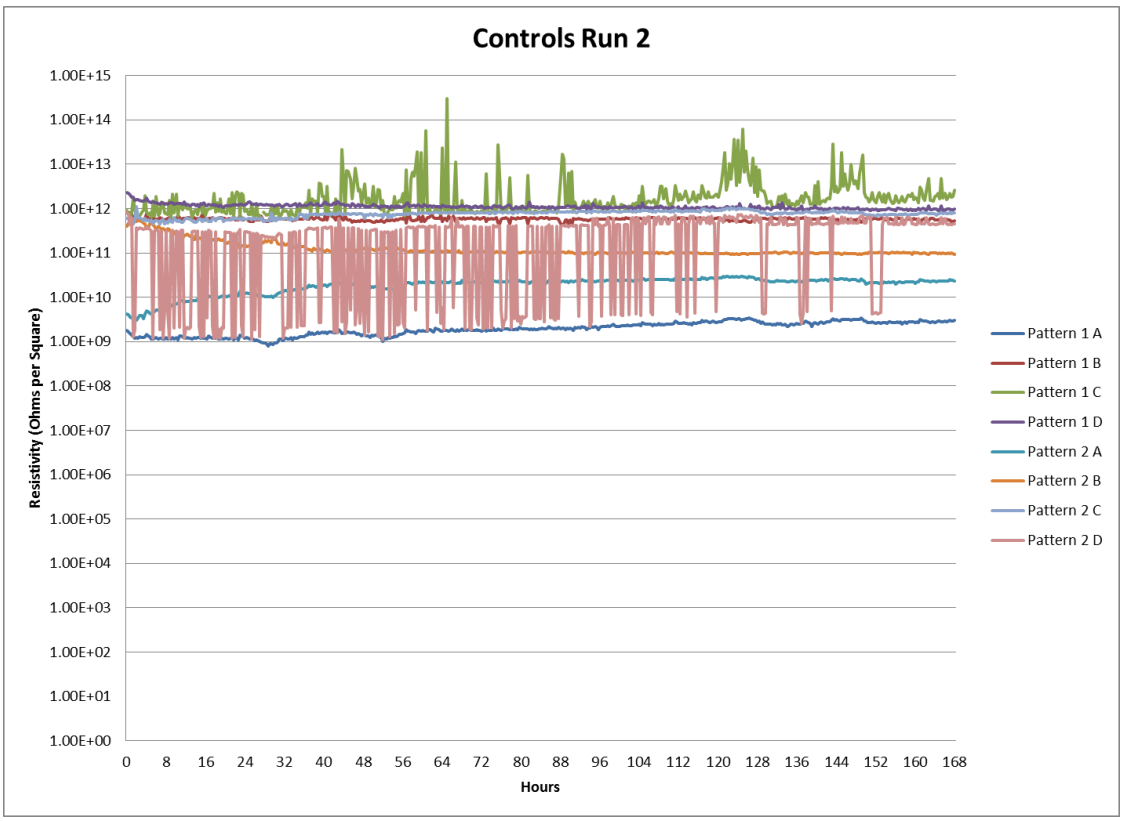


Figure 26 – Controls (Run 2)

The intent of this paper is to show the overall effect, if any, that reflow profiling has on the SIR performance of no-clean solder pastes. Figures 10 through 26 plot every SIR reading of every SIR pattern. Viewing the data in such a way makes it difficult to identify an overall trend from scenario to scenario. In order to be able to do this more easily, an average SIR value was calculated for each scenario. For each scenario, two boards were prepared, with 4 SIR patterns per board. SIR readings were taken for each SIR pattern every 20 minutes over the course of 168 hours (1 week). The result is the accumulation of 4032 SIR readings from which the average SIR value was obtained.

Because of the number of SIR boards and the test chamber's inability to accommodate all the boards at one time, the SIR testing had to be run in two separate batches, as mentioned earlier. An unintended side effect of running multiple batches is the possible occurrence of slight batch to batch variations. The best way to detect these variations is with the controls, as these are bare clean unprocessed (unreflowed) boards. A critical examination of the average SIR values obtained from each scenario seems to indicate that such a variation occurred in this study. The SIR values obtained from Run 2, including those values measured on the controls, were generally lower than those obtained from Run 1. In order to effectively compare all the data as one large data set and reduce the impact of the batch to batch variation, the data was later "normalized".

To normalize the data, the author divided the average SIR value from the controls in Run1 by the average SIR value from the controls in Run 2. That quotient, 1.54, then became the factor by which the average SIR values from the scenarios in Run 2 were multiplied. Figures 27 and 28 show normalized data. Because it is normalized data, it should be used only for relative comparison with the intent of trying to determine any trends.

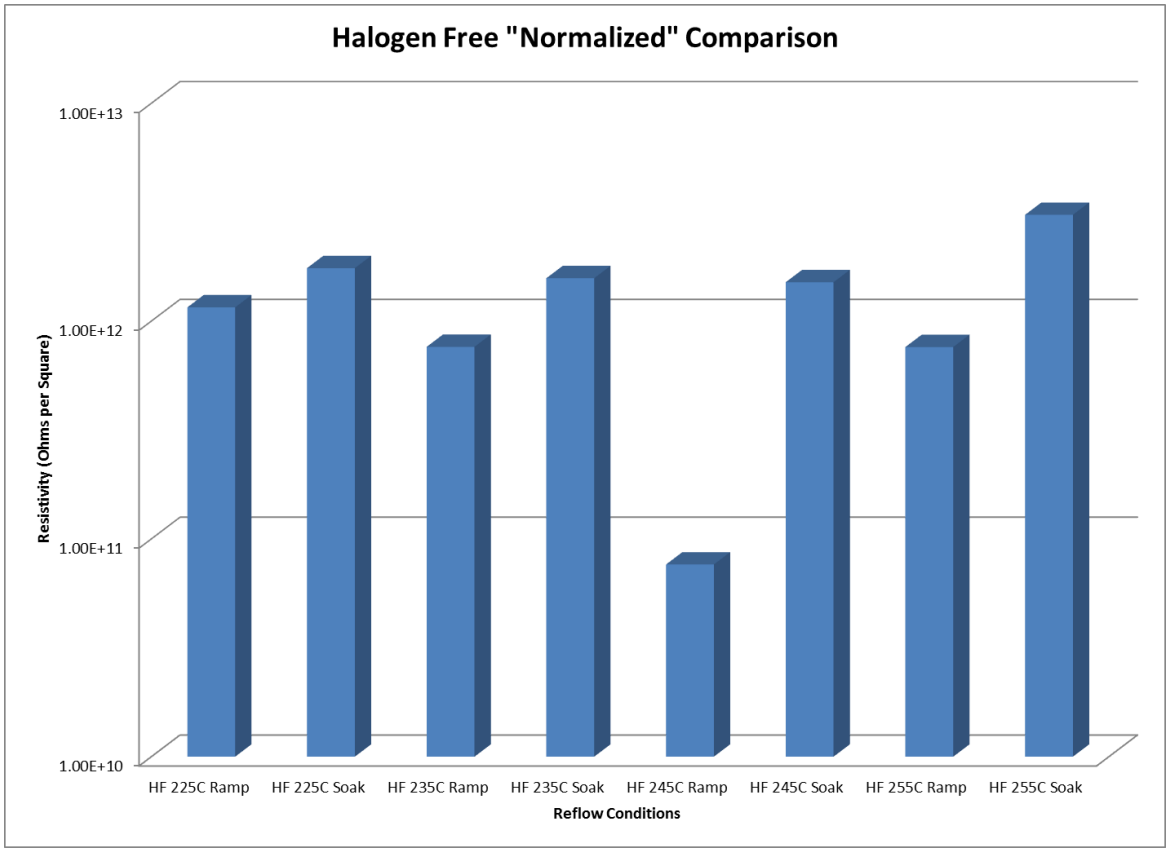


Figure 27 – Halogen-Free Normalized Average SIR Values

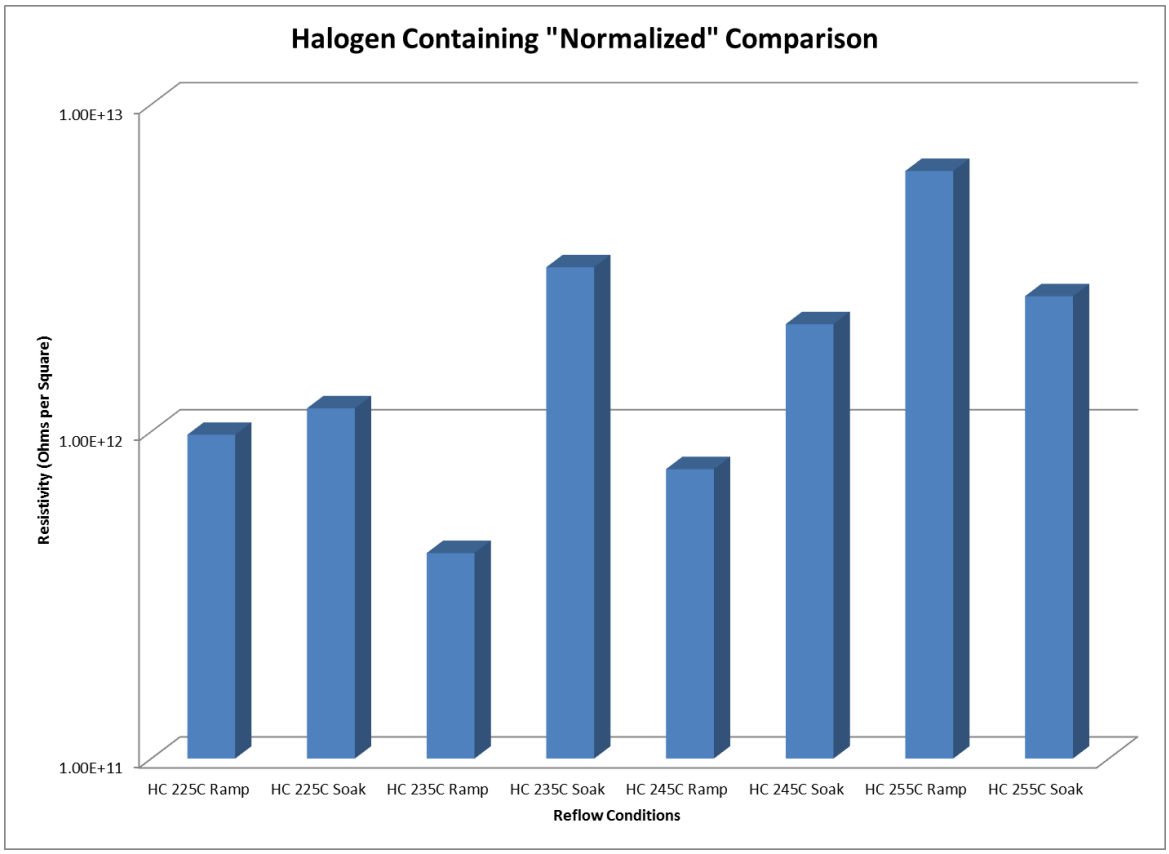


Figure 28 – Halogen-Containing Normalized Average SIR Values

The minimal impact that reflow profiling had on the SIR performance of a no-clean solder paste was quite surprising. It was anticipated that a much larger difference in SIR performance would be observed as a function of the peak temperature. But even at a temperature of 225°C, a mere 5 degrees above the liquidus temperature of SAC305, very good (high) SIR values were achieved. This may be an indication of the advancements that have been made in no-clean flux technology. It should also be noted that there were no visual differences in the appearance of the residues regardless of the reflow profile.

However, it should be kept in mind that the flux residues in this study were exposed on the surface of the PCB as opposed to being trapped under a component body or RF shield. An earlier work by the author shows that entrapment, somewhat regardless of peak temperature, can have a measurable negative effect of the SIR performance [2]. What is noticeable is the effect that a soak has on the SIR values. In all cases, except for the halogen-containing/255°C peak temperature scenario, the soak profile produced higher SIR values than its respective linear ramp profile. The results also imply that a brief soak improves the SIR values more than a 10 degree increase in the peak temperature with a linear ramp profile. It is worth noting that the soak need not be not excessively long to create this improvement in SIR performance. The soak times in this study ranged from only 31 to 40 seconds (time between 200°C and 215°C). This may be good news for applications involving thermally sensitive components and/or substrate materials, or in applications where achieving a higher peak temperature may be challenging due to thermal density. The effect of flux chemistry—halogen-free versus halogen-containing—does not appear to have a significant impact.

Conclusions

There are many variables that affect SIR performance. And with the specific knowledge of the impact of proper heating on a flux's SIR performance, such an experiment as this seemed appropriate. What was surprising is that even with a very short "soak" the SIR performance of a residue can be "improved" more than by using a higher peak temperature. Such knowledge could be useful in such problematic situations as temperature sensitive assemblies and flux residues trapped under component bodies and RF shields. The latter situations can produce unusual visual anomalies and gooey flux residues, as was discovered in a prior work, with less than optimum SIR performance [2. As the acumen of knowledge increases relative to the parameters which affect SIR performance of flux residues, no-clean processes can be honed to provide reliable products. For those processes involving cleaning/removal of no-clean residues, especially with the ever decreasing standoff of SMT components, more work should be done to understand the impact of partial or incomplete removal of such residues.

References

1. IPC J-STD-004 Requirement for Soldering Fluxes
2. E. Bastow, The Effects of Partially Activated No-Clean Flux Residues Under Component Bodies and No-Clean Flux Residues Entrapped Under RF Cans on Electrical Reliability, IPC APEX 2011 conference.