Durable Conductive Inks and SMD Attachment for Robust Printed Electronics

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Abstract
Polymer Thick Film (PTF)-based printed electronics (aka Printed Electronics) has improved in durability over the last few decades and is now a proven alternative to copper circuitry in many applications once thought beyond the capability of PTF circuitry. This paper describes peak performance and areas for future improvement.

State-of-the-art PTF circuitry performance includes the ability to withstand sharp crease tests, 85C/85%RH damp heat 5VDC bias aging (silver migration), auto seat durability cycling, SMT mandrel flexing, and others. The IPC/SGIA subcommittee for Standards Tests development has adopted several ASTM test methods for PTF circuitry and is actively developing needed improvements or additions. These standards are described herein. Advantages of PTF circuitry over copper include: varied conductive material compositions, lower cost and lower environmental impact. Necessary improvements include: robust integration of chip and power, higher conductivity, and fine line multi-layer patterning.

Introduction

The problem we have solved

Common practice for today's PTF circuitry industry is to prescribe careful handling procedures during installation into equipment or devices. Older SGIA(Specialty Graphic Imaging Association)/ASTM and IPC test standards specify milder environmental and performance test conditions compared to that of copper circuitry. This situation has been brought on (in the opinion of the author) by numerous designs of PTF circuitry, varied substrate make and quality, numerous PTF inks of varied compatibility, and the ever driving need for lower prices. Fabricators new to PTF circuitry often attract business with lower prices, not having the overhead or expertise to understand the necessary design criteria and material selection for robust circuitry. Resulting low quality and field failures can damage the market's confidence in PTF circuitry and send users back to copper.

IPC and SGIA have teamed up to develop state-of-the-art test standards for Printed Electronics to provide the means to identify and ensure robust circuitry. Kid gloves handling is not necessary with properly designed PTF circuitry and materials selection. Open sharing of best techniques and materials, that these new standards illustrate, will raise the performance bar for material suppliers and fabricators alike, and raise industry confidence and awareness of PTF circuitry.

Why the problem is not already solved or other solutions are ineffective in one or more important ways

Test standards were historically written not to force a failure, but rather to allow high yield production and customer acceptance. Hence, the relaxed performance criteria.

Material suppliers and circuitry fabricators tend to protect good ideas and advantages as trade secrets. PTF circuit industry symposiums could provide a valuable service to identify where PTF circuitry is winning, where it needs to improve, and how to get there…as a collaborative group.

Much production is locked into older established inks from big name suppliers since fabricators avoid material change if comfortable with production settings and the cost to change legacy specifications. Thereby, many jobs continue to adopt existing Bill-of-Material (BOM) specifications written many years ago and with materials developed over 30 years ago. Attention that is paid to leading edge technology(e.g. nano materials, sintered conductors, ink-jet dispensing)attracts investment, but does not deliver robust circuitry. All the while, valuable improvements in the basic blocking and tackling of material durability goes unnoticed.

Why a better solution is worth considering and why is it effective in some ways that others are not

A well designed selection of materials and design layouts will permit sharp creasing, 85% RH/ 85°C damp heat with bias load aging, SMT mandrel flexing and other critical tests that prove and ensure robust PTF circuitry fabrication.

Material improvements are available in substrate, inks, adhesives, connectors and SMD components. It is important to understand what to look for and test against when selecting your specific material set. Simple techniques for stress management of the various inks and adhesives should be used to add durability.

As more producers of PTF circuitry build to these better standards then the industry as a whole will grow and prosper as confidence in this technology grows.

Other efforts that exist to solve this problem and why are they less effective than our method

Discussions need to take place to better identify where PTF circuitry is succeeding, what factors are holding it back and a framework of how to test and solve these problems with which to improve.IPC should prove an ideal venue for this since much expertise in both copper and PTF circuitry can readily attend and contribute. The Printed Electronics Symposium of the Specialty Graphics Imaging Association remains isolated from copper circuitry expertise and users of electronic circuitry. The creation of the Flexible Hybrid Printed Electronics pavilion at IPC APEX EXPO 2017 is welcomed and overdue.

Current efforts of the Flexible Hybrid Electronics initiative are well targeted to the integration of chip, power and Printed Electronic circuitry and will surely offer a better understanding of material and design requirements. The industry would also be well served by considering near-term and durable solutions for robust circuitry.

The remainder of the paper discusses IPC and ASTM test standards pertinent to PTF circuitry durability, their description and what to look for in material sets for peak performance.

Implementation

Pertinent IPC/ASTM standard tests

The following ASTM test standards were primarily written by the Membrane Touch Switch group which started in the early 1980's and later adopted and sponsored by SGIA.

ASTM F1596-15 Standard Test Method for Exposure of a Membrane Switch or Printed Electronic Device to Temperature and Relative Humidity

This test method is performed to evaluate the properties of materials used in the construction of membrane switch or printed electronic assemblies as they are influenced by the absorption and diffusion of moisture and moisture vapor. This is an accelerated environmental test, accomplished by the continuous exposure of the test specimen to high relative humidity at an elevated temperature. Absorption of moisture by many materials results in swelling, which destroys their functional utility, causes loss of physical strength, and changes in other mechanical properties. Insulating materials which absorb moisture may suffer degradation of their electrical properties.

The F1596-15test specifies 55°C/85%RH for 240 hours, non-condensing, <2mA load. The IPC TM650 2.6.3.3 test for Surface Insulation Resistance on copper circuitry specifies 85°C /85%RH 168 hours 50VDC. Environmental tests for solar panels apply 85°C/85%RH to represent outdoor aging. Ink manufacturers can and should test PTF circuitry at 85°C/85%RH and 5VDC bias to prove robust properties. A proper material set printed well can withstand 500 hours in these conditions.

ASTM F1662-16 Standard Test Method for Verifying the Specified Dielectric Withstand Voltage and Determining the Dielectric Breakdown Voltage of a Membrane Switch or Printed Electronic Device

This test method is used to verify that the membrane switch or printed electronic device can operate safely at its rated voltage, and withstand momentary over potentials due to switching, surges and other similar electrical phenomena.

Most dielectric insulators can and should withstand 2500 VDC.

ASTM F1689-05 Standard Test Method for Determining the Insulation Resistance of a Membrane Switch

Low insulation resistance can cause high leakage currents. High leakage currents can lead to deterioration of the insulation or false triggering of the associated input device, or both.

There is a wide variation in dielectric insulators and their ability to withstand leakage currents.

ASTM 2749-15StandardTest Method for Creasing Membrane Switch or Assembly

Creasing a membrane switch or their components can affect their visual appearance, mechanical integrity or electrical functionality. This practice simulates conditions that may be seen during manufacture, installation or use.

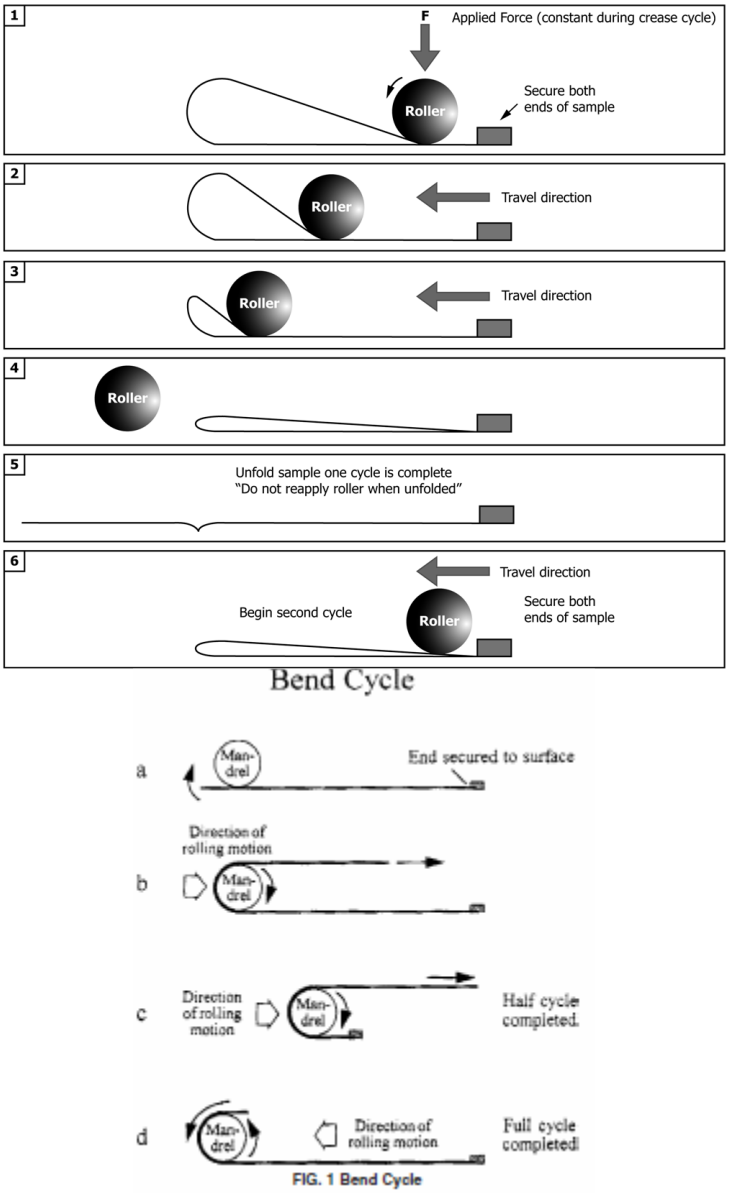

Figure 1. Crease Test Fixture Setup (from ASTM 2749-15)

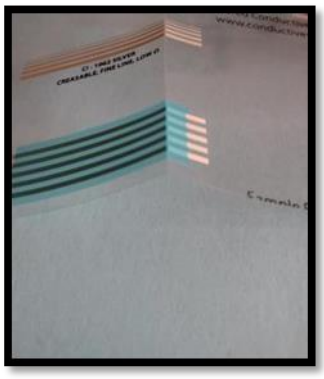

Figure 2.Creased test coupon

Highly durable silver ink and insulator combinations can withstand crease cycles of compression followed by extension (one cycle) for over 10 cycles.

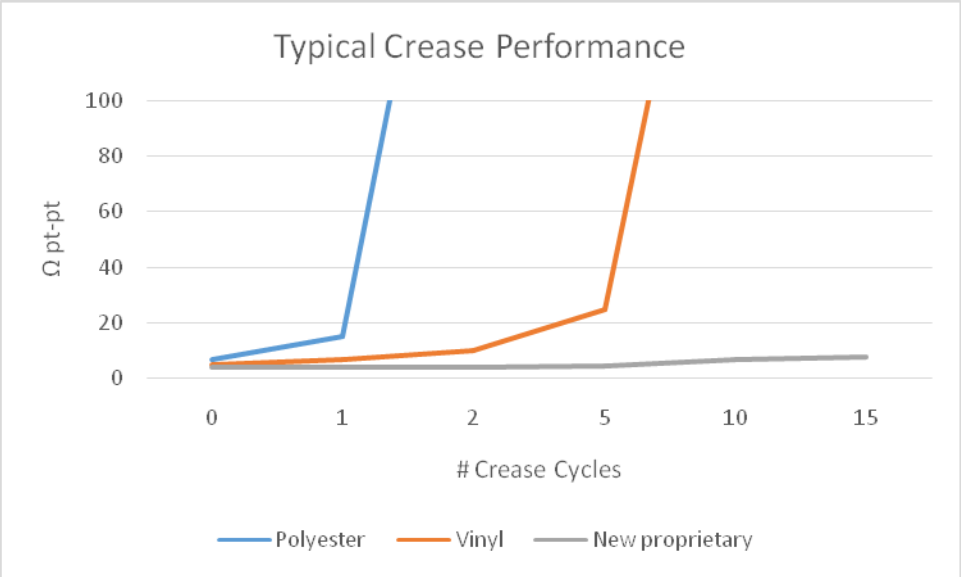

Figure 3. Crease test performance comparisons

ASTM F2750-16 Standard Test Method for Determining the Effects of Bending a Membrane Switch or Printed Electronic Device

Bending of membrane switches, printed electronic device or their components can affect their visual appearance, mechanical integrity or electrical functionality. This test method simulates conditions that may be seen during manufacture, installation or use.

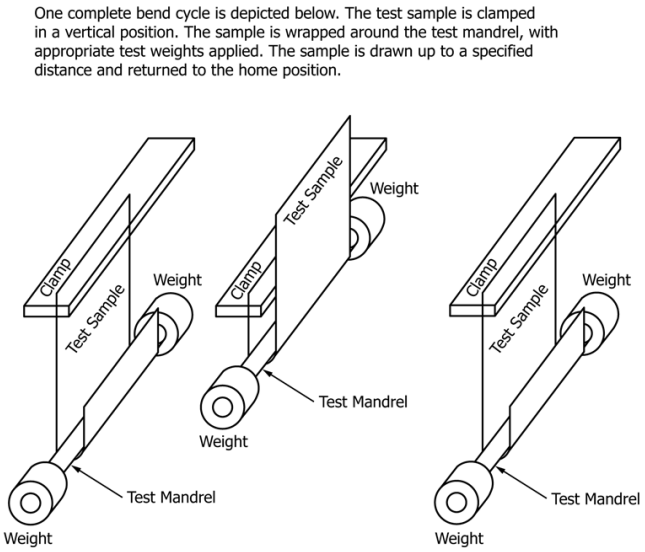

Figure 4.Bend test fixture setup (from ASTM F2750-16)

A robust ink set on a compatible substrate can withstand over 500,000 bend cycles. This is important in applications that see repeated deformation.

ASTM F1842-15 Standard Test Method for Determining Ink or Coating Adhesion on Flexible Substrates for a Membrane Switch or Printed Electronic Device

If the ink or coating is to fulfill its function, it must adhere to the substrate. Substrates and their surface preparation have a significant effect on the adhesion of inks or coatings. Therefore, a method of evaluating adhesion of inks or coatings to different substrates or surface treatments, or of different inks or coatings to the same substrate and surface treatment, is useful to the industry. This test method is based on existing Test Method ASTM D3359-09e2, with modifications to make it suitable for flexible substrates, printed electronic devices and membrane switches.

5B adhesion (best) should be expected for all conductive and insulation materials on given substrate.

Figure 5. 5B or Excellent Adhesion

Figure 6. 3B or Poor Adhesion

ASTM F1996-14 Standard Test Method for Silver Migration for Membrane Switch Circuitry

This test method is used to determine the susceptibility of a membrane switch to the migration of the silver between circuit traces under dc voltage potential.

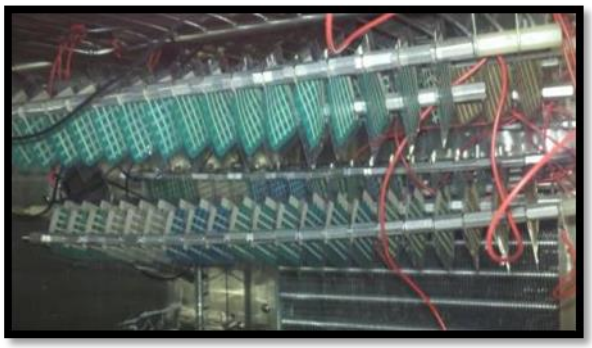

Figure 7. Printed Test Coupons in Humidity Chamber Wired for Bias Load

Material suppliers can and should strive for 85°C/85%RH 5VDC bias for over 500 hours. This requires best-in-class but available dielectric insulators.

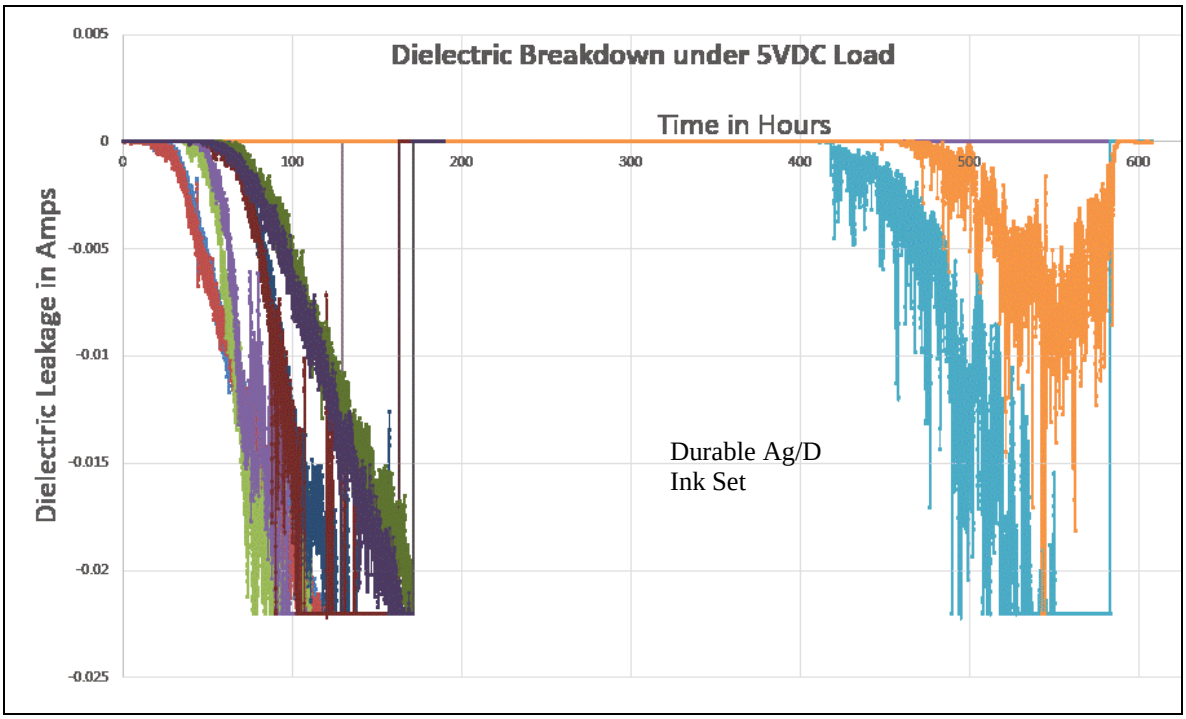

Figure 8.Dielectric Leakage in Amps during 85%RH/85°C 5VDC Aging

ASTM F3147-15 Standard Test Method for Evaluating the Reliability of Surface Mounted Device (SMD) Joints on a Flexible Circuit by a Rolling Mandrel Bend

The existing Test Method ASTM F1995-13, while very useful, is difficult to conduct if an encapsulating dome is applied, and does not reveal the possible failures caused by mechanical stress incompatibility in the overall SMT joint. This mandrel bend test will reveal possible mechanical stress incompatibility between the various adhesives which can result in latent field failures during production handling or with thermal cycling in normal use.

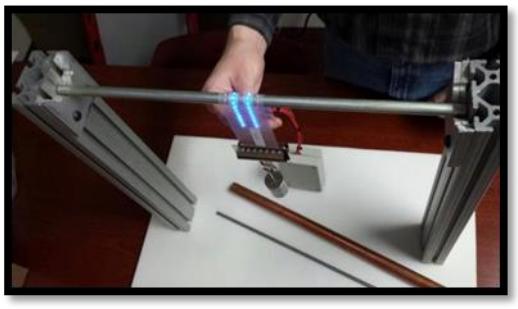

Figure 9.SMT Mandrel Test

Figure 10.Robust SMT Joint Design

A properly designed layout and material set should survive 10 cycles of 1/4" diameter mandrel and 1kg weight. The test with LEDs attached will flicker upon failure.

ASTM F2357-10 Standard Test Method for Determining the Abrasion Resistance of Inks and Coatings on Membrane Switches Using the Abrader Wear Tester

This test method provides a way of comparing relative abrasion resistance of inks and coatings.

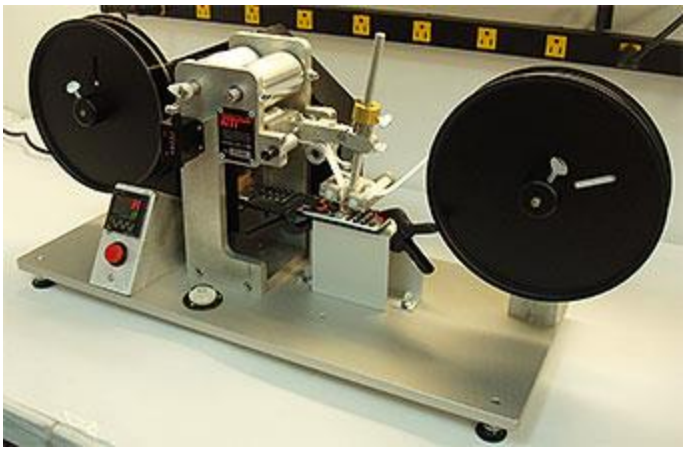

Figure 11. Abrader Wear Tester

ASTM F0.1.18 Standard Practice/Guide for Handling and Application of a Membrane Switch or Printed Electronic Assembly to its Final Support Structure (under development)
This developing handling and application guide includes many precautions that seem required for sub-standard material sets such as older formulations that are many legacy Bill of Materials.

The following standards were more recently developed by the Printed Electronics Functional Materials Subcommittee(D-63) of the Printed Electronics Committee (D-60) of IPC.

IPC-2292 Design Standard for Printed Electronics on Flexible Substrates
This standard establishes the specific requirements for the design of flexible printed electronic circuit applications and its forms of component mounting and interconnecting structures.

IPC-9204 Guideline on Flexibility and Stretchability Test Methods for Printed Electronics
This document provides an overview of proposed test methods that may be suitable for use to evaluate flexibility and stretchability of printed electronics for flexible, stretchable and wearable applications.

Figure 12. Silver and Insulator on TPU Film under Stretch

IPC/JPCA-4921 Requirements for Printed Electronics Base Materials (Substrates)
This standard establishes the classification system, the qualification and quality conformance requirements for printed electronics base materials (substrates).

IPC/JPCA-2291 Design Guideline for Printed Electronics
The intent of IPC/JPCA-2291 was to establish a design process flow that would facilitate and improve the practice of printed electronics design. IPC/JPCA-2291 identifies documents such as standards that can be used to assist during the design process flow.

IPC/JPCA-4591 Requirements for Printed Electronics Functional Conductive Materials
This standard establishes the classification system, the qualification and quality conformance requirements for printed electronics functional conductive materials.

How a Properly Design PTF Circuit Should Work

Silver ink and insulator combinations should pass 10 sharp crease cycles without electrical discontinuity (Figure 3). This proves robust performance when circuits are handled roughly or if, for example, tails need to be sharply creased in use for a specific device and restricted real estate.

Silver ink and insulator combinations should withstand 85°C/85%RH exposure with 5VDC bias for over 500 hours with no shorts. This is needed to prove that PTF circuitry can replace copper circuitry in harsh environments (Figure 8).

Properly designed SMT joints of package sizes 0402, 0603 and 1206 should withstand 10 mandrel cycles on ½" diameter mandrel with no loss of conductivity for resistors or flickering for LEDs. Again, this proves PTF circuitry performance in harsh environments and handling.

Silver ink, insulators and carbon inks on given substrates should survive automotive seat durability tests which requires millions of deformation actuations.

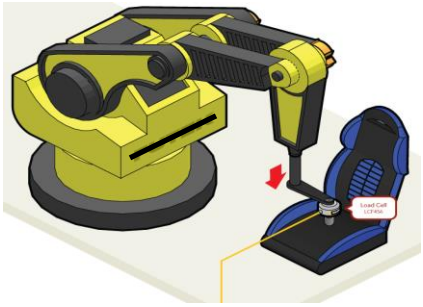

Figure 13.Car seat durability test

Beware that random material sets and mix-and-match can be a perilous path

Conductive and insulation material providers should put much effort into developing compatible ink sets in terms of mechanical and chemical compatibility between each layer. Unfortunately, many do not and field failures can give the entire industry a bad reputation. Using the proper test standards can ensure that the printed electronics developed are robust.

Conclusions and Future Work

The problem we have solved

Robust PTF circuitry with mounted components is not only possible, but should be mandatory for the success of the industry.

What we will (or could) do next

The biggest challenge to PTF circuitry is the integration of IC chip and power. Current best practices are to integrate a copper flex circuit with the IC chip and power to the PTF circuit. Developments in printable memory, flexible power cells and highly conductive interfaces should provide answers in the future. As for the timeline for these new developments, 20 years ago it was predicted printed IC would be available today. Clearly we are not there yet. Some companies have attached IC to PTF Electronics, but it is not mainstream.

References

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