

DIELECTRICS FOR EMBEDDING ACTIVE AND PASSIVE COMPONENTS

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ABSTRACT

Embedding of actives and passives is a quickly growing field which is being investigated by many companies and institutes. Reasons for this increasing interest are to reduce the complexity of the packages, achievement of higher degree of miniaturization, shorter electrical connections, and a reduction of layer count.

Among other technical challenges, warpage is a major concern. The inherent different thermomechanical properties of the different materials involved cause internal stresses. Those stresses show up as warpage which makes handling during production more difficult, reduces the overall yield, and imparts reliability.

Presented in this paper is a composite type material which can be used as dielectric for the embedding of actives and passives. It combines the advantages of the mechanical stability of prepregs and the good encapsulation properties and ease of handling of resin coated copper foils (RCC). Also described is a concept for simulating the warpage of packages using such composite build-up materials taking into account different resin properties.

Key words: Embedding material, actives, passives, simulation, warpage

INTRODUCTION

In the area of chip embedding there are currently two main technologies which find increasing interest. Packages which are based on a molded wafer infrastructure (Fan out wafer level packages, FOWLP), a technology which is mainly driven by the large packaging houses which already have much of the required infrastructure or which have the necessary capital for the needed investments^[1].

The other principal technology uses the know-how and the equipment which is used in printed circuit board (PCB) manufacturing. This panel based approach is of main interest for PCB companies which want to extend their product portfolio and see a chance to enter the market of chip packaging.

Advantages of FOWLP are that there is no need for an organic substrate like a copper clad laminate (CCL), the use of existing supply chains because the existing packaging players can implement this technology, and huge investments which are already made in the last two years. Technical challenges are currently the restriction to 200 mm / 300 mm wafer size and the need to shift to panel formats to reduce costs, the need to develop “3D” capability, current package size limitations of 8 mm x 8 mm, and die shift during shrinkage of the mold compound during curing^[1].

The technology of die embedding using a PCB infrastructure has the intrinsic advantage to use panel size, the possibility to connect both sides of a panel (“3D” intrinsically given), and the fact that relatively thick copper tracks can be made which opens the way to embed high power components like insulated gate bipolar transistors (IGBT) or metal oxide semiconductor field effect transistors (MOSFET). Issues with this approach are the complex supply chain, a lower rerouting density, currently low manufacturing yields, warpage due to CTE mismatch, and laborious process steps like pre-machining (cavity formation) of prepregs^[1].

The two main techniques in the die embedding arena are “chip first” and “chip last”^[2,3,4,5]. Whereas “chip first” has the highest potential for miniaturization, formation of thin packages, and good thermal properties, it suffers from very high cost of yield loss. For final testing the substrate manufacturer requires detailed information regarding the test program and the IC, which is sensitive information and which the semiconductor IC company does normally not want to disclose.

The “chip last” approach has the advantages that only known good dies (KGD) are actually used and assembled after most of the PCB processes are completed and that all kind of cooling systems and interconnect technologies can be applied directly on top of the die. On the other hand the thickness cannot be reduced so much, it is less suitable to system in package (SiP) applications and a complex process for cavity formation in the prefabricated PCB is needed.

Both approaches have their merits and drawbacks and will find their niches in the market place. Among others there is interest for high power applications^[6], for electromobility^[7], for high frequency applications^[8], embedding of passive devices^[9], embedding for flexible and medical devices^[10].

TECHNICAL CHALLENGES WITH DIE EMBEDDING

Embedding technology provides a lot of advantages but also several risks and challenges that have to be overcome. One of the major concerns is on process yield related to the fact that the value of PCBs with integrated components is increased by orders of magnitude and so is the costs of yield loss.

Warpage of boards after lamination/curing and in application are a particular challenge as a variety of different materials with significantly different thermo mechanical properties is packed jointly into one build-up. This affects both, yield and reliability.

Some early work regarding chip embedding using the “chip first” approach used RCC for the embedding of the dies^[11]. Resin coated foils are readily available, handling is easy, and there is no need for cavity formation in the resin, i.e. the resin can directly encapsulate any given structure. The disadvantage of this methodology is the limitation of resin thickness of the RCC and therefore a limitation in the thickness of the dies which can be embedded. Warpage is a concern for unsymmetrical designs because common RCC materials have a rather high coefficient of thermal expansion (CTE). Another technical limitation of RCC for embedding, apart from its high CTE, is the limited resin thickness of RCC materials and therefore also a limitation regarding the thickness of the dies which can be embedded.

Prepregs are an alternative to RCC. Prepregs are commercially available with a variety of resin systems and thicknesses. In a first step cavities are formed by laser. The pre-machined prepregs are then stacked on top of each other and the chips are placed into the openings. The whole stack is then vacuum pressed and cured, this is illustrated in Figure 1. Warpage is better controlled in this approach due to the lower CTE of the prepregs. One problem can be protrusion of glass fibers into the cavity enclosing the chip. A huge disadvantage is the need for the cavity formation process which is an additional costly process step.

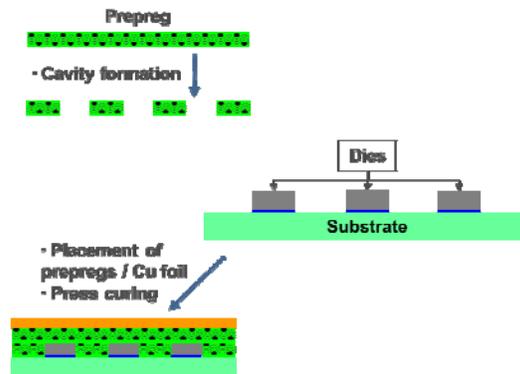


Fig. 1: Embedding approach using pre-machined prepregs

Figure 2 shows an example of a power demonstrator which was part of the HERMES project^[11]. This shows that in reality a number of prepregs have to be pre-machined, depending on the thickness of the structure.

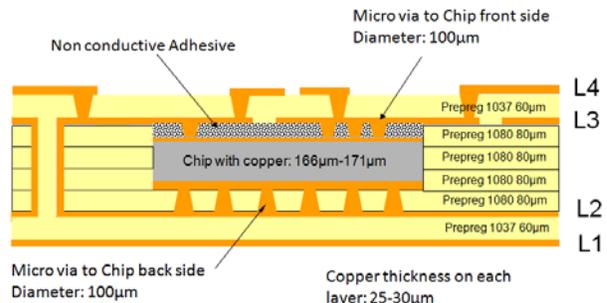


Fig. 2: Example of a power demonstrator which needs numerous pre-machined prepregs (courtesy of Infineon/HERMES consortium)

COMPOSITE MATERIAL FOR EMBEDDING MANUFACTURING

Atotech has been active in the development of RCCs for the last years. A proprietary solvent free technology for the manufacture of dielectrics for the high end PCB and packaging industry was developed. Here the focus is on the manufacturing of resin coated copper foils (RCC), reinforced resin coated copper foils (RRCC), and coated polymer foils. Those semi-finished goods are used at the customer site for the formation of build-up layers, the production of coreless structures, and for embedding. The overall process is entirely solvent free and is to some degree similar to powder coatings which are used in other industries^[12].

The unique procedure which was developed over the last years and which is used to manufacture such products is illustrated in Figure 3.

From solid raw materials (resins, hardeners, flame retardants etc.) a powder is produced by melt extrusion and subsequent milling^[13].

The powder is scattered on the substrate, for example a copper foil, in a continuous roll to roll process. Shortly after the powder deposition the powder is molten in an oven and forms a closed film which sticks to the substrate surface. At

the same time the oven conditions can be set in order to achieve a defined b-staging of the resin.

A glass fabric is being laminated in this resin layer of this RCC in a subsequent roll to roll production step. Since the stress on the glass fabric is negligible, there is no risk of damaging or destroying the fabric and therefore also ultrathin glass fabrics can be deployed. The degree of b-staging is defined by the lamination parameters.

A second resin layer is then deposited and molten on top of the reinforced layer of the RRCC. This final product, a composite type material, can be applied to embed actives and passives.

The absence of solvent is an important aspect of the overall process. Solvent could swell the underlying resin of the reinforced layer. This could impart the position of the glass fabric which was already defined in the previous lamination step. Solvent which penetrated this resin layer would be difficult to be fully removed by evaporation and might partially remain in the resin which would then pose a huge risk in terms of reliability after being applied on a PCB. Furthermore due to the low solid content and low viscosity of solvent based lacquers the maximum thickness which can be achieved is always inherently limited. Such limitations are absent with a 100 % solid system like powder coatings.

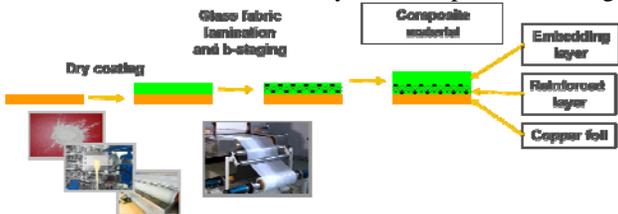


Fig. 3: Sequential process to manufacture composite embedding material: Dry coating of the first layer, lamination of glass reinforcement, dry coating of embedding resin layer.

THICKNESS DISTRIBUTION

The suggested composite material can be used to embed active and passive structures by vacuum pressing or lamination. In contrast to prepreg embedding there is no need for a cavity formation step. The sheets of the composite material are laid up on the structure to be embedded and pressed and cured in one single step.

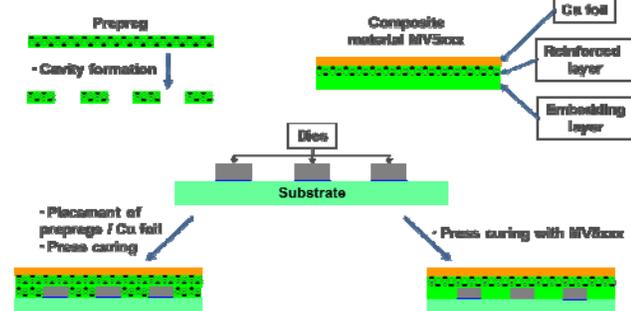


Fig. 4: Embedding using pre-machined prepregs and composite type material

Two representative examples are shown in Figure 5. All the area of the lead frame and around the die is filled with the resin of the embedding layer. The degree of b-staging allows the optimization of the rheology of the resin which guarantees void free encapsulation of the entire structure under the given processing conditions. The glass fabric reinforcement is situated above the chip. The reinforcement defines the distance and the uniformity between the chip surface and the copper foil, while the glass cloth is kept in a defined position.

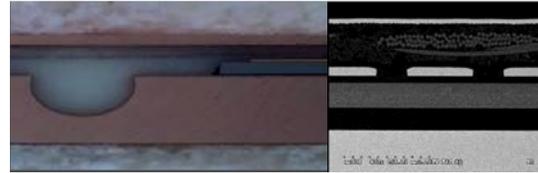


Fig. 5: Left: Embedding of chips on a Cu lead frame; void free resin encapsulates the whole structure; Right: well defined glass fabric position on top of the die

A test design with dummy structures was created in order to evaluate the lamination performance, the thickness distribution, to optimize the press profile, to compare different resin formulations, and to determine the influence of the rheology of the resin. This design is shown in Figure 6. The notation (A1, A2 etc.) indicates the position where measurements are taken, e. g. the thickness by cross section.

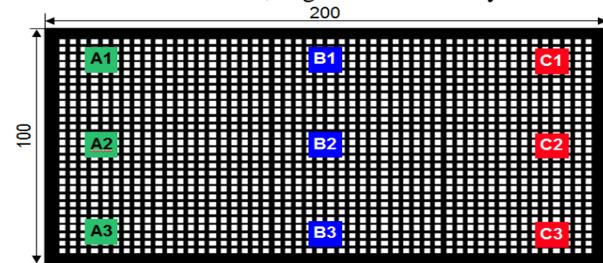


Fig. 6: Test layout used for the evaluation of composite material performance

A typical result of the thickness distribution is shown in Figure 7. In this case the reinforced layer was made using a glass type 1027 and the thickness above the structure is very uniform. This good thickness distribution will facilitate the laser drilling of microvias which will connect the chip to the next layer.

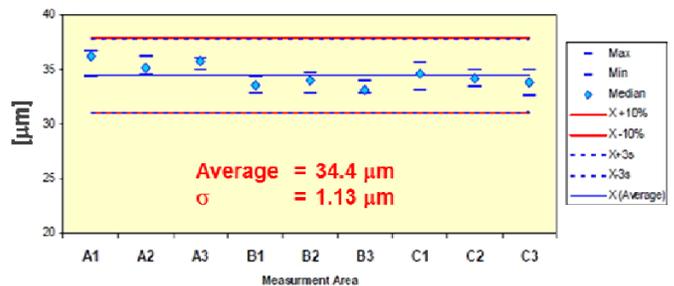


Fig. 7: Thickness measured above the dummies by cross section

STRUCTURES WHICH CAN BE EMBEDDED

The composite materials can be used to embed a variety of different layouts and different chip thicknesses. According to Yole report on “FOWLP & Embedded Die Packages” from 2012 the thicknesses of chips to be embedded by 2013/2014 will be in the range of 30 - 350 μm [1].

The dielectric resin thickness which is required to encapsulate a given design can be estimated consulting the chart shown in Figure 8. It shows a plot of the free area for a given layout versus the thickness of the active/passive which is to be encapsulated. The different colored zones indicate different thicknesses of the embedding layer of the composite material. The thickness of the dies and the free area on the layout are the two factors which determine the amount of resin which is needed. For example in order to embed a structure with chips having a thickness of 150 μm and the design having a free area of 70 %, the thickness of the embedding layer should be in the range of 140 μm .

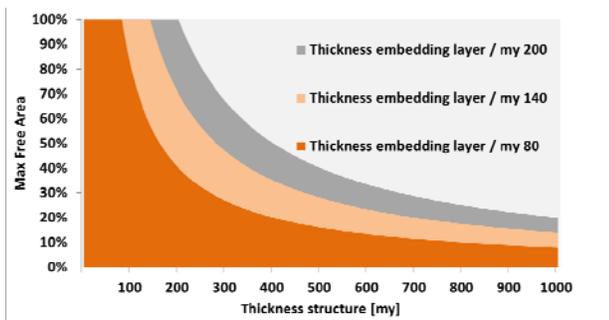


Fig. 8: Free area for a given die thickness and the required thickness of the embedding layer

Another example is illustrated in Figure 9. Two cases are shown: A die with a thickness of 150 μm and multi layer ceramic capacitors (MLCC) of similar height surrounding it. If the design has a free area of 38 %, a thickness of the embedding layer of 80 μm would be sufficient for encapsulation. The second example shows a die with a height of 600 μm , again surrounded by MLCCs having a lower thickness than the dies. In this case the required embedding resin thickness is in the range of 220 μm . This last example also shows the potential to embed structures in which parts of different size and height are present at the same panel, for example actives and passives or different kind of dies.

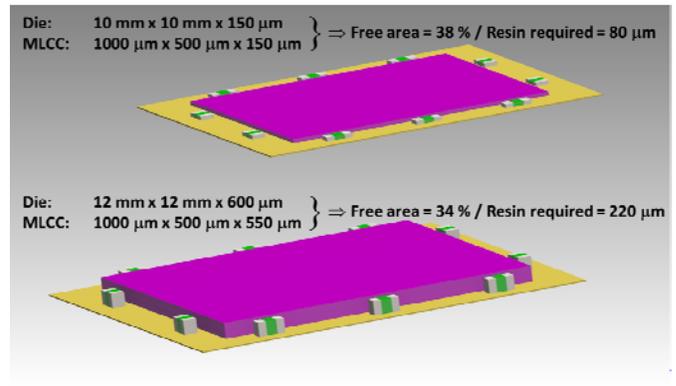


Fig. 9: Example of two design layouts with different form factors and the required resin thickness needed

The capabilities of the composite type material will reach its limits when it comes to the embedding of layouts which have a high free volume which has to be filled with resin. This is either the case with very thick structures and/or a low density of components per area unit. The limiting factor for the maximum resin thickness is not the powder coating step itself, but rather the adhesion of the b-staged embedding layer on the reinforced layer during manufacturing. The b-staged resin can flake off in the reel to reel process if the layer becomes too thick.

The actual current available composite materials in terms of thickness ranges are indicated in Figure 10.

The carrier copper foil can be ultrathin low profile copper or standard profile copper. The standard profile foils can be used for subtractive structuring, the ultrathin low profile foils are intended for modified semi additive plating (MSAP) fine line structuring.

Regarding the reinforced layer as thin as 25 μm can be realized (1015 glass), thicker glass fabrics like 1027, 1037 can also be used. Even thicker glass fabrics can be employed which could be of interest for embedding of thick copper structures for high power applications. The embedding layer thickness which can be currently produced ranges from 20 μm - 200 μm .

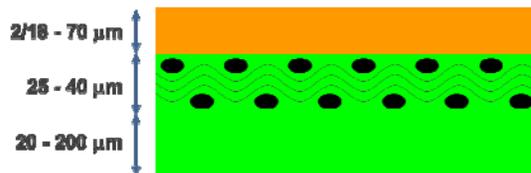


Fig 10: Thicknesses which are currently accessible for composite type embedding material

WARPAGE CONSIDERATIONS AND SIMULATION

In addition to the already mentioned advantages of such composite materials, there emerge some interesting possibilities. This is because the reinforced layer and the embedding layer can in principle be tuned independently according to technical requirements. For example the

ubiquitous problem of warpage might be tackled in a novel way. In order to be able to better understand which factors have the largest influence on warpage, a more detailed study has been started.

The reinforced layer and the embedding layer can have quite different physical properties, e. g. in terms of CTE, modulus, and glass transition temperature (T_g). The hypothesis to be tested is that warpage for a given design is minimized under the following conditions: The reinforced layer having a high Young's modulus and a low CTE, and the embedding layer having at least a rather low modulus, ideally in combination with a low CTE. This would allow the embedding resin layer to take up whatever stress might be formed during the different process steps such as vacuum pressing, curing, cooling, soldering etc. This is illustrated in Figure 11.

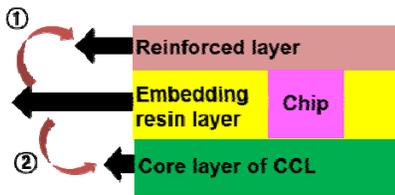


Fig. 11: Compensation of the CTE mismatch between the core material and the reinforced layer by the embedding resin having a low modulus

Warpage after pressing and curing and the evaluation of the significance of the applied finite element method (FEM) itself were to be evaluated first. Therefore the warpage predicted by the FEM has to be compared with the actual warpage determined on physical samples.

The mechanical analysis (MA) or the technology of thermal mechanically coupled analysis (TMCA) was applied to cured materials in the field of PCB technology in the past^[14]. However, in this study we wanted to use FEM to calculate the warpage taking into account the changing physical properties of the resin during the curing cycle. The physical properties which were determined for each resin type are summarized in Figure 12.

The test layout is shown in Figure 12. It has an array of chip dummies placed on a low CTE copper clad laminate having a thickness of 40 µm. The dimension of the dummies is 2.5 mm x 2.5 mm x 0.06 mm, the distance between the dies being 1.2 mm.

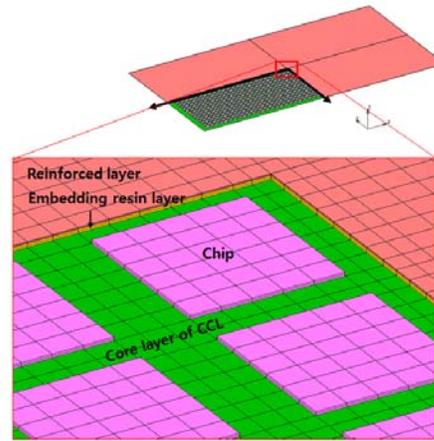


Fig. 12: Layout of the test design

In order to test the utility of the simulation, physical test boards will be built using the same resins the properties of which were used in the simulation. The three different resins have different moduli, CTE, cure shrinkage, and T_g. The glass fabric used in the reinforced layer was in all cases 1027 glass type (layer thickness 30 µm). The thickness of the embedding layer was 60 µm in all cases. The material properties of the embedding resin layer were measured for each resin formulation over the range of the entire press cycle which is summarized in Figure 13.

<i>Reinforced layer with 1027 glass</i>	
Modulus / [GPa]	Measured on cured sample by DMA (tensile mode)
CTE / [ppm/K]	Measured on cured sample by TMA
<i>Embedding resin layer</i>	
Heat conductivity / [W/mK]	Measured on the cured sample
Modulus / [GPa]	Determined by rheometer over the entire curing cycle starting with uncured resin
Shrinkage / [%]	Determined by volume change over the entire curing cycle starting with uncured resin

Fig. 13: Measured physical properties which were determined of three different resin

After establishing the principal capability of this approach, further simulation work will be carried out in order to estimate the warpage after other process steps like soldering and the long term reliability of a given composition of the composite material.

SUMMARY

A solvent free coating process allows for the production of composite materials with relatively thick resin layers which can be used for embedding of structures of various height and density. The application process is as easy as the use of an RCC and uses the infrastructure which is already available in PCB shops. Inherently there is no risk of glass fabric protrusion. The thickness distribution after press curing is excellent which will allow for reliable laser drilling of the microvias and therefore better yield of the overall production sequence. The modular approach of two distinct layers within the composite material allows in principle the

adaptation of each layer in order to reduce technical issues like warpage. Theoretical and practical work to prove this concept are under way.

Future improvements will include resin compositions having higher thermal conductivity, the extension of the current maximum thickness of the embedding layer, and low profile substrate foils which would allow for finer pattern beyond the current MSAP capability.

CONCLUSIONS

New material types can help to overcome some of the challenges of embedding technologies. We presented a type of composite resin material consisting of two distinct dielectric layers which are attached to a carrier foil. In a solvent free manufacturing, ultrathin glass fabrics can be easily employed and relatively thick resin layers for embedding can be created. Such a material combines the advantages of a prepreg (mechanical stability) with the advantages of an RCC (encapsulation properties). The thickness distribution above the dies is excellent which is important for reliable laser drilling processes.

A study was initiated in which the warpage is to be predicted for a defined chip layout and a defined set of material properties. The results of this investigation might allow to minimize warpage for a given layout by adjusting the material properties of the individual layers of the composite.

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