DESIGN FOR MANUFACTURE AND TEST USING THERMAL CYCLING UNDER BIAS TO MEASURE ELECTROCHEMICAL RELIABILITY ON BOTTOM TERMINATED COMPONENTS

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ABSTRACT
There are many factors contributing to electrochemical failures on electronic devices including pitch, electrical field, ionic contamination and environmental conditions. Each of these factors is dependent on the installation location, with exposure to varying temperatures and humidity.

The interactions of all these factors are quite complex, and being able to predict potential electrochemical failures is challenging. A series of detection and preventive measures from the qualification of solder pastes to controlling the ionic contamination levels of the materials in production is needed.

The purpose of this research is to characterize this problem by varying humidity and temperature conditions. Humid heat simulates the thermal load of the components under test at high humidity levels with cyclic temperature conditions. Condensation tests verify the design, materials, and remaining electronic circuit residues' resistance to moisture.

The test methodology used for this research study will subject the test cards to humid heat and cyclic temperatures with frost conditions. The harsh environment simulates the thermal load including frost cycling to induce low dewing point conditions through cyclic temperature changes at high humidity. Humid environments challenge no-clean electronics and the basis for detecting electrochemical robustness at various points during the design validation testing.

INTRODUCTION
Highly dense interconnections require increased functionality, reduced power consumption, and low cost. Electronic hardware requires more complex component technology. Miniaturization places new challenges on the electronic assembly. These technological challenges need to be considered in the first stages of the product development life cycle.

Designing hardware for electrochemical reliability is paramount due to the need for devices to perform on demand. Along with these technological challenges, electronic systems are increasingly exposed to harsh environments[1]. Smaller component pad to pad gap designs reduces the insulation distance between exposed metal, which requires closer scrutiny of the circuit design for trapping process residues. Additional monitoring and control of flux residues in production are needed along with a focus on validation testing to mitigate risks of electrochemical migration.

The circuit design must consider all required clearances with the relevant risk assessments understood. Sensitive components such as the QFN (Bottom Terminated Components) can trap active residues under the bottom termination[2]. PCB board designs that provide outgassing channels can significantly reduce the electrochemical migration risks. As there is a reduced inspection and test capability within the miniaturized structure, it is crucial to know the weakness of components, processes, and designs.

Failing early and learning from these failures is a must for HDI and electronic circuit card miniaturization. Understanding all material behavior is critical. The complexity of electronic faults and the influence of random variation in materials and or process parameters can result in quite complex failure modes[3].

Design for Manufacture and Test
The technological challenges of reduced insulation distances increase the importance of cleanliness and the use of no-clean soldering materials[3]. For leadless, area array, and bottom terminated packages, contamination control is critical to understanding cleanliness factors. Surface Insulation Resistance testing before and after reflow soldering can provide invaluable information on the process[4]. With the increased population of components, PCB board design needs consideration for achieving the proper thermal load to improve the decomposition of flux activators. Characterizing insulation resistance provides a critical understanding of contamination control.

It is essential to identify those risk components that are susceptible to trapping flux residues due to high I/O and low standoff gaps. With the increased component population with more hidden terminations, inspection is significantly impeded[5]. The inerent properties/risks for the more sensitive (BTC style) components need a comprehensive study to understand electrochemical behavior. This is further complicated with a double-sided population of components as well as the impact of multiple soldering operations.

The effect of miniaturization can be compounded with the introduction of Microvia technology, which is needed to facilitate higher density routing[3]. Microvia failures have become more and

more prevalent in highly dense circuit designs. Many Microvia defects are incidental from a complicated process and involve contaminations or blockage of flux outgassing channels. The critical interconnection defects are mainly associated with manufacturing / fabrication issues with detection dependent on electrical failure that may only become evident after operating in a temperature cycling environment

Design for Miniaturization

Designing for miniaturization requires test vehicles that simulate production hardware[6]. Surface Insulation Testing is needed to quantify and understand the physics of failure. It is important to understand sensitive components throughout the new product development process to determine design rules. The technological constraints require detailed assessment and understanding of a multitude of variables/factors.

The demand for the components and materials requires a close relationship with suppliers to understand the capability of components in a miniaturized electronics assembly. The sharing of experience and knowledge within numerous stakeholders is critical. Reviewing and assessing these challenging factors, with the required level of risk assessment and mitigation becomes part of the evolution of designing miniaturized electronic assemblies that meet the reliability objectives of today.

Learning the capability of process parameters, upgrading equipment, and their fine-tuning increases the capacity for miniaturization. Through multidisciplinary teams employing comprehensive Design for Manufacturing and Test programs with Design Reviews at the critical points of the product development can deliver robust miniaturization designs that meet the designers in use environment design objectives[3].

Class 3 Industries

Due to the challenging environmental operating conditions of Class 3 industries, the presence of ionic contaminants requires specialized monitoring. Identifying the types of contaminants and their source, as well as establishing the design susceptibility to the associated failure mechanisms, is critical at the earliest stages of the design lifecycle[3].

Each material introduces different contaminants, and the manufacturing process further influences the contaminants on electronic assemblies. To mitigate the risk of ionic contamination that can impact the reliability of the assembly, a series of qualification, validation, verification, process monitoring and controls employed throughout the product manufacturing lifecycle are required.

Failure Modes

The most dominant and known failure type is the electrochemical metal migration failure characterized by the growth of conductive metal filaments between potentially biased metal surfaces in the presence of an electrolytic solution (Figure 1)[7]. Ionic contaminants readily dissolve in water. When electronics are exposed to humid conditions, ionic residues dissolved in water mobilize metal oxides. This electrolytic solution allows the positively charged metal ions to migrate from the anode to the cathode. These dendritic growth fragments (tree-like structures) result in leakage currents, which can cause intermittent failures.

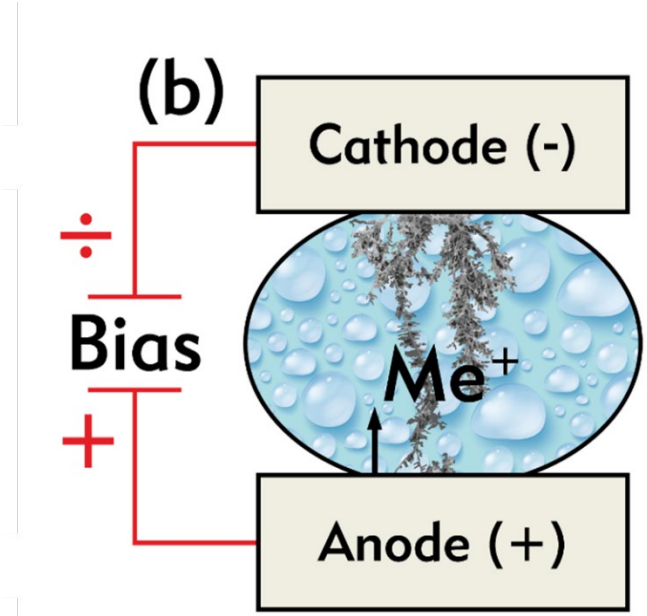


Figure 1: Electrochemical Cell

Within uncontrolled environments, a significant contributor to electrochemical related No-Fault-Found returns is Leakage Current failures. Leakage current failures depend on the humidity levels, presence of ionic contaminants, and potential bias between metal interconnects on an electronic circuit. The characteristic corrosion failure is not always evident on the surface of the PCBA. This type of failure is difficult to isolate as the failure may be present as an initial interruption to functionality without further recurrence when returned for debugging analysis. The electrochemical event may have exhausted the level of ionic contaminants and it is difficult to recreate the encountered real-world operation levels during debugging.

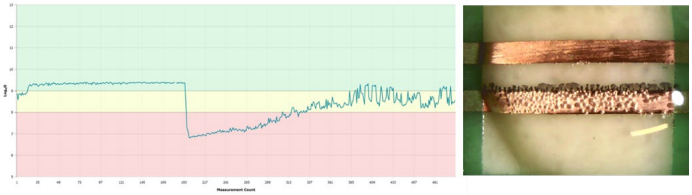


Figure 2: Leakage Currents resulting in No-Fault Failures

Isolating the root cause of leakage current failures is one of the most challenging Validation Test fails or Warranty Returns that can consume significant resources and costs to analyze. It is critical to isolate and identify the origin of all ionic contaminants during Failure Analysis.

Validation Testing

To mitigate the risk of electrochemical failures, there are various validation tests with thermal load and humidity/condensation environmental test conditions that attempt to recreate the worst operating conditions. Humid heat is effective at verifying the resistance to corrosion, migration, and electrochemical migration. Humid heat, along with cyclic temperature cycling simulates the thermal load of the module at high humidity levels. Condensation tests verify the design, materials and remaining electronic circuit process residues resistance to condensation conditions.

Humid Heat, cyclic (with frost) simulates the thermal load including frost cycling to induce low dew point conditions through cyclic temperature changes at high humidities during operation[5]. This is challenging for No-Clean electronics and the basis for the overcurrent failures. Overcurrent events tend to occur at low dew point condensation.

The QFN component represents one of the toughest cleaning challenges. The standoff gap is typically less than 50µms. During reflow, outgassing channels can become blocked with flux residues. The activity of the flux residue is at high risk for leakage currents. The objective of this research is to evaluate four PCB board design variations by stressing the QFN components using thermal cycling within cold frost conditions to hot humid conditions (Figure 3). The SIR test board is comprised of four Channels using a different PCB board design.

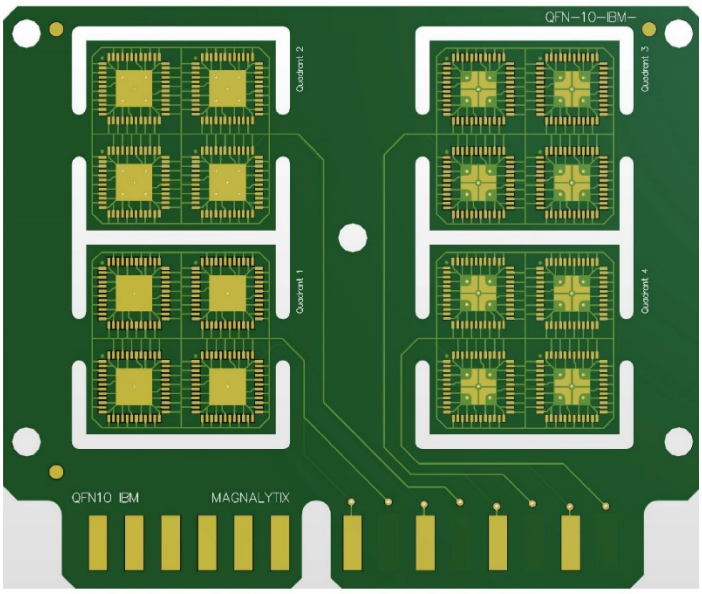


Figure 3: QFN Test Vehicle Design

Channel A [Quadrant 1] design features

- Open Copper
- Ganged I/O (No-Solder Mask)
- No thermal vias placed into the thermal pad

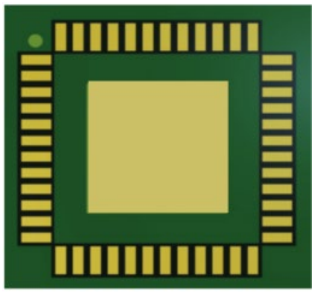


Figure 4: QFN Open Copper Design with Ganged I/O

The open copper design has no outgassing vias. During reflow, flux residues from the center lug can create large lake voids within the center lug and result in heavy flux residues at the outer center lug peripheral. The ganged I/O (no-solder mask) next to the signal pins does provide improved outgassing at the signal pin region.

Channel B [Quadrant 2]

- Open Copper
- Singulated I/O (Non-Solder Mask Defined)
- No thermal vias placed into the thermal pad

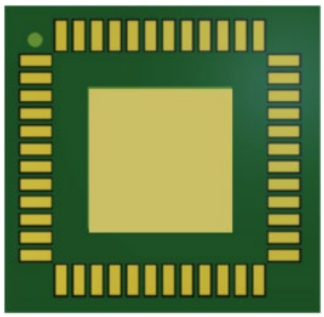


Figure 5: QFN Open Copper Design with Singulated I/O

The open copper design has no outgassing vias. During reflow, flux residues from the center lug can create large lake voids within the center lug and result in heavy flux residues at the outer center lug peripheral. The singulated I/O (non-solder mask defined) at the signal pin region can prevent outgassing at the signal pin region.

Channel C [Quadrant 3]

- SMD Thermal Pad
- Ganged I/O
- Encroached Vias
- 12-mil thermal vias within a solder mask web

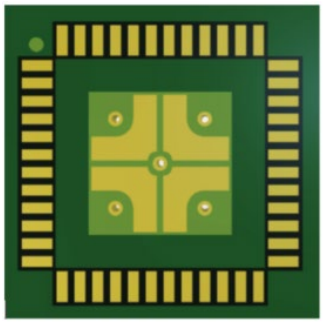


Figure 6: Solder Mask Defined Encroach Vias with Ganged I/O

The thermal lug region is designed to allow flux to properly outgass during reflow. Solder mask is applied to prevent solder from wetting and filling the via holes. The encroached plated via diameter is 12 mils. Five encroached vias are placed within the center lug at the corners and one in the center. The ganged I/O within the signal pin region has no solder mask. This design is thought to improve insulation since the flux activators have a channel to decompose during reflow.

Channel D [Quadrant 4]

- SMD Thermal Pad
- Singulated I/O
- Encroached Vias
- 12-mil thermal vias within a solder mask web

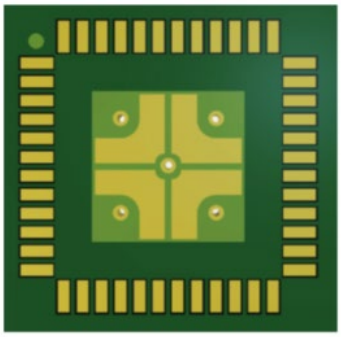


Figure 7: Solder Mask Defined Encroach Vias with Singulated I/O

The thermal lug region is designed to allow flux to properly outgass during reflow. Solder mask is applied to prevent solder from wetting and filling the via holes. The encroached plated via diameter is 12 mils. Five encroached vias are placed within the center lug at the corners and one in the center. The singulated I/O within the signal pin region is non solder mask defined. This design can potentially reduce insulation since the flux residue tends to bridge the signal pins. This condition increases cleaning time and can prevent decomposition of flux activators during reflow.

Experimental

1. Test Boards build with No-Clean SAC 305 solder paste
2. 4-Cleaning conditions
    a. No-cleaning
    b. Inline cleaned @ 2FPM
    c. Inline cleaned @ 1 FPM
    d. Inline cleaned @ 0.5 FPM
3. Stage 1: SIR test at 40°C/90% RH @ 3 V Bias for 72-hours
4. Stage 2: SIR test - Thermal Cycling at -40°C to 40°C / 90%RH @ 5V Bias for 168-Hours
5. Stage 3: SIR test at 40°C/90% RH @ 5V Bias for 72-hours after Thermal Cycle Testing
6. Two boards per condition were processed

What is a "Good" SIR Number

When viewing SIR data, a common question asked is, "what is a good or acceptable number"? That is a difficult question to answer as there is no single number determined to divide acceptable from unacceptable performance, and since SIR test data is also dependent on the geometry of the test electrodes, the data will vary by the test pattern[6]. The chart below records the insulation resistance values in LogOhms on the Y-axis and the number of Measurement Sets on the X-axis. IPC committees have generally agreed that values above 8 LogOhms is considered acceptable performance.

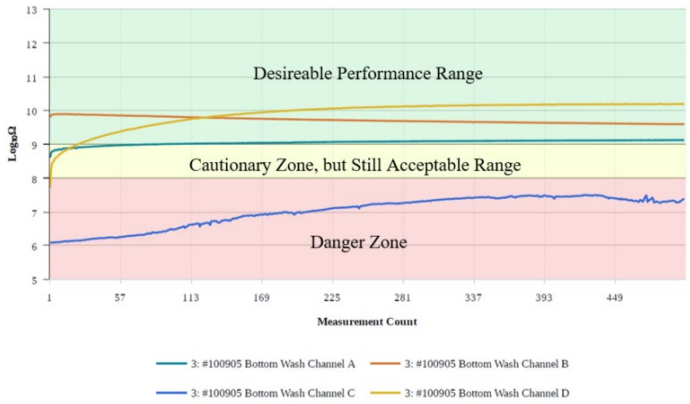


Figure 8: Danger Zone below 8 LogΩs / Cautionary Zone between 8 to 9 Log Ωs / Desirable Performance Zone above 9 LogΩs

DATA FINDINGS

Channel A: At the Beginning of the Test

- Open Copper / Ganged I/O
- 72 hours @ 40°C/90%RH/ 5V

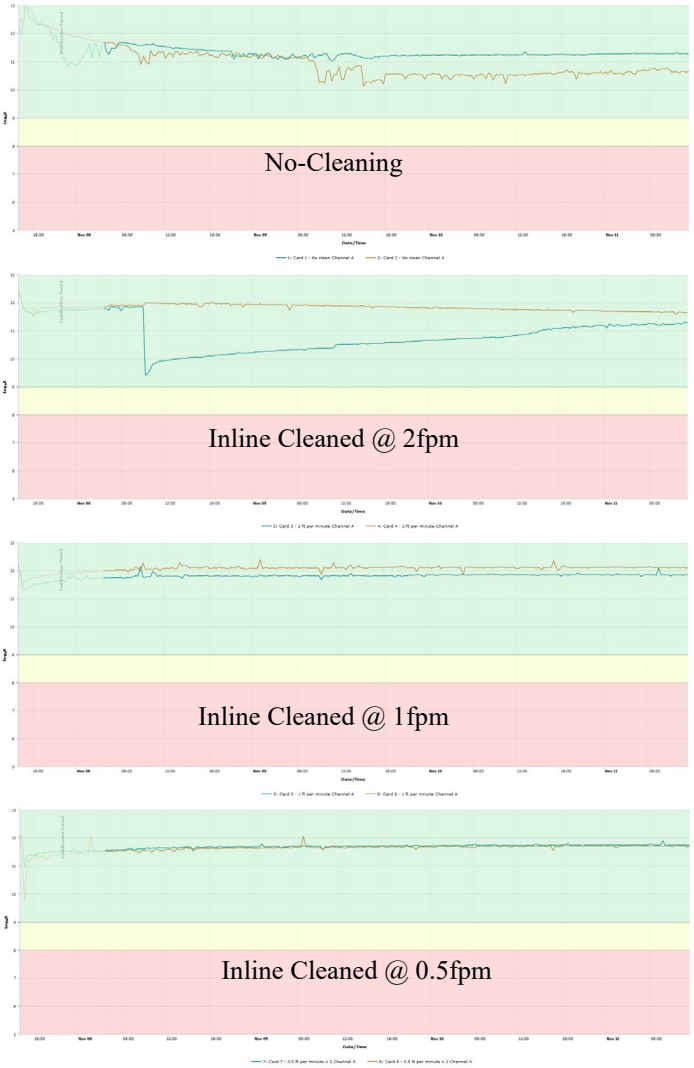


Figure 9: Channel A SIR @ 40°C / 90% RH / 5V for 72-hours

The inline cleaned boards at 0.5 fpm and 1.0 fpm SIR values exceeded 11 LogΩs. Longer dwell time in cleaning solution

resulted in higher more stable SIR readings as evidenced by 1.0 fpm / .5 fpm vs. 2.0 fpm / no clean. The values were stable. One of the inline cleaned boards at 2 fpm had a channel which dropped and then slowly recovered. This is an indication of partially cleaned flux residue. The not-cleaned boards performed well but did show some ionic movement during the test period.

Following the 72-hour SIR test, the boards were thermal cycled at 40°C / 90% RH / 5 V for one hour followed by a reduction of temperature to - 40°C / 90% RH / 5 V for one hour. The cyclic temperatures were changed each hour for 168 hours.

Channel A: Open Copper / Ganged I/O

- Thermal Cycling @ -40°C to 40°C/ /90%RH/ 5V/ 1-hour cycled / 168-hours

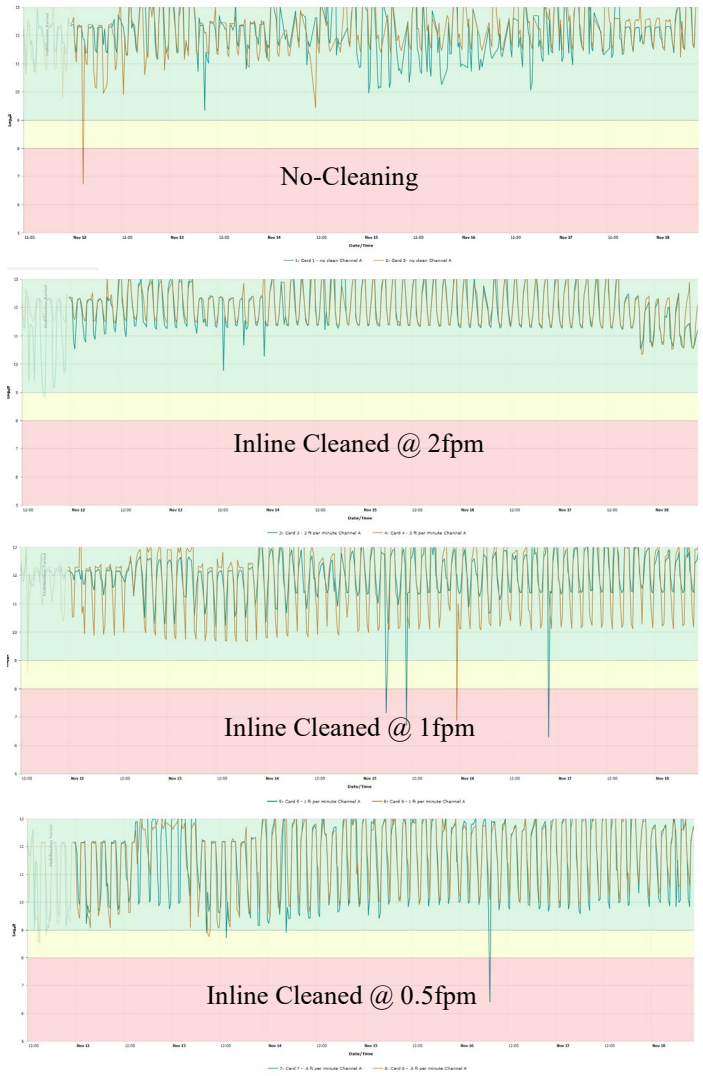


Figure 10: Channel A Thermal Cycling for 168-hours

The insulation resistance values varied based on the temperature condition. During the -40°C condition, insulation resistance rose. As the temperature was increased from -40°C to 40°C, insulation resistance declined by 3-4 decades. One of the Non-Cleaned boards spiked into the danger zone but quickly recovered. The inline cleaned board @ 2 fpm was the most stable of the boards tested. The 1 fpm and 0.5 fpm exhibited a larger decline between the cyclic conditions with some spikes into the danger zones. The data findings can be summarized as follows:

1. Channel A design was very consistent over all 4 cleaning approaches as measured by SIR
2. Channel A no clean / 2.0 fpm had higher SIR levels and stability vs. 1.0 fpm / .5 fpm cleaning time
3. 1.0 fpm / .5 fpm cleaning time test vehicles showed greater swing SIR values as defined from high to low
4. In temperature cycling environments with frost / condensation events leaving flux residue between adjacent pins and grounds aided in the SIR results over a more cleaned component state
5. In theory – more cleaning time allowed for the condensation to penetrate underneath the device and reduce the SIR value during warm temperature occureneces where there can be more ionic movement

Following the cyclic testing, the boards were tested at 40°C / 90% RH / 5V for 72-hours.

Channel A: At the end of the test

- Open Copper / Ganged I/O
- 72 hours @ 40°C/90%RH/ 5V

Figure 11: Channel A at 40°C / 90% RH / 5 V for 72-hours

Following cyclic testing, each of the boards tested shows some ionic movement. All boards conditions were in the desireable performance range. The inlined cleaned board at 0.5 fpm has some ionic movement on one of the boards. That board recovered with

the insulation resistance being stable over the remainder of the test period. The data findings can be summarized as follows:

1. All 4 cleaning states produced passing results with a 10 log ohm or higher SIR
2. Longer dwell time in cleaning solution resulted in higher more stable SIR readings as evidenced by 1.0 fpm / .5 fpm vs. 2.0 fpm / no clean
3. SIR results in log 10 to 11 is considered very good results when compared to an industry floor of log 8 plus
4. Post Temp Cycling SIR TESTING 40 / 90 % RH showed some variability in the early testing before settling into a steady run average over time
5. 5 Pre and Post SIR Testing showed very similar results

Channel B: At the beginning of the test

- Open Copper
- Singulated I/O (Non-Solder Mask Defined)
- 72 hours @ 40°C/90%RH/ 5V

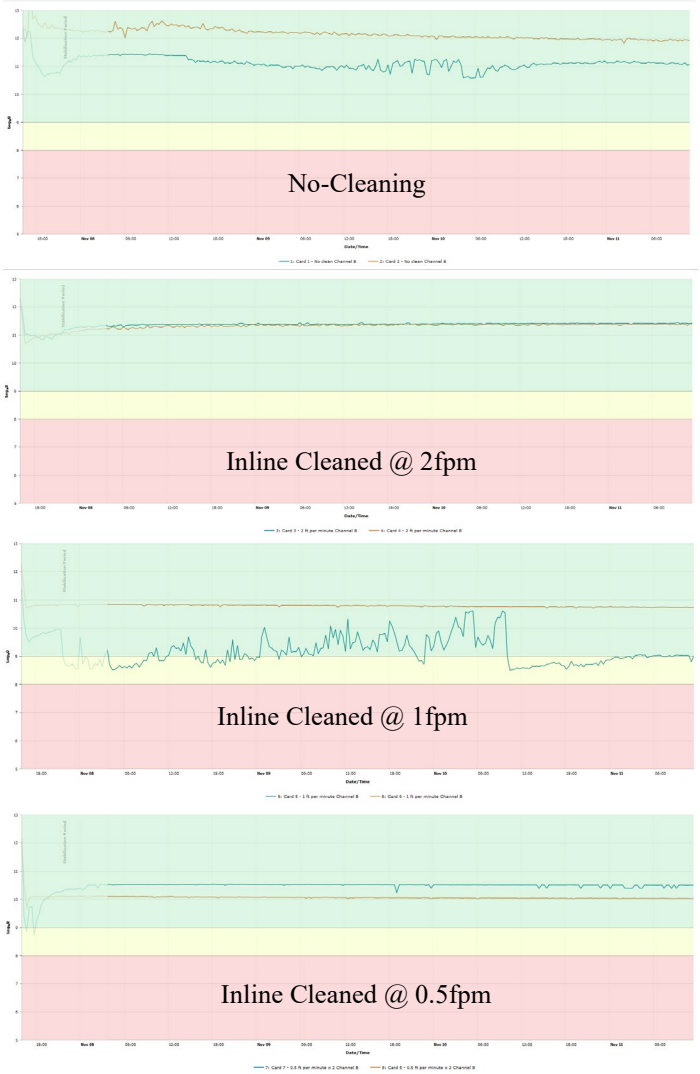


Figure 12: Channel B SIR @ 40°C / 90% RH / 5V for 72-hours

With the exception of one of the boards cleaned at 1 fpm, all boards were fairly stable and performed well over the first 72-hours @ 40° / 90% RH / 5V. One of the boards cleaned at 1 fpm showed evidence of leakage currents. The data findings can be summarized as follows:

1. All 4 cleaning states produced similar results with an 11 log ohm average SIR for no –clean and 2.0 fpm and log 10 average for .5 fpm and test card 6 with one anamoly being card 5 which avg. log 9
2. Lower dwell time in cleaning solution resulted in higher more stable SIR readings as evidenced by no –clean / 2.0 fpm vs. 1.0 fpm / .5 fpm
3. SIR results in log 10 to 11 is considered very good results when compared to an industry floor of log 8 plus

Following the 72-hour SIR test, the boards were thermal cycled at 40°C / 90% RH / 5 V for one hour followed by a reduction of temperature to - 40°C / 90% RH / 5 V for one hour. The cyclic temperatures were changed each hour for 168 hours.

Channel B: Open Copper / Singulated I/O

- Thermal Cycling @ -40°C to 40°C/ /90%RH/ 5V/ 1-hour cycled / 168-hours

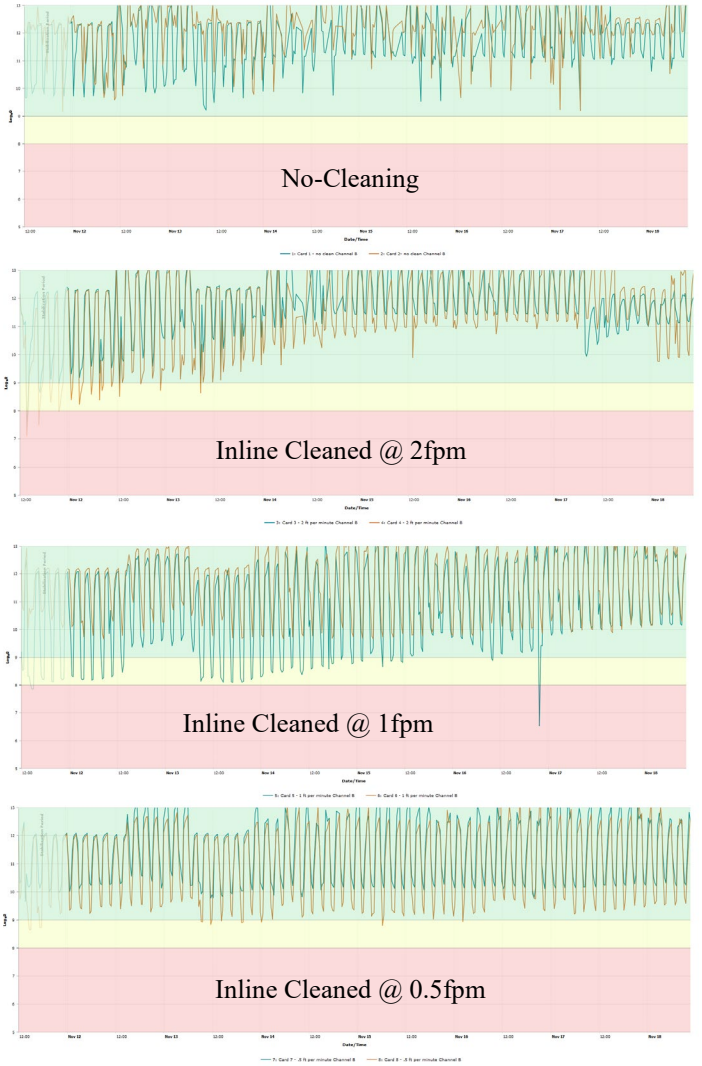


Figure 13: Channel B at 40°C / 90% RH / 5 V for 72-hours

The insulation resistance values varied based on the temperature condition. During the -40°C condition, insulation resistance rose. As the temperature was increased from -40°C to 40°C, insulation resistance declined from 3-4 decades. The not cleaned board had more variability within the insulation resistance upper and downward movements. The 0.5 fpm and 1.0 fpm board had

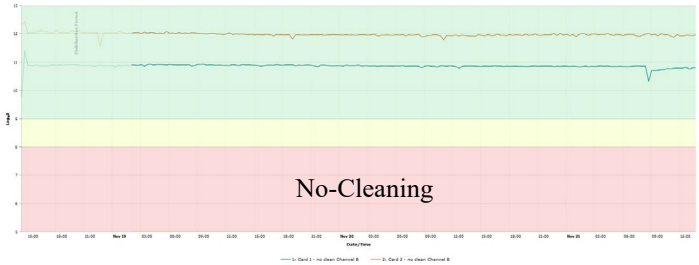
declined one to two decades lower than the not cleaned and 2 fpm cleaned boards. The data findings can be summarized as follows:

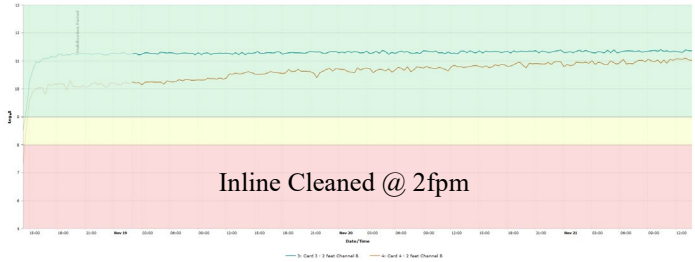
1. Channel B design was very consistent over all 4 cleaning approaches as measured by SIR
2. Channel B no clean / 2.0 fpm had higher SIR levels and stability vs. 1.0 fpm / .5 fpm cleaning time
3. 1.0 fpm / .5 fpm cleaning time test vehicles showed greater swing SIR values as defined from high to low
4. In temperature cycling environments with frost / condensation events leaving flux residue between adjacent pins and grounds aided in the SIR results over a more cleaned component state
5. In theory – more cleaning time allowed for the condensation to penetrate underneath the device and reduce the SIR value during warm temperature occureneces where there can be more ionic movement

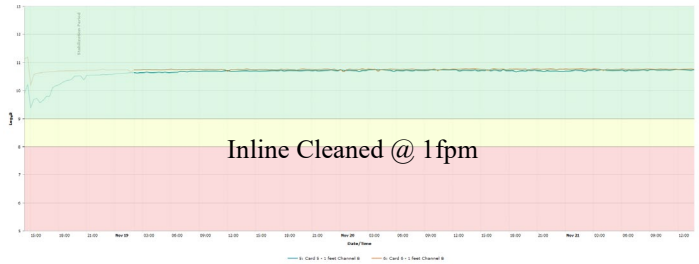
Following the cyclic testing, the boards were tested at 40°C / 90% RH / 5V for 72-hours.

Channel B: At the end of the test

- Open Copper
- Singulated I/O (Non-Solder Mask Defined)
- 72 hours @ 40°C/90%RH/ 5V







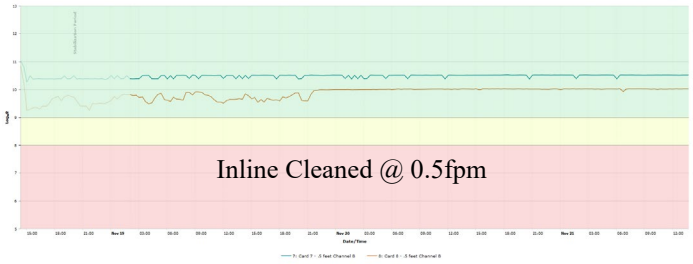


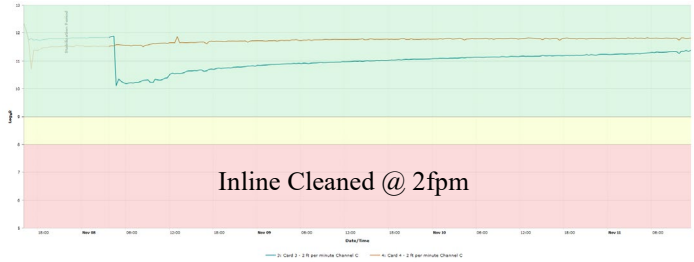
Figure 14: Channel B SIR @ 40°C / 90% RH / 5V for 72-hours

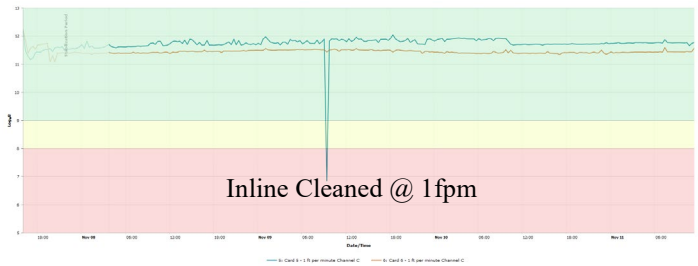
Following cyclic testing, all test conditions performed well. The data findings can be summarized as follows:

1. All 4 cleaning states produced passing results with a 10 log ohm or higher SIR
2. Lower dwell time in cleaning solution resulted in higher more stable SIR readings as evidenced by no-clean and 2.0 fpm vs. 1.0 fpm and .5 fpm
3. SIR results in log 10 to 11 is considered very good results when compared to an industry floor of log 8 plus
4. Post Temp Cycling SIR TESTING 40 / 90 % RH showed some variability in the early testing before settling into a steady run average over time
5. Pre and Post SIR Testing showed very similar results

Channel C at beginning of the test

- SMD Thermal Pad
- Ganged I/O
- Encroached Vias
- 12-mil thermal vias within a solder mask web
- 40°C /90%RH / 5V / 72-hours





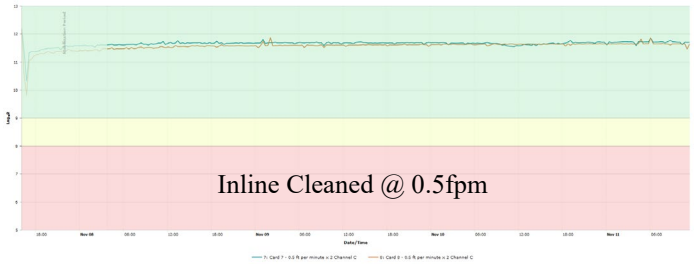


Figure 15: Channel C SIR @ 90% RH / 5V for 72-hours

The inline cleaned boards at 0.5 fpm SIR values exceeded 11 Log Ωs. One of the boards for the not-cleaned, 2 fpm and 1 fpm exhibited some downward spikes with full recovery. Overall, the values were stable. The major difference for this board design is the encroached outgassing vias within the thermal lug. The data findings can be summarized as follows:

1. All 4 cleaning states produced similar results with an 11 log ohm average SIR
2. Longer dwell time in cleaning solution resulted in higher more stable SIR readings as evidenced by 1.0 fpm / .5 fpm vs. 2.0 fpm / no - clean
3. SIR results in log 10 to 11 is considered very good results when compared to an industry floor of log 8 plus

Following the 72-hour SIR test, the boards were thermal cycled at 40°C / 90% RH / 5 V for one hour followed by a reduction of temperature to - 40°C / 90% RH / 5 V for one hour. The cyclic temperatures were changed each hour for 168 hours.

Channel C: Solder Mask with Encroached Vias using a Ganged I/O within the Signal Pin Region

- 12-mil thermal vias within a solder mask web
- Thermal Cycling @ -40°C to 40°C/ /90%RH/ 5V/ 1-hour cycled / 168-hours

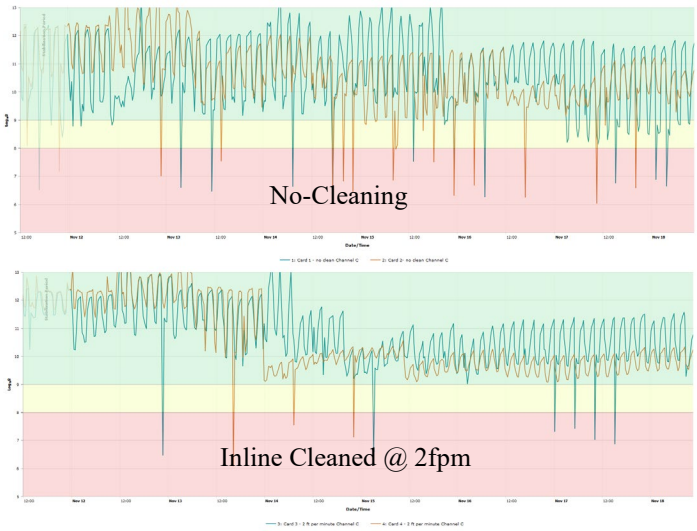


Figure 16: Channel C at 40°C / 90% RH / 5 V for 72-hours

The insulation resistance values varied in the range of 2-5 decades based on the temperature condition. The board design using the encroached vias in the thermal lug showed lower insulation resistance, more upward and downward movements, and higher variability than did the open copper designs. This result could be due to condensation under the bottom termination through the encroached vias. The reliability of this board design was not as good under the cyclic cycling conditions. The data findings can be summarized as follows:

1. Channel C design was very IN-consistent over all 4 cleaning approaches as measured by SIR with a number of events shorting out in log 6
2. Channel C no clean / 2.0 fpm had higher SIR levels vs. 1.0 fpm / .5 fpm cleaning time by 1 log ohm (log 12 vs log 11)
3. 1.0 fpm / .5 fpm cleaning time test vehicles showed greater swing SIR values as defined from high to low
4. In temperature cycling environments with frost / condensation events leaving flux residue between adjacent pins and grounds aided in the SIR results over a more cleaned component state
5. In theory – more cleaning time allowed for the condensation to penetrate underneath the device and reduce the SIR value during warm temperature occureneces where there can be more ionic movement
6. Designed Vias underneath the QFN device clearly allowed more moisture intrusion which impacted SIR results as evidenced by the number of events where SIR dropped down to log 6 region
7. Channel A and B design minus vias underneath the QFN device were more stable and consistent vs. Channel C

Following the cyclic testing, the boards were tested at 40°C / 90% RH / 5V for 72-hours.

Channel C at the end of the test

- SMD Thermal Pad
- Ganged I/O
- Encroached Vias
- 12-mil thermal vias within a solder mask web

- 40°C / 90%RH / 5V / 72-hours

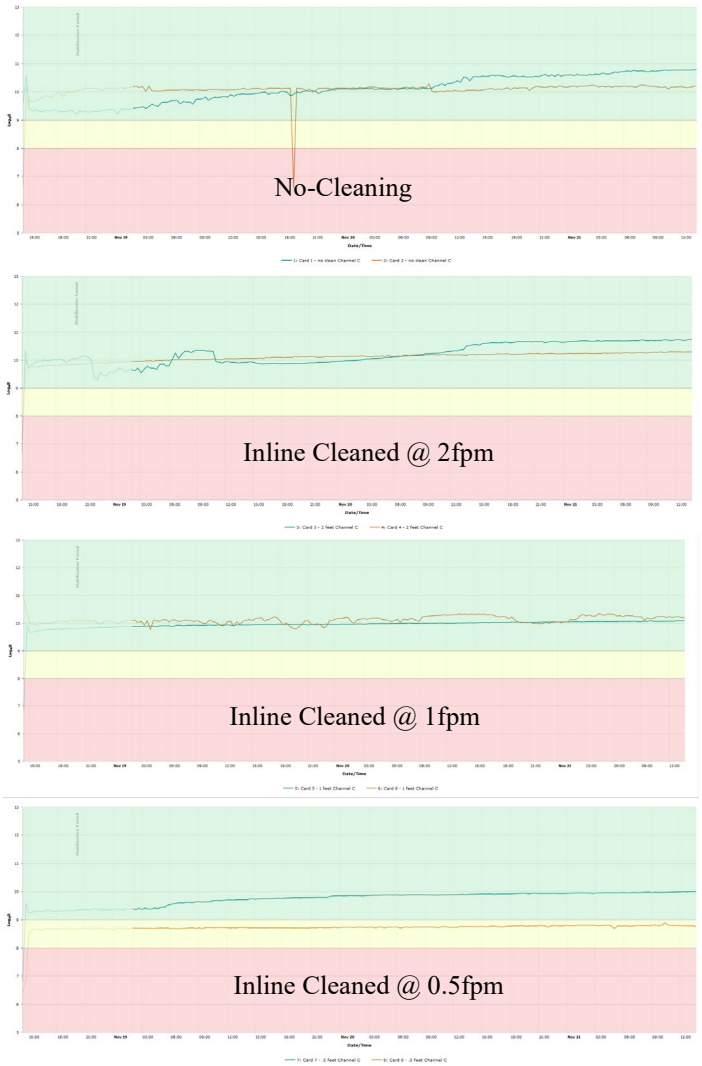


Figure 17: Channel C SIR @ 90% RH / 5V for 72-hours

Upon returning to 40°C / 90% RH / 5V for 72-hours, all the channels were much more stable. Ionic movement was minimal. This further indicates that moisture penetration into the encroached vias occurred during thermal cycling. The data findings can be summarized as follows:

1. All 4 cleaning states produced passing results with a 10 log ohm SIR
2. Lower dwell time in cleaning solution resulted in higher more stable SIR readings as evidenced by no-clean and 2.0 fpm vs. 1.0 fpm and .5 fpm
3. SIR results in log 10 is considered very good results when compared to an industry floor of log 8 plus
4. Post Temp Cycling SIR TESTING 40 / 90 % RH showed some variability in the early testing before settling into a steady run average over time
5. Pre and Post SIR Testing showed very DIFFERENT results with each cleaning speed being atleast 1 log ohm lower to 2 log ohm after temp cycling

Channel D at the beginning of the test

- SMD Thermal Pad
- Singulated I/O
- Encroached Vias
- 12-mil thermal vias within a solder mask web
- 40°C / 90%RH / 5V / 72-hours

Figure 18: Channel D SIR @ 90% RH / 5V for 72-hours

All boards, including the not-cleaned and cleaned boards were stable over the first 72-hours of testing. The singulated I/O at the signal pins using the encroached vias in the thermal lug found very consistent values. The data findings can be summarized as follows:

1. All 4 cleaning states produced similar results with a 10 log to 11 log ohm average SIR
2. Lower dwell time in cleaning solution resulted in higher more stable SIR readings as evidenced by no - clean / 2.0 fpm vs. 1.0 fpm / .5 fpm
3. SIR results in log 10 to 11 is considered very good results when compared to an industry floor of log 8 plus

Following the 72-hour SIR test, the boards were thermal cycled at 40°C / 90% RH / 5 V for one hour followed by a reduction of

temperature to - 40°C / 90% RH / 5 V for one hour. The cyclic temperatures were changed each hour for 168 hours.

Channel D Solder Mask with Encroached Vias using a Singulated I/O within the Signal Pin Region

- SMD Thermal Pad
- Singulated I/O
- Encroached Vias
- 12-mil thermal vias within a solder mask web
- Thermal Cycling @ -40°C to 40°C/ /90%RH/ 5V/ 1-hour cycled / 168-hours

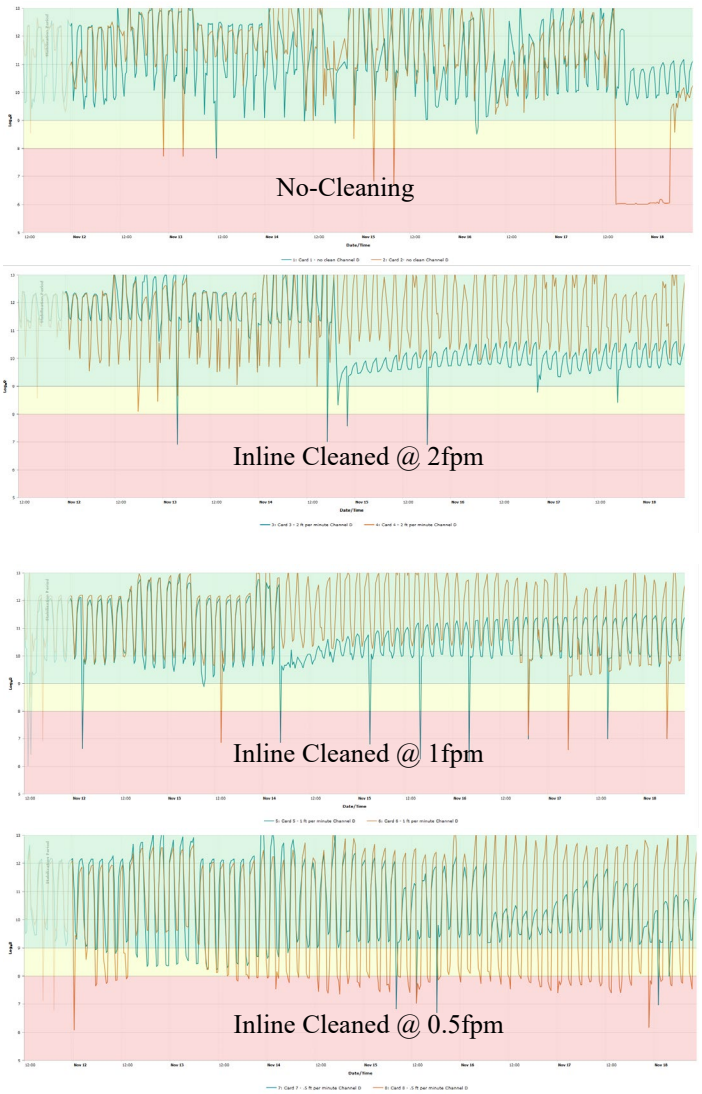


Figure 19: Channel D at 40°C / 90% RH / 5 V for 72-hours

Similar to the ganged I/O design with encroached vias, the insulation resistance values varied in the range of 2-5 decades based on the temperature condition. One of the not-cleaned boards developed a dead-short near the end of the 168-hour cyclic cycling test. This board design using the encroached vias in the thermal lug also showed lower insulation resistance, more upward and downward movements, and higher variability than did the open copper designs. This result could be due to condensation under the bottom termination through the encroached vias. The reliability of this board design was not as good under the cyclic cycling conditions. The data findings can be summarized as follows:

1. Channel D design was very IN-consistent over all 4 cleaning approaches as measured by SIR with a number of events shorting out in log 6
2. Channel D no clean / 2.0 fpm had higher SIR levels vs. 1.0 fpm / .5 fpm cleaning time by .5 to 1 log ohm
3. 1.0 fpm / .5 fpm cleaning time test vehicles showed greater swing SIR values as defined from high to low
4. In temperature cycling environments with frost / condensation events leaving flux residue between adjacent pins and grounds aided in the SIR results over a more cleaned component state
5. In theory – more cleaning time allowed for the condensation to penetrate underneath the device and reduce the SIR value during warm temperature occureneces where there can be more ionic movement
6. Designed Vias underneath the QFN device clearly allowed more moisture intrusion which impacted SIR results as evidenced by the number of events where SIR dropped down to log 6 and 7 region
7. Channel A and B design minus vias underneath the QFN device were more stable and consistent vs. Channel C and D that was designed with vias

Following the cyclic testing, the boards were tested at 40°C / 90% RH / 5V for 72-hours.

Channel D at the end of the test

- SMD Thermal Pad
- Singulated I/O
- Encroached Vias
- 12-mil thermal vias within a solder mask web
- 40°C / 90%RH / 5V / 72-hours

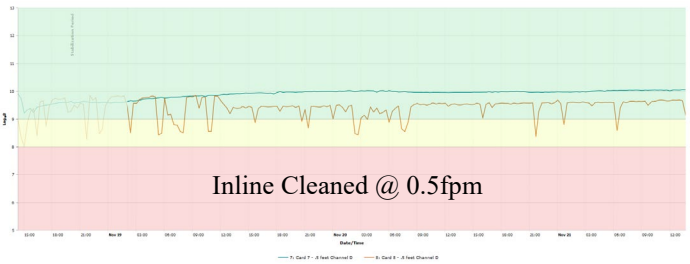


Figure 20: Channel D SIR @ 90% RH / 5V for 72-hours

Similar to the Channel C boards, following the cyclic testing, the channels returned to a stable condition. Only one board cleaned at 0.5 fpm showed variability. The data findings can summarized as follows:

1. All 4 cleaning states produced similar results with a 10 log ohm average SIR
2. Lower dwell time in cleaning solution resulted in higher more stable SIR readings as evidenced by no - clean / 2.0 fpm vs. 1.0 fpm / .5 fpm
3. SIR results in log 10 is considered very good results when compared to an industry floor of log 8 plus
4. .5 fpm test cards resulted in lowest Post Temp Cycle SIR test for 72 hours with test card 7 barely reaching log 10 and test card 8 log 9

Inferences and lessons learned

1. SIR results alone did not tell the whole story – All pre and post temp cycling SIR Testing showed acceptable SIR results from log 9 to log 11
2. Temperature cycling with frost / condensation events showed extreme environmental conditions and which pcb design rules and cleaning conditions worked best
3. Designed via structures work good for SIR test results when temperature cycling with condensation is not applied. Temperature cycling with condensation exposed a problem with exposed vias underneath BTC components whereby voids and moisture accumulation can occur is a problem for passing this test condition.
5. SIR testing combined with Temperature cycling with frost / condensation is an extreme accelerated test that exposes weaknesses in material choices – flux and process controls – outgassing and reflow conditions to aid in optimizing the cleanliness level underneath BTM components
4. SIR testing combined with Temperature cycling with frost / condensation is an extreme accelerated test that exposes weaknesses in PCB design configurations and layout rules
5. No – clean fluxes performed better than partially clean fluxes but fully cleaned fluxes .5 fpm showed better stability and repeatability on both test conditions
6. Future Test Doe –
    a. Post via fill encapsulation vs open via
    b. Underfill vs no underfill on BTC devices
    c. Expand the test card sample size in a double blind test

Concluding Remarks

The use of temperature cyclic with condensation is a unique test tool and protocol that is designed to put a number of variables into an accelerated format to find and uncover weaknesses in electronic assembly methods. This test is designed to find cleanliness issues as well as design issues and manufacturing process issues.

By using this multi variable test that uses both hot and cold thermal cycling to drive coefficient of thermal expansion (cte) (-40 to 40c) and the introduction of frost and condensation into the test protocol aids in ionic mobility and high humidity moisture ingression. These conditions aids in the dew point condensation and frost condition. This is an extreme accelerated test to uncover and find weaknesses in material choices, process control, process parameters, and circuit card layout design and component package choices.

This Particular test DOE exposed the problem with via structures underneath BTC (Bottom Terminated Components) by crating voids and blank space for frost and condensation to ingress into the area that we needed to be clean and minimize ionic movement and leakage currents. The idea of via structures for improving out gassing and minimizing unvolatized flux residues, which improves SIR results is quite proven as a good design rule. The vulnerability of ingression issues underneath BTC style components during thermal cyclic environments with frost and condensation shows the need for better test methodologies for design engineers to insure they address these potential failure modes in real fielded applications. This DOE was designed to explore the need to gather real test data and objective evidence to help develop new test protocols that better define BTC vulnerabilities and create a greater understanding of the variables that greatly impact BTC's.

SIR testing along with temperature cyclic testing with frost / condensation is a good tool in collecting beneficial data and objective evidence of what material sets, production parameters, and process control parameters, circuit design rules and component layout best practices to meet your fielded environmental objectives. SIR testing using specific real world components (SIR Designed test components) in a test environment and in different circuit/component layout designs allows for determining and finding the weakest link in your design and which design gives you the best results from an SIR cleanliness objective before testing it in the final layout configuration. The more testing and objective evidence one can perform at the development and design stage the better the final design will work in a real fielded state because of the lessons learned on the front end.

This DOE showed how SIR test data in a non - thermal cyclic state all passed with SIR readings in the Log 10 and 11 range but once thermal cyclic testing with frost and condensation started then downward spikes and a drop in SIR was seen on the different designed circuit pad and via structures. Depending on your fielded application the use of SIR alone and in conjunction with thermal cyclic testing may better prepare and prevent latent warranty issues in production.

Follow On Research

The test boards used for this research study will be microstructed to further understand material behavior. The goal is to improve understanding of the SIR testing for each of the board channels. The following test conditions will be conducted:

- Light microscope
- Electron microscope
- X-Ray spectroscopy
- Electron Diffraction

One of the aspects of this research is to identify leakage currents and electrochemical migration. In order to analyze and understand the SIR data findings we must be able to visualize the effects under the bottom terminations.

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