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DESIGN AND FABRICATION OF ULTRA-THIN FLEXIBLE SUBSTRATE

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ABSTRACT

We present the development of a flexible polyimide substrate that act as the conduit for power and signal transmission with the additional features of precise control of the metal trace geometries. Using microfabrication techniques, a metal trace is fabricated that possesses a flexible polyimide-based interconnection. The performance of the design was measured with multi-meter. The HFSS simulation result of copper-plated interconnection with a core thickness of 12 um has an impedance value of 50 ohm at 1 GHz. Investigated of microfabrication were performed using an energy-dispersive spectrometry (EDS) and Zygo Optical Profilometer in order to verify the visual aspects of the Cu interconnection, such as identification the elemental composition of materials, roughness and thickness. The experiment is conducted to study the effect of the process parameters on the Cu film surface properties. The results obtained in this work can be applied to the fabrication of flexible microelectronic devices.

Key words: 3D Integration, Flexible Polyimide Interposer (FPI), fine line wiring, energy-dispersive spectrometry (EDS).

INTRODUCTION

The industry market is now faced with the increasing importance of a new trend, "More than Moore" (MtM), where value-added applications are provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". Historically, Moore's law has been predicted that the number of components per chip would double every 12 months. Performance and productivity of microelectronics has been increased continuously over more than four decades due to the enormous advances in photolithography, wafer size, process technology, and device. This has led to the development of technologies that can lead to the ultra-miniaturization of electronic systems. However, the performance improvement gained in transistor scaling is insignificant compared to the negative effects of interconnect scaling. The delay of global interconnects increases with technology scaling. The ITRS roadmap predicts Three-dimensional (3D) integration as a key technique to overcome this so-called ''wiring crisis'' [1]. 3D technology, an alternative solution to the scaling problems, is a well-accepted approach for so-called ''More than Moore'' applications [2].

3D integration is an emerging technology that vertically stacks and interconnects multiple device layers. In the 3D integration, silicon interposer and Through-Silicon-Via (TSV) are primary enablers that can take full advantages of 3D ICs. 3D ICs with TSVs offer improved electrical performance due to the short interconnect between stacked ICs. 3D interposers based on silicon or glass substrate aim at replacing traditional printed circuit board (PCB) laminate or ceramic technologies for the sake of extreme miniaturization and performance. However, a silicon substrate cannot be utilized as a good medium for signal transmission since interconnects on the silicon substrate suffer from substrate losses caused by the penetration of the electric and magnetic field. Glass has many advantages as an interposer material over silicon; namely ultra-high resistivity and availability in thin and large sizes. Glass has been studied as an interposer material, mainly focusing on metalized through-glass-via (TGV) in thick glass substrates using laser ablation [3-6]. To implement 3D stacking technology as a low-cost and easy-to-use mounting method, a new interposer is necessary. The thin flexible PI films have desirable properties for use in the electrical and electronics industry because they are a group of good thermal stability, high flexibility, low dielectric constants, excellent mechanical strength, low loss tangent and electrical insulating properties [7-9]. Developments have lately been made with various embedding technologies, such as Chip-In-Polymer [10, 11], Chip-In-Substrate [12], or flexible bumped tape interposer (FBTI)[13]. The development of a flexible polyimide interposer (FPI) is reported in this study.

This study focuses on an approach based on the use of polyimide substrate for 2.5D/3D ultra-thin packaging applications. We present our investigations of the factors associated with fabrication of high-density Cu interconnect structures and Cu via using polyimide film and electroplated Cu conductor lines. We use a 3D-profilometer microscope for characterizing roughness and slope errors to determine the influence of each technological step on the surface quality.

DESIGN

3-D TSVs are incorporated into IC packages as a mean to interconnect two or more stacked die. In addition, a vias can go through the bulk silicon of the lower die to connect to the package substrate. A variation on this idea is the notion of 2.5-D, where devices are sitting side by side on a common interposer. This interposer can be used to fan out or reroute the electrical traces of a device while routing the traces to the package substrate below, connected by means of microbumps. For example, a silicon interposer can be placed between a die and an organic substrate. A silicon interposer has fine pitch interconnects on its top surface to connect with and redistribute signals from the die above. As shown in Figure 1, the interposer's interconnects redistribute signals to TSVs running downward through the interposer and connecting with the substrate. TSV interposers provide flexibility for the integration of die from different semiconductor technology nodes and deliver advantages in miniaturization, thermal performance and fine line/width spacing in a semiconductor package [14].

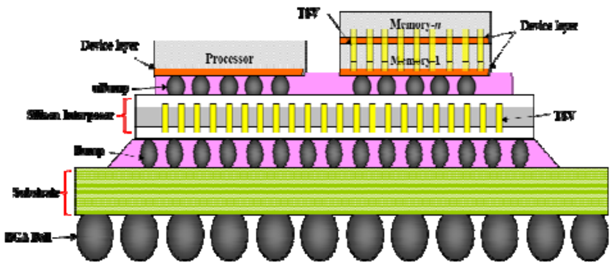
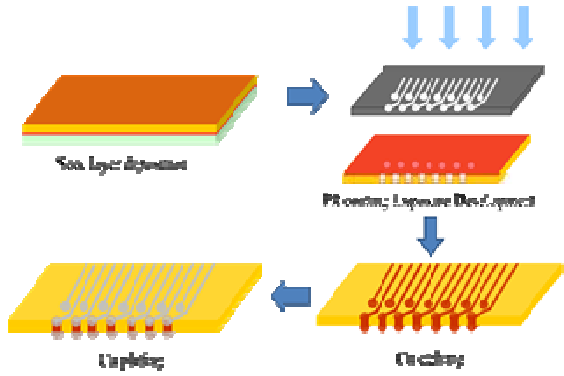


Figure 1. Schematic Drawing of 3D Stacking of the Silicon Interposer with TSV

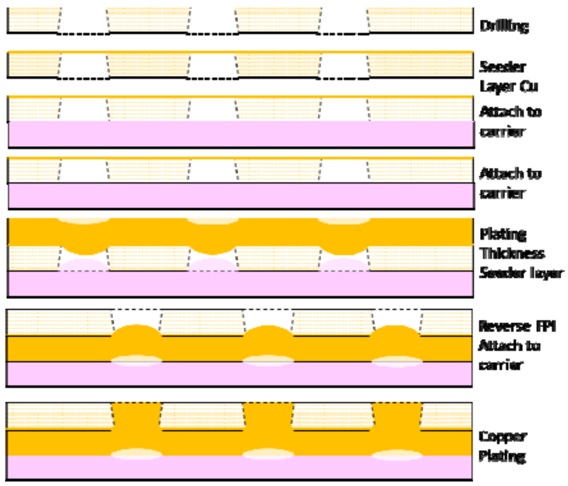
A construction of Cu fine pitch pattern on the FPI includes a PI base film, a seeder layer copper, and a layer of electrodeposited copper. The FPI was made using a copper-coated PI film composed of 12.5 µm of polymerized PI layer with a size 20 × 30 mm^2. The manufacture of these fine pitch patterns makes use of photolithographic techniques for fine pattern generation, continuous vacuum techniques for seeder layer, and special electrodeposition methods for copper build-up. The main experimental fabrication process of interposers is shown in Figure 2 (a) and (b).

A test pattern for further electroplating process was fabricated using standard photolithographic techniques. For the formation of the test pattern used in the electroplating of Cu, a seed layer was coated on the surface of the PI substrate by an evaporator. Before the experiment, the flexible substrates were baked in a hot plate for 10 minutes at 110 □ to remove any surface absorbed moisture. To start the fabrication process the PI substrate was ultrasonically cleaned by ethanol and then rinsed with DI water allowed by drying using nitrogen gas. The seed layer of 200nm Cu is deposited on a flexible substrate using a thermal-evaporation process, without using a catalyst or pre-deposited buffer layers. The substrates were spin-coated with a patterned layer of thick AZ4620 photoresist (AZ Electronic Materials). The PR of 6 µm was spun onto the substrate at 3000 rev. per min for 30s using a spinner. The substrate was then soft baked on an open hotplate at 90 ℃ for 3 minutes. The substrate was exposed with a dose of UV illumination of 350-450 nm wavelengths at 100mJ/cm2 intensity, using an M&R Nano Technology Co. AG350 Mask Aligner and Exposure System and a plastic mask. The mixture of AZ 400K and DI water (1:4) was used to develop the exposed pattern for about 5 minutes.

The samples were immersed in an activator for 1 min and cleaned with distilled water, nitric acid (3% in volume) and acetone. In the electroplating process, Cu was deposited by the direct current on the Cu/PI substrate in an electrolyte at the 25 ℃ and 50 ℃ temperatures. We used a commercial Cu sulfate solution from A Gold Jet Tech Inc. in Taiwan. The Cu electroplating bath includes electrolyte consisting of PTH-502A, 10% with H_2O and PTH-501B, 10% with H_2O. To obtain Cu layers with a 2~15 µm thickness, the current was varied in the range of 20~30 mA and the plating time was controlled in the range of 200~800 seconds.



(a)



(b)

Figure 2. Schematic Illustrations for the Fabrication Processes of a FPI (a) and Bottom-up Cu Electroplating Via Process (b)

Bottom-up Cu electroplating of via is proposed in this paper for high aspect ratio via filling [15]. The bottom electrode could be made by sputtering metals on polymer and then remove the polymer to form the film type bottom electrode. Many studies report bottom-up fill of Cu in electroplating baths using additives, but few reports about bottom-up fill of Cu in electroless plating solutions have been published [16]. It lost ground to electrolytic plating because of concerns due to hydrogen evolution, complexity in process control, low deposition rates, and potentially adverse environmental impact. They can be hampered by poor contacts to the surrounding layers and an incomplete fill. We used Cu electroforming method after the seeder layer formation by the heat evaporation. Figure 2 (b) illustrates the process flow chart of DC Cu electroforming vias after the FPI holes made by laser ablation process. Excellent selectivity is as expected within the whole FPI and all of vias are covered by electroforming Cu with good uniformity. Figure 3 shows the design of the interposer mask.

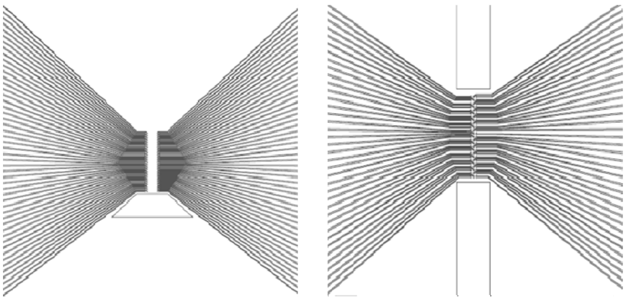


Figure 3. Illustrative Drawing of Two-layer Cu Interposer

To verify the FPI structures in Figure 2, we simulated the transmission coefficient (S21) of microstrip lines structures. The simulations are performed using an Ansoft's High Frequency Structure Simulator (HFSS). The FPI substrate used in the simulation has the same parameters as the Taiflex PI with a core thickness of 12.5 um, a dielectric constant of εr=3.4, and a loss tangent of 0.003. In general, two variables determine the characteristic impedance: line width and gap width. In the simulations, the width of the center metal trace in all the structures is 12 um. The reflection coefficients are reduced by -3 dB at 4.65 GHz under the 2.5 cm length of FPI interconnection as depicted in Figure 4.

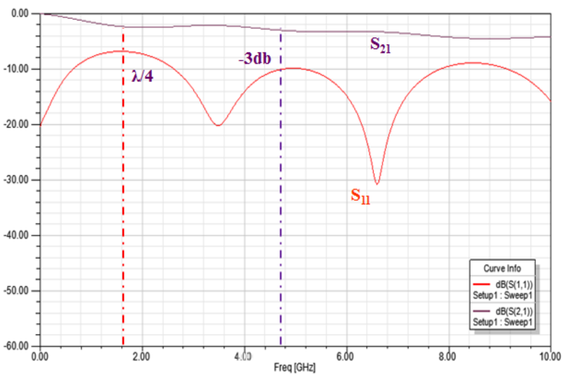
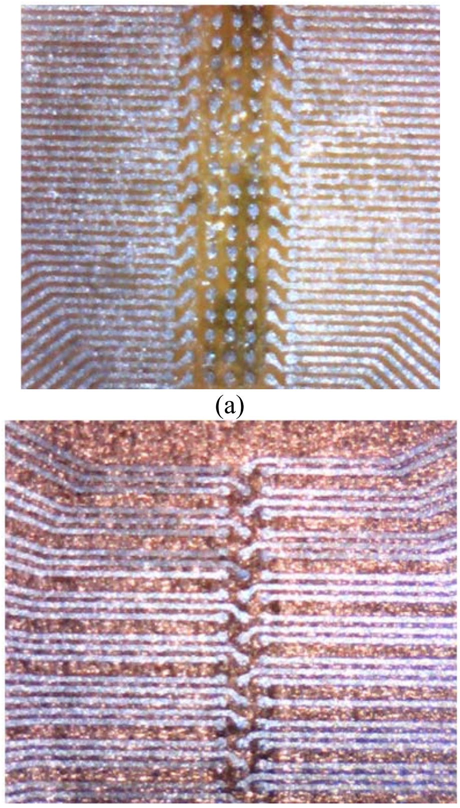


Figure 4. Simulation Results of the Frequency Dependent Scattering Parameters for the Structures deplicted in Figure 3

FABRICATION RESULTS

Electroplating Cu

Optical images of the Cu evaporation-coated PI surface after electroplating Cu deposited for different times were fabricated in Figure 5. The surface microstructure was observed using a Nikon Eclipse ME600 optical microscope (with a digital camera, Sony DFW-SW910), 2400× magnifications with attached image analysis software (Sony IIDC), after suitable calibration as shown in Figure 6(a). It can be seen that there were no voids at the wetting interface. The incorporation of Cu in the electroplated Cu surface was verified by the presence of the Cu peak in the EDS spectrum as indicated in Figure 6(b).

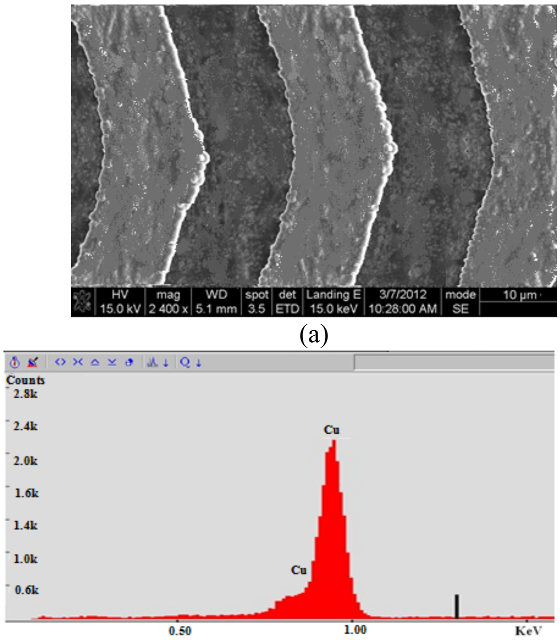


(a)

(b)

Figure 5. Optical Image of Fabrication Results for Top side(a) and Bottom Side(b)

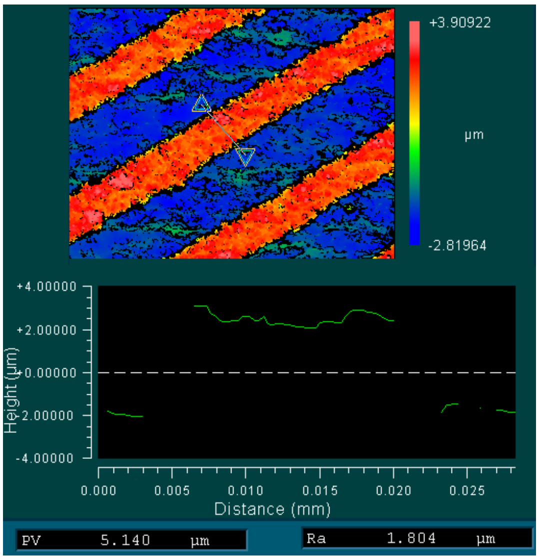
There are two parameters that must be adjusted in order to improve the uniformity of Cu: the current density and the temperature of the bath. The first test concerns the study of the variation in applied current value. The thickness of the Cu coatings deposited was determined by ZYGO NewView 7000 series 3D optical surface profilometer (Zygo Corporation). A 10* objective and 2*zoom were used for a lateral resolution of 1.12 nm. Various samples were measured to ensure that the images were representative of the trace surface. The profile result of FPI interconnection obtained by the proposed method is shown in Figure 7, where Peak to Valley Distance (PV) was found to be 5.140 um with a Ra Value as 1.804 um. The Cu thickness proved to be linear as a function of the deposition time with zero incubation time at 50 °C temperatures and the agitation speed of 50 rpm. Figure 8 shows the thickness and roughness of the plated FPI interconnection at room temperatures under 30mA of plating current. The Ra value of trace surface increased as the neutralization time increased and the Ra of the 800 seconds under 300mA current was 1.5 um.



(a)

(b)

Figure 6. SEM Image of the Surface of Interconnection-coated Copper at 2400× magnifications (a) and an EDS Spectrum on the Metal Trace (b)



(b)

Figure 7. Zygo 3D Surface Analysis of the FPI Sample. Peak to Valley Distance (PV) was Found to be 5.140 um and Ra Value was 1.804 um.

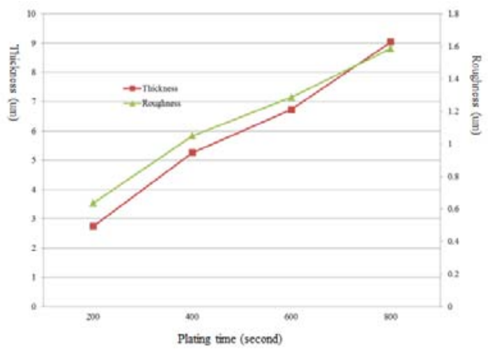


Figure 8. Variation of the Copper Thickness and Surface Roughness under 30mA of Plating Current

CONCLUSION

A fine pitch patterned processing sequence for the preparation of interposer used for 3D integration applications was developed and experimentally evaluated. The main features of this technology are the preparation of conductor lines on the FPI, which enable the chip connect to the interposer.

ACKNOWLEDGEMENT

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REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS) (2007) http://www.public.itrs.net.

[2] P. Garrow, C. Bower, P. Ramm, "Handbook of 3D Integration", Wiley-VCH, 2008 (ISBN: 978-3-527-32034-9).

[3] L. Brusberg, H. Schröder, M.Töpper,and H. Reichl, "Photonic System-in-Package technologies using thin glass substrates," in Electronics Packaging Technology Conference, 2009. EPTC '09. 11th, 2009, pp. 930-935.

[4] H. Schröder, L. Brusberg, R. Erxleben, I. Ndip, M. Töpper, NF Nissen, H. Reichl, "glassPack; A 3D glass based interposer concept for SiP with integrated optical interconnects," in Electronic Components and Technology Conference (ECTC), 2010, pp. 1647-1652.

[5] L. Brusberg, H. Schröder, N. Arndt-Staufenbiel, M. Wiemer,, "3-D Thin film interposer based on TGV (Through Glass Vias): An alternative to Siinterposer," in Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th, 2010, pp. 66-73.

[6] L. Brusberg, H. Schröder, M. Töpper, N. Arndt-Staufenbiel, J. Röder, M. Lutz, H. Reichl,, "Thin glass based packaging technologies for optoelectronic modules," in Electronic Components and Technology Conference (ECTC) 59th, 2009, pp. 207-212.

[7] M.S. Doyle, W. Martin, D. Pease, T. Timpane,, "Low-loss flex circuit interconnect: Development of reduced insertion-loss flexible packaging," in Proc. 57th ECTC, 2007, pp. 1870-1876.

[8] H. Braunisch, J.E. Jaussi, J.A. Mix, M.B. Trobough, B.D. Horine, V. Prokofiev, L. Daoqiang, R. Baskaran, P.C.H. Meier, D.H. Han, K.E. Mallory, M.W. Leddige,, "High-speed flex-circuit chip-to-chip interconnects," IEEE Transactions on Advanced Packaging, Vol. 31, No. 1, pp. 82-90, Feb. 2008.

[9] E. McGibney, J. Barton, L. Floyd, P. Tassie, J. Barrett,, "The High Frequency Electrical Properties of Interconnects on a Flexible Polyimide Substrate Including the Effects of Humidity," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 1, No 1, pp. 4-, Jan. 2011.

[10] R. Aschenbrenner, A. Ostmann, A. Neumann, H. Reichl,"Process Flow and Manufacturing Concept for Embedded Active Devices," Proc. Of the IEEE Electronics Packaging Technology Conference, 2004, pp. 605- 609.

[11] A. Ostmann, A. Neumann, S. Weser, E. Jung, L. Böttcher, H. Reichl, “Realization of a Stackable Package Using Chip in Polymer technology,“ Polytronic Conference, June 23. – 26. 2002.

[12] Y. H. Chen, J.R. Lin, S. Chen, C.T. Ko, T.Y. Kuo, C.W. Chien, S.P. Yu, “Chipin-Substrate Package,” CSP Technology.

[13] Kazuhito Hikasa, Toshiaki Amano, Toshiya Hikami, Ken'ichi Sugahara and Naoyuki Toyoda, "Development of Flexible Bumped Tape Interposer," http://www.furukawa.co.jp.

[14] J. U. Knickerbocker, et al, “Development of next generation system-on-package (SOP) technology based on silicon carriers with fine-pitch interconnection,” IBM Journal of Research and Development, Vol. 49, No. 4/5, pp. 725-754, 2005.

[15] H.H. Chang, Y.C. Shih, C.K. Hsu, Z.C. Hsiao, C.W. Chiang,Y.H. Chen,and K.N. Chiang "TSV Process Using Bottom-up Cu Electroplating and its Reliability Test," Proc. 2nd Electronics System-Integration Technology Conference, Greenwich, UK, 2008 pp 645-650.

[16] Z. Wang, O. Yaegashi, H. Sakaue, T. Takahagi, and S. Shingubara, "Bottom-Up Fill for Submicrometer Copper Via Holes of ULSIs by Electroless Plating," Journal of The Electrochemical Society, Vol. 151, No. 12, pp. C781-C785, 2004.