CHARACTERIZATION OF SIP ASSEMBLY AND RELIABILITY UNDER THERMAL CYCLES

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ABSTRACT
This paper presents assembly challenges and reliability evaluation of 3D TMV™ (Three-Dimensional Through-Mold Via) and SiP (System in Package) in fine pitch ball grid arrays (FPGA). First, it presents the test matrix for various 3D TMV™ packaging assembly configurations and reliability characterizations performed under thermal cycling condition (–55°C to 125°C). The SiP test vehicles were configured with centrally located flip-chip (FC) die surrounded by eight chip scale packages (CSPs). The FC and CSPs, either with tin-lead or SAC305 balls, were assembled onto top of the FPGA interposer for subsequent assembly into a hybrid integrated configuration. Mix hybrid assemblies were characterized by X-ray for solder-joint quality and by Shadow Moiré method for warpage characterization. The assemblies were then subjected to thermal cycling between -40°C and 125°C for evaluation of reliability and followed for characterization of failure mechanisms. The paper presents details of design, characterization by X-ray and Moiré as well as behavior of the SiP and 3D TMV™ assemblies under two different thermal cycling conditions.

Key words: PBGA, system in package, SiP, thermal cycle, solder joint reliability, CSP, flip-chip, TMV™

INTRODUCTION

Stack packaging—more than Moore—has now widely implemented for use in commercial electronics because of cost and limitation of die fabrication with finer features [1-3]. Moore's law, stating that the number of transistors on a given chip will double every two years (now 18 months), has been substantiated and implemented throughout the past several decades. The exponential growth for die density has allowed computers and electronic communication devices to become cheaper and more powerful and smaller simultaneously. In addition, the increase in package density has further helped this miniaturization trend by using area array for interconnection rather than conventional packaging such as quad flat package (QFP) with peripheral leads [4-8]. A package with an array of solder bumps is commonly referred to as ball-grid array (BGA) technology. If the package dimension is nearly that of the integrated circuit (IC) itself, then the technology is called chip-scale package (CSP). Wafer-level package (WLP) uses wafers with added protection coating, and subsequent singulation provides dense components with standard packaging attributes such as ease of testing and handling. Fan-out WLP (FO-WLP) redistributes I/Os to outer rows by reconstitution at wafer level with subsequent singulation to better accommodate die size changes and ease of assembly at PCB level.

Figure 1 illustrates 2.5/3D stack packaging trends from those that are in the development stage to those that are now mainstream. The 2.5D covers segmented die with passive Through Silicon Via (TSV) interposer within package or active interposer with packages, aka as System in a Package (SiP). The 3D packaging consists of stacking of packaged devices called package-on-package (PoP), including through-mold via (TMV™), and stacking of die within a package called package-in-package (PiP) or stacked wire-bonded die (primarily memory) [9-10]. The PoP and PiP technologies are used today using conventional stacking or other unique technologies such as TMV™ and TSV as well as through-edge-interconnection processes for device stacking within packages [11-15].

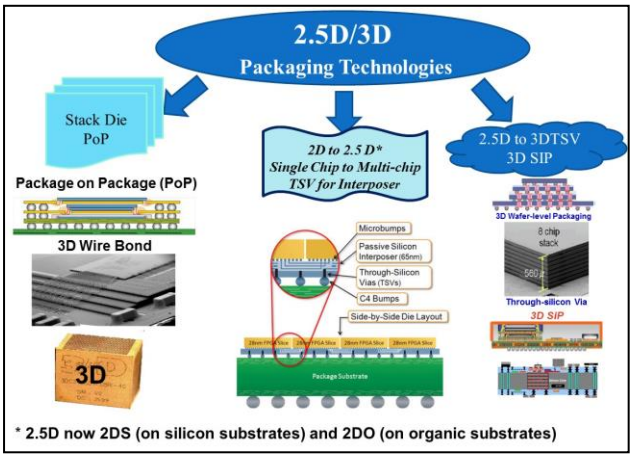

Figure 1. 2.5/3D stack packaging technology roadmap with maturity status.

In general, COTS conventional or 3D packages using plastic-encapsulated materials (PEMs) have two key limitations:

1. Due to the major differences in design and construction, COTS packages have a smaller operating temperature range and are typically more frail and susceptible to moisture absorption compared to high-performance devices; therefore, the standard test practices used to ensure that high-performance devices are robust and

highly reliable often cannot be applied to PEM packages.

2. Users of 3D COTS packages have little visibility into commercial manufacturers' proprietary design, materials, die traceability, and production processes and procedures, whereas controls are in place for the high-reliability systems.

A literature survey indicates that most prominent failures for COTS 3D packages and assemblies are due to warpages (individual or system) for plastic packages. For the stack ceramic package and TMV™, failures due to via are also of concern. In addition, both plastic and ceramic stack packages are required to meet minimum shock and vibration requirements per Mil-STD-883. Separation of stack layers, if not adhesively bonded together, during shock is another failure mechanism that needs to be considered. Moreover, very limited techniques are available to ensure quality and reliability of 2.5/3D stack packaging and assemblies.

TEST VEHICLES

Figure 2 presents the two experimental methods —3D TMV™ and SiP — carried out as part of an internal task by R. Ghaffarian and in collaboration with AREA Consortium, respectively. The internal task has concentrated on evaluation of thermal cycle behavior of advanced COTS 2.5/3D electronics including 3D TMV™ for high-reliability applications. This paper first presents the evaluation performed on TMV™ stack packaging-assembly reliability. Then, it presents evaluation performed for a number of SiP assemblies with CSP packages and FC die assembled on top of an FPGA interposer under AREA Consortium.

The first section presents test matrix design, 3D TMV™ package daisy-chain patterns, detailed design of PCB, test vehicle design, and detailed information with representative images of assemblies. It also includes the three approaches of 3D stack assembly— pre-stacking package or stacking during PCB assembly with using either flux/solder or solder/solder. The interim thermal cycle test results to 200 cycles (–55°C /125°C) were also presented.

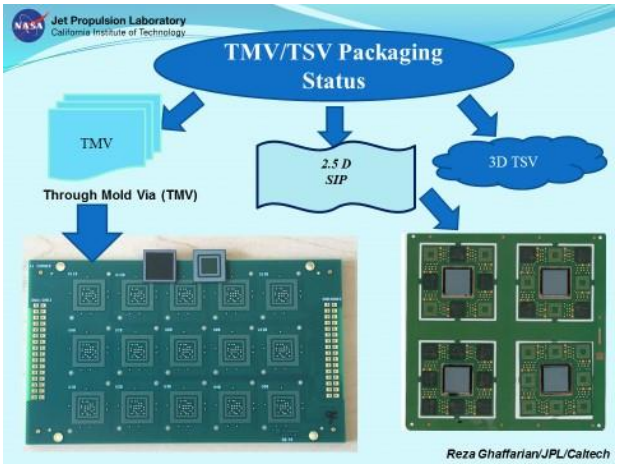

Figure 2. Two test vehicles were evaluated: (1) 3D TMV™ packages and (2) SiP on FPBGA interposer.

The second section presents assembly, characterization, and reliability test results for SiP assembly configurations with a centrally located FC die surrounded by eight chip scale packages (CSPs). The interim thermal cycle (–40°C /125°C) test results for two configurations of CSPs, with and without underfill conditions, were presented. Extensive failure analyses were performed by X-ray, optical, and SEM were also presented.

3D TMV™ Test Matrix

To determine assembly reliability of 3D TMV™ stack packaging technologies, packages with daisy chain patterns are required for detecting solder joint failure by electrical daisy-chain open. Industry has designed the stack package with daisy-chain pattern to match those of PCB for drop test evaluation, but it in this evaluation, it was used for thermal-cycle reliability characterization. Figure 3 illustrates the key elements of the bottom TMV™ package on package configuration. This packaging technology uses a matrix-molded platform for bottom construction and creates through-via interconnections to the top surface via a laser ablation process [9]. The 14×14 mm daisy chain package incorporates a 200 I/O, 0.5 mm pitch, on top side interface, and 620 bottom FBGAs at 0.4 mm pitch.

This package with already daisy-chain test verified design was considered for solder joint evaluation. The design facilitates the 3D TMV™ solder-joint reliability characterization since most package styles from a manufacturer do not come in daisy-chain form. This was the most effective approach to meet the cost objectives since to design a unique test vehicle (TV) for evaluation is costly. The daisy-chain resistive loop were monitored during thermal cycling during cycling or at intervals to allow detection of an open resistive loop due to solder-joint opens at either package levels (bottom or top) of 3D TMV™ assemblies.

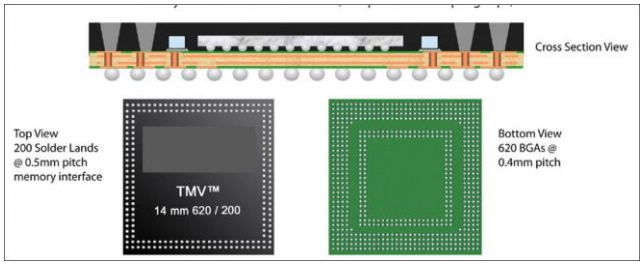

Figure 3. Cross-section top and bottom view of a new 3D TMV™ package [9].

A design of experiment (DOE) technique was used to cover three aspects of packaging stack assemblies and their effect on the stack packaging assembly reliability. The three package stacking were as the following.

- The top package was only fluxed and placed onto the lower package, which was placed on tin-lead solder paste. Then, both reflowed with 15 TMV packages (see Figure 4).

- Solder paste was placed onto the bottom package pads prior to placement of the top package, which was placed on tin-lead solder paste of the PCB pad patterns. Then, the TMV™ stacks were reflowed.
- Pre-stack package as a unit with tin-lead solder and then assemble the stack package onto PCB with tin-lead solder paste. Then, the pre-stack reflowed with 9 TMV packages (see Figure 5).
- The top 14 mm package had 200 lead free SAC105 balls with 0.5-mm pitch. The lower through mold via 14 mm package has 620 lead free SAC125 balls with 0.4-mm pitch.
- PCB materials was FR-4 with 93 mil thickness with microvia in pad and ENEPIG surface finish

The pre-stack approach is possibly the most applicable approach for high-reliability application even though this approach is the most costly approach. Reliability is another key aspect that should be considered in the overall final selection of the 3D TMV selection for application.

Figure 4. Fifteen 3D TMV™ daisy-chain package assembly with tin-lead solder either at package or PCB level.

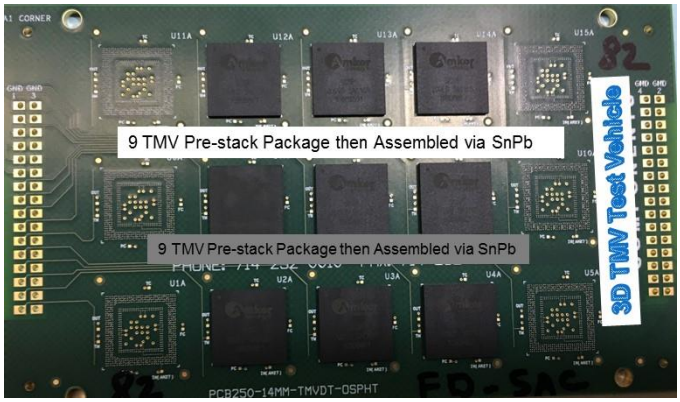

Figure 5. Nine 3D TMV™ daisy-chain package pre-stacked and then assembly onto PCB with tin-lead solder

TMV™ under Thermal Cycles

After successful assembly of a large number of test vehicles, they were subjected to 200 thermal cycles (TC) in the range of –55 to 125°C. In addition to daisy-chain resistance evaluation monitoring, X-ray and optical images for the as assembled and after thermal cycles are presented. Figure 6-7 present representative of X-ray and optical images after thermal cycling.

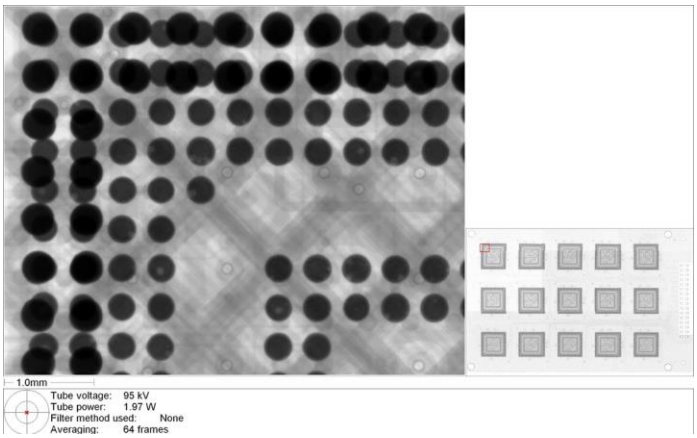

Figure 6. X-ray image of corner of 3D TMV™ package showing packages configuration being peripheral and limited number of voids.

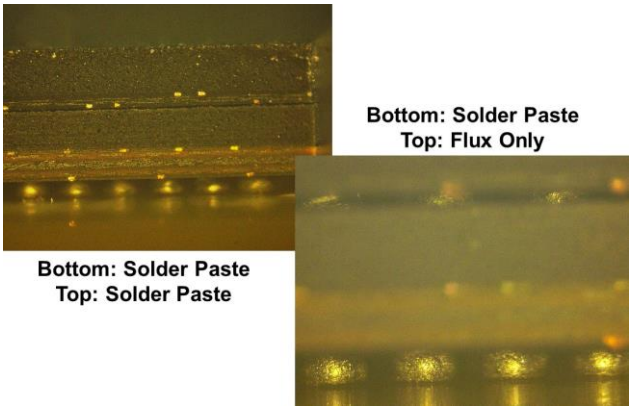

Figure 7. Optical photomicrographs of two 3D TMV™ daisy-chain packages, one with using solder paste on both and the other on the bottom FPGA.

SYSTEM-IN-PACKAGE EVALUATION

In the second experimental approach, SiP TVs were configured with centrally located FC die surrounded by CSPs. As shown in Figure 8, the TV design allowed for up to eight CSP packages to be attached around perimeter of each SiP interposer.

The FC die and CSPs of the SiP were assembled onto an FPGA interposer for subsequent assembly in a hybrid configuration (see Figure 9). The CSPs with tin-lead or SAC305 solder balls were assembled onto interposer covering partially or fully the interposer-CSP sites. Mix assembly becomes a challenging task and needs to be characterized for acceptance of quality. Characterizations were performed by X-ray for solder-joint quality and by a Shadow Moiré method for warpage analysis.

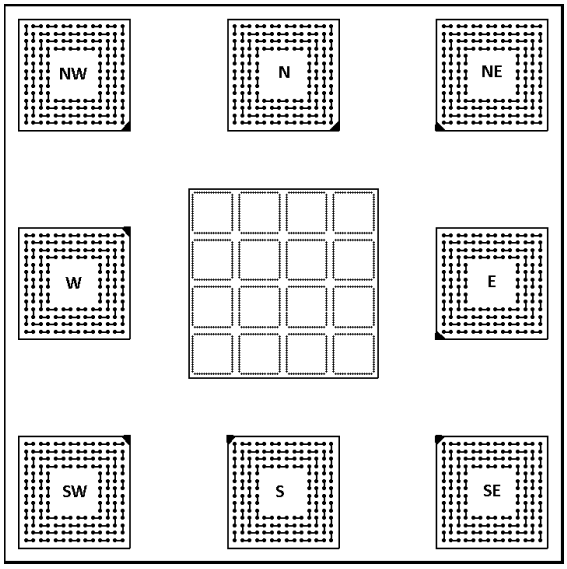

Figure 8. Drawing showing top view of SiP substrate with eight CSP memory placements and centrally located IC placement. Reference designators provided.

Acceptable assemblies were then subjected to thermal cycling for reliability evaluation. Thermal cycling was performed between -40°C and 125°C with 15 minute dwells at the temperature extremes. Transition rates between the temperature extremes were less than 10°C per minute resulting in a total cycle time of 74 minutes. Results are presented in the following.

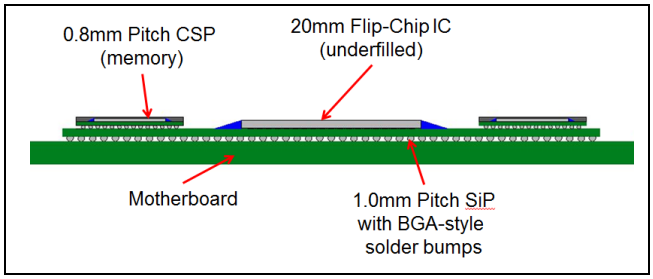

Figure 9. Drawing showing cross-sectional view of SiP test vehicle.

SiP Test Vehicles

Figure 10 shows a SIP interposer with the IC assembled at the center and showing CSP pattern surrounding the interposer before their assembling.

The interposer constructed using daisy-chain pattern to complement the IC and CSP daisy-chain patterns. The CSP simulates a memory package and had 160 solder balls (CABGA 160), 12x12 mm, with SAC305 balls as shown in Figure 11.

The SiP interposer BGA body was designed having 3364 balls with 1.0-mm pitch. The SiP inteposer area was 60x60 mm^2 with 0.9-mm thickness utilizing blind and buried via structures representing signal conduction between the layers (see Figure 12).

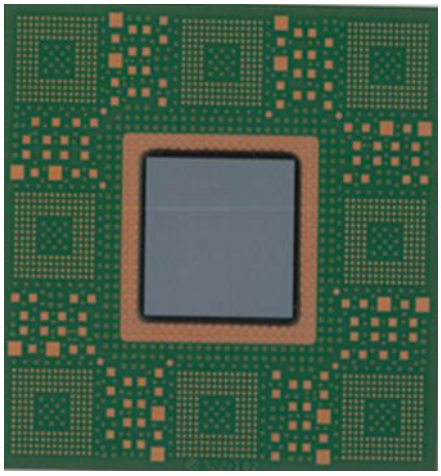

Figure 10. Top view of SiP substrate with flip-chip die.

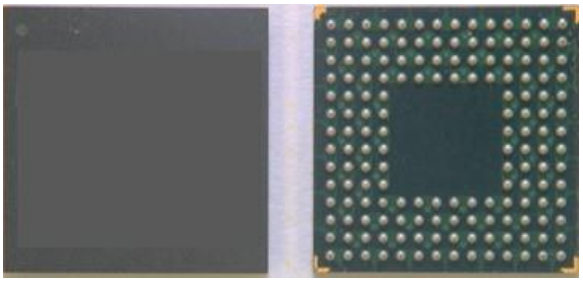

Figure 11. Top and bottom view of CABGA with 160 solder balls.

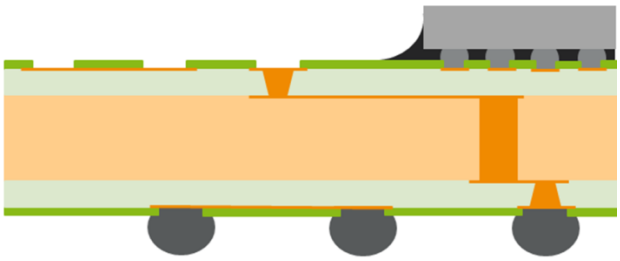

Figure 12. Drawing showing partial cross-section of SiP BGA with FC die and BGA solder bumps attached.

Interposer Warpage Characterization

Shadow Moiré analysis was performed during assembly reflow cycle to determine deformation behavior of SiP interposer with temperature. The SiP-interposer deformations were measured at temperature intervals including room temperature (RT), 100°C, 150°C, 215°C, and 245°C during ramp up and at 215°C, 150°C, 100°C and 25°C. Analysis evaluated the free-body deformation across the FBGA bump side and for each component. The measurement temperatures were selected to coincide with

milestone temperatures experienced during typical lead-free reflow processes including peak reflow temperature (245°C) and the expected solder solidification range of 215°C to 150°C. Figure 13 shows a representative of Shadow Moiré color coded warpage configuration for a bare SiP interposer.

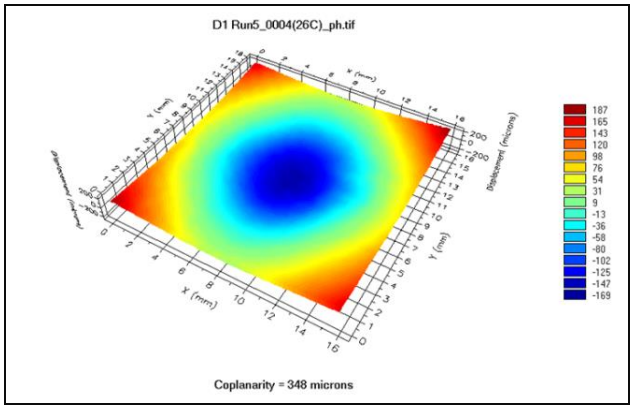

Figure 13. Representative Shadow Moiré contour plot at 25°C for a non-populated SiP FBGA interpose. Image is produced "ball side up" and indicates that the center of the package would be raised above the board surface.

Figure 14 shows plots of a number of interposer warpage profile from RT to reflow temperatures. The results of the analysis indicate that the interposer has an extreme convex shape profile at RT that rapidly flattens with a slightly concave at elevated temperatures. The interposer are reasonably flat at solder solidification temperatures (215°C to 150°C).

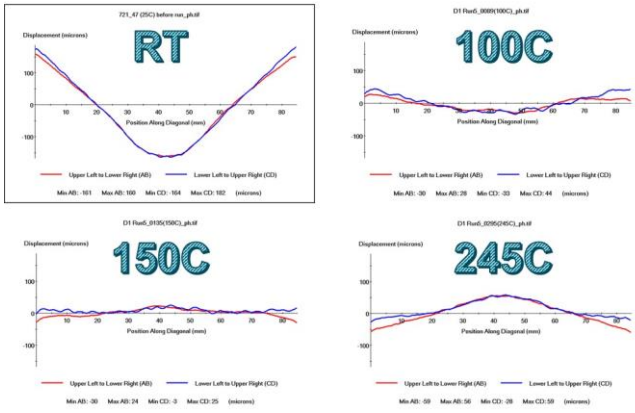

Figure 14. Representative of Shadow Moiré diagonal plots for RT to reflow temperatures showing change in curvature sign and near flatness near the reflow temperatures.

Assembly and Inspection Processes

The basic process flow used to construct and evaluate the test assemblies was:

1. Print solder paste over interposer
2. Place SiP and interposer CSP (with and without dip flux, as needed)
3. Dip flux and pace CSP on SiP as required
4. Perform reflow soldering
5. X-ray inspection
6. Daisy-chain verification test

Reflow was performed using a convection reflow oven featured 10 heating and 3 cooling zones. All assemblies were inspected by X-ray to characterize quality of solder joints prior to environmental exposures. The X-ray inspection was primarily focused on characterizing voids in solder joints and identifying solder bridging, if any. Both CSP and FBGA solder joints were inspected. Out of 80 SiP assemblies, only two were found to have workmanship defects. One defect was attributed to a placement error during the pick & place process, which resulted in the SiP being placed one row off in the y-direction. The other defect was due to solder bridging. The solder-bridge defect occurred in a SiP assembled with SnPb solder. The X-ray images showed that six solder-joint pairs located at the center of the device had bridged (Figures 15).

The reason for the bridges is unknown, but bridging at the center of a package is often occurred due to the deflection profile of the device resulting either in a concave 'corner ball up' or concave down that in both cases result in increased loading, leading to excess solder ball collapse or stretching and possible bridging. This is especially more prominent for the concave condition. Based on the Shadow Moiré results, these defects most likely occurred while the samples were near the peak reflow temperature, when the parts demonstrated concave warpage of 120 to 140 microns.

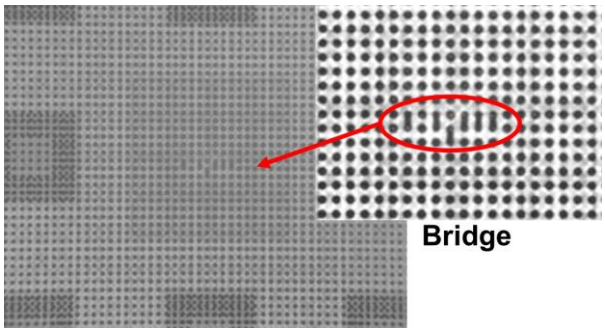

Figure 15. Solder bridging at the center of device in the SiP interposer.

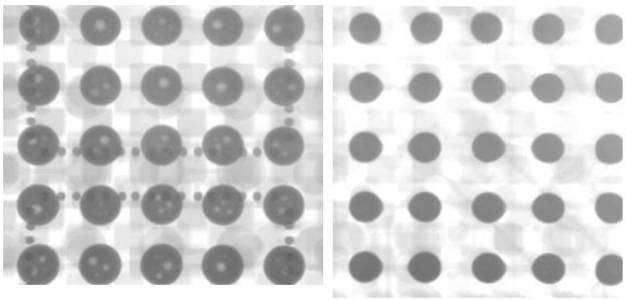

Figure 16. Comparison of voids near center of SnPb SiP (left image) and perimeter of SiP (right image).

The other goal of the X-ray inspection was to characterize solder-joint void levels. In most cases, the number and/or size of voids observed in the CSP or SiP FBGA solder joints were negligible. However, the SnPb test cell did produce large and numerous voids in the SiP FBGA. Interestingly, the voids were primarily located near the center of the package as previously shown in Figure 16.

TEST RESULTS

Thermal Cycle

The SiP functionally good assemblies were subjected to accelerated thermal cycle testing in order to evaluate solder joint reliability. Event detector was used to detect resistance spikes, exceeding 500 ohms and lasting in an excess of 200 nanoseconds. Accelerated thermal cycle was performed between –40°C and 125°C with 15 minute dwells at the temperature extremes with a total cycle of 74 minutes.

A large number of variables were considered in the DOE design including evaluation of bare FBGA, FBGA balls either with SAC305 or tin-lead solder, FBGA fully/partially populated with CSPs and FC die, and selectively adding underfill on CSPs. Failure analyses indicate that the SiP FBGA solder joint lifetime was significantly impacted by these variables. The Weibull failure characteristic lifetimes ranged from about 500 to 2000 thermal cycles. However, the first cycles-to-failures were lower and were about 300 to 1500 cycles.

The lowest cycles-to-failure was for the SiP FPGA with underfilled CSPs. This test cell was a SAC305 assembly in which all eight CSPs had been placed onto the FPGA and were underfilled. For this case, the Weibull characteristic lifetime of the population was 512 thermal cycles with the first failure detected at 325 cycles. Cycling of this test cell was stopped after 800 cycles with 7 of 8 failures.

Increase in cycles-to failures was observed when CSPs were not underfilled. The characteristic lifetime increased to 1339 cycles with the first failure at 455 cycles. The possible reasons for such changes in reliability are discussed in the following section.

DISCUSSION

Reliability under thermal stress for SiP package and assembly affected by constituent elements and global/local interfaces. Solders in surface mount are unique since they provide both electrical interconnection and mechanical load-bearing element for attachment of package on PCB. So, three elements play key roles in defining reliability for SiP, global, local, and interconnections. The characteristics of these three elements — FBGA in SiP (e.g., rigidity change by FC die/CSP), PCB (e.g., rigidity change by thickness), and solder joints (e.g., characteristic change by SAC305/tin-lead solder ball/attachment)—affect thermal cycle reliability characteristics and failure mechanisms. Majority of fatigue failures of solder joints in SiP assemblies are due to induced damage by global CTE mismatches, which result from differential thermal expansions of the SiP package and the PCB assembly and their rigidities. These thermal expansion differences stem from differences in the coefficients of thermal expansion (CTEs) covering the CSP and FC die assemblies and underfill condition. The shear strain representative of the global CTE mismatch due to thermal excursion is given as the following.

$$\Delta\gamma = (\alpha_{SiP} - \alpha_{PCB})\,(Tc - T_0)\,L_d/h = (\Delta\alpha)\,(\Delta T)\,DNP/h$$

Global CTE mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch, i.e., the CTE-mismatch ($\Delta\alpha$), the temperature swing (ΔT), and the largest acting package length (L_d), a.k.a., distance to neutral point (DNP), can be large. In thermal cycling, this global expansion mismatches will cyclically stressed, and thus fatigue, the solder joints. The stress level on SiP assembly also affected by the local stiffness changes for FBGA due to addition of CSP/FC, solder balls and joints, and PCB. Considering this background, now, the reasons for early failure of SiP with CSP underfill and improvement without CSP underfill are as follows:

1. For this design, CSPs are located at the corner of SiP, The addition of CSP with underfill at these corners increased induced stresses due to local increase in rigidity. In addition, warpages are highest at the corners of SiP (see Figure 17) that add tensile stresses in addition to shear stresses due to global CTE mismatches. Combination of the two, increases the state of stresses on the corner of SiP; therefore, decreasing the fatigue life
2. When CSPs on FBGA are not underfilled, the local stiffness at a corner of SiP decreases relative to the CSPs with underfilled condition. This decrease in stiffness condition expected to increase cycles-to-failures. The thermal cycle test data shows this trend, cycles-to-failures for underfilled condition were in the range of 325 to 512 that were increased to 455 to 1339 cycles for the assemblies with CSPs having no underfill.

Fatigue inversely proportional to SiP stiffness and $(\Delta T)^2$. The cumulative fatigue damage will ultimately cause the

failure of one of the solder joints, typically corner joints in complex BGA or the corner of the die within pacakge if the stiffness of die become a dominant factors in a full array BGA assembly.

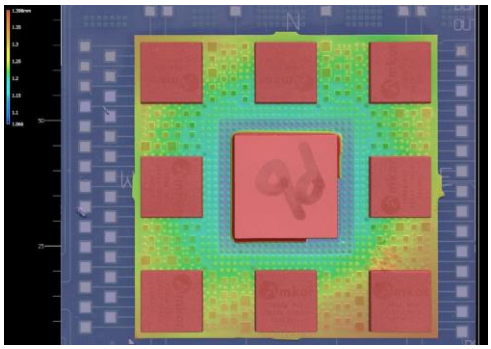

Figure 17. Representative of warpage of SiP after thermal cycling with corner having the highest values.

CONCLUSIONS

This paper presented a comprehensive test matrix developed to assemble and evaluate reliability under thermal cycle conditions for a large number of advanced 3D TMV™ and SiP package assemblies. The 3D TMV™ and SiP assemblies were subjected to cycling profiles in the range of –55°C to +125°C and –40°C to +125°C, respectively. Characterization for quality assurance (QA) and failure analyses were performed by X-ray, optical images, and by X-sectioning evaluation.

- For an accelerated thermal cycle profile of –55°/125°C, the three 3D TMV™ stack configuration assemblies—built with tin-lead solder at package and PCB levels, flux dip at package level and tin-lead solder at PCB level, and pre-stack package and solder at PCB—did not show failures after 200 cycles determined by daisy-chain resistance measurement. However, failures were observed at higher cycles and were analyzed by X-ray and X-sectioning.
- For an accelerated thermal cycle profile of –40°/125°C, the SiP assemblies with either tin-lead or SAC305 solder balls did not show failures after 200 ATC determined by daisy-chain resistance measurement. However, failures were observed at higher cycles.
- Possible reasons for early failures of SiP assemblies with underfilled CSPs were presented. Key parameters that paly roles in early failures are postulated to be: (1) the global CTE mismatches between FPGA and PCB, (2) local stiffness due to CSP on FPGA, and (3) higher warpage at the FPGA corner locations.

Further qualification tests are being performed by thermal cycling and characterizations to determine failure mechanisms and the reliability limitations of these advanced 2.5/3D electronic packaging technologies for high-reliability applications.

ACKNOWLEDGEMENTS

Part of the research described in this publication is being conducted at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Copyright 2018. California Institute of Technology. U.S. Government sponsorship acknowledged.

The SiP activities was carried in collaboration with AREA Consortium. The authors would like to acknowledge the support of JPL and Universal team members.

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