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Characterization of Printed Circuit Board Material & Manufacturing Technology for High Frequency

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Abstract
Today´s Electronic Industry is changing at a high pace. The root causes are manifold. So world population is growing up to eight billions and gives new challenges in terms of urbanization, mobility and connectivity. Consequently, there will raise up a lot of new business models for the electronic industry. Connectivity will take a large influence on our lives. Concepts like Industry 4.0, internet of things, M2M communication, smart homes or communication in or to cars are growing up. All these applications are based on the same demanding requirement – a high amount of data and increased data transfer rate. These arguments bring up large challenges to the Printed Circuit Board (PCB) design and manufacturing.

This paper investigates the impact of different PCB manufacturing technologies and their relation to their high frequency behavior. In the course of the paper a brief overview of PCB manufacturing capabilities is be presented. Moreover, signal losses in terms of frequency, design, manufacturing processes, and substrate materials are investigated. The aim of this paper is, to develop a concept to use materials in combination with optimized PCB manufacturing processes, which allows a significant reduction of losses and increased signal quality.

First analysis demonstrate, that for increased signal frequency, demanded by growing data transfer rate, the capabilities to manufacture high frequency PCBs become a key factor in terms of losses. Base materials with particularly high speed properties like very low dielectric constants are used for efficient design of high speed data link lines. Furthermore, copper foils with very low treatment are to be used to minimize loss caused by the skin effect. In addition to the materials composition, the design of high speed circuits is optimized with the help of comprehensive simulations studies.

The work on this paper focuses on requirements and main questions arising during the PCB manufacturing process in order to improve the system in terms of losses. For that matter, there are several approaches that can be used. For example, the optimization of the structuring process, the use of efficient interconnection capabilities, and dedicated surface finishing can be used to reduce losses and preserve signal integrity.

In this study, a comparison of different PCB manufacturing processes by using measurement results of demonstrators that imitate real PCB applications will be discussed. Special attention has be drawn to the manufacturing capabilities which are optimized for high frequency requirements and focused to avoid signal loss. Different line structures like microstrip lines, coplanar waveguides, and surface integrated waveguides are used for this assessment.

This research was carried out by Austria Technologie & Systemtechnik AG (AT&S AG), in cooperation with Vienna University of Technology, Institute of Electrodynamics, Microwave and Circuit Engineering.

Introduction

Several commercially available PCB fabrication processes exist for manufacturing PCBs. In this paper two methods, pattern plating and panel plating, were utilized for manufacturing the test samples.

The first step in both described manufacturing processes is drilling, which allows connections in between different copper layers. The second step for pattern plating (see figure 1) is the flash copper plating process, wherein only a thin copper skin (flash copper) is plated into the drilled holes and over the entire surface. On top of the plated copper a layer of photosensitive etch resist is laminated which is imaged subsequently by ultraviolet (UV) light with a negative film. Negative film imaging is exposing the gaps in between the traces to the UV light. In developing process the non-exposed dry film is removed with a sodium solution. After that, the whole surrounding space is plated with copper and is eventually covered by tin. The tin layer protects the actual circuit pattern during etching. The pattern plating process shows typically a smaller line width tolerance, compared to panel plating, because of a lower copper thickness before etching. The overall process tolerance for narrow dimensions in the order of several tenths of µm is approximately ± 10%.

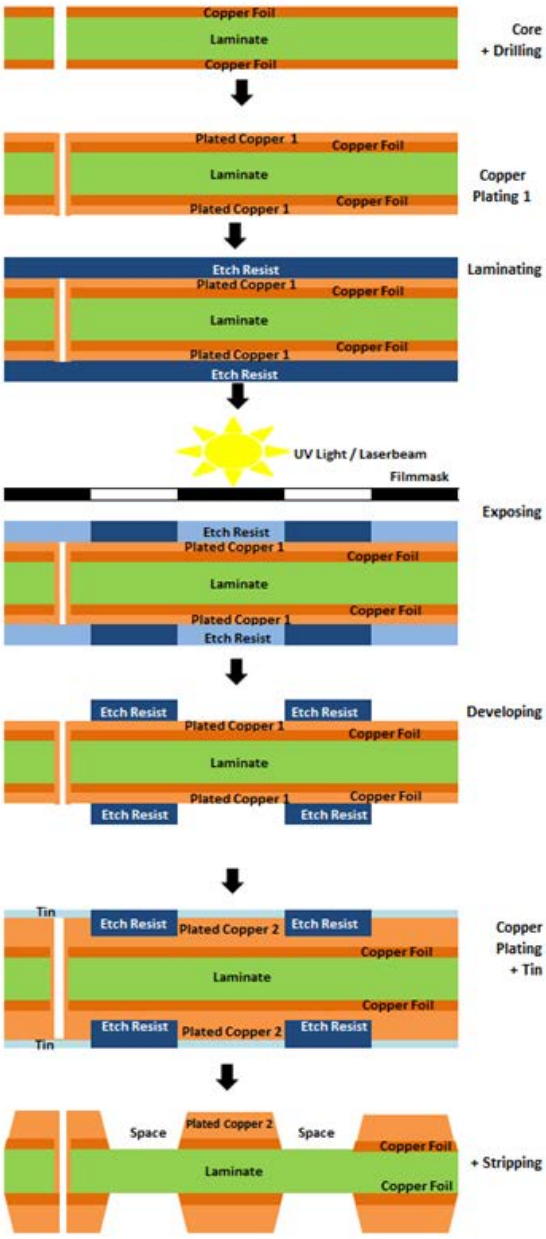

Figure 1: Pattern plating

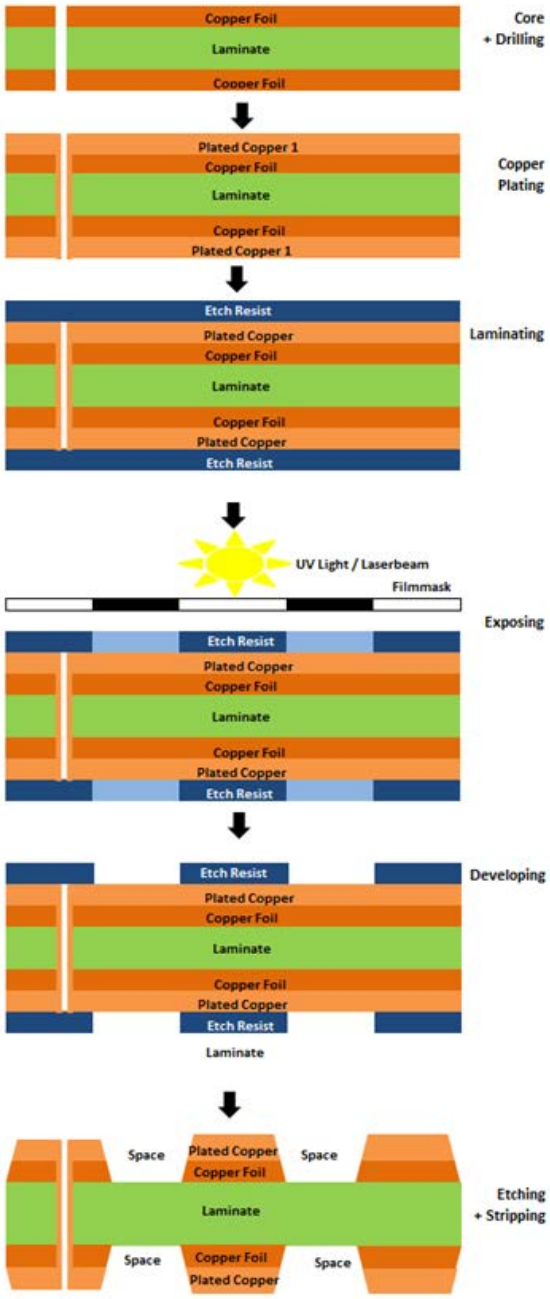

Figure 2: Panel plating

The second typical PCB manufacturing process is panel plating (see Figure 2). In this process, after drilling, the entire panel is plated with copper. On top of the plated copper a layer of photosensitive etch resist is laminated. After that, there is positive film imaging, whereby the actual circuit pattern is exposed to UV light. After developing, the copper is etched with a chemical wet process and in the last step the etch resist is removed and the copper structure is finished. It should be noted that in panel plating the etching is applied on the whole thickness of plated copper and copper foil. During panel plating the copper thickness varies up to ± 3% only, because of the uniform plating method. However, the distribution of the etching solution on the surface is unequal, a lower exchange of etching solution and copper occurs in the center and somewhat more on the edges of a production panel. This is called “puddling effect”. The consequences are wider lines in the center and narrower lines at the edges of each panel. The overall process tolerance for narrow dimensions in the order of several tenths of µm is approximately ± 20%.

The purpose of this paper is to investigate how these structuring processes impact the losses of radio frequency (RF) signals up to 110 GHz. Furthermore, as different transmission line modes may exhibit distinct loss behavior, the second point is how these losses depend on the selected transmission line mode, namely microstrip (MS), conductor backed coplanar waveguides (CBCPW), and substrate integrated waveguides (SIW).

Materials & Evaluation Board

In order to investigate the relationship between losses and structuring processes, various PCBs have been designed and manufactured using distinct dielectric materials. Material type A is a very low dielectric constant (Dk) material based on PTFE with ingredients of fused silica, continuous filament, and titanium dioxide i.e. a ceramic filler. According to the manufacturer's datasheet, the dielectric constant of this material is 3.00 with an LT of 0.001 at 10 GHz. Material type B is a low Dk material with 2 x 2116 glass type and 54% nominal resin content on either side of the fiber. The compound has a Dk of 3.61 and an LT of 0.004 at 10 GHz, according to the datasheet. The basic stack-up for both materials consists of the described RF-substrates with a top and bottom copper layer (see Figure 3). To avoid difficulties during the measurements on a waver prober, due to the small overall thickness of less than 200 µm, an additional carrier is attached on the bottom side to minimize the risk of waviness of the evaluation board. The thickness of the conductive layer varies within 28 – 37 µm and 22 – 25 µm for panel plating and pattern plating process respectively. Thickness of the dielectric layer ranges within 125 – 130 µm. The outmost surface, the signal layer, is covered with immersion nickel/gold. The thickness of nickel and gold is 6 µm ±1 µm and 0.5 µm ± 0.1 µm, respectively.

Figure 3: Stack-up

Design Description

The losses should be continuously evaluated up to a maximum frequency of 110 GHz, therefore, line elements with different lengths are designed and manufactured for the transmission modes of interest. For best measurement accuracy all lines have been designed for a 50 Ω wave impedance. All measurements have been carried out using a wafer prober, which requires appropriate launching pads for contacting the probe-tips to PCBs. Furthermore, the waver prober limits the maximum probe separation and consequently allows the longest straight line to be around 25 mm.

The first mode to be investigated is MS (see Figure 4a). MS lines feature a quasi-TEM propagation mode with a significant amount of the fields in air depending on the line width to substrate height dimensions. The trace width for an MS transmission mode W_{MS} is determined to be 285 µm and 260 µm, for material type A and B, respectively. The second mode is CBCPW (see Figure 4b), a quasi-TEM propagation mode too, whereby in this case most of the field is concentrated in the substrate. The involved field pattern of CBCPW strongly depends on the manufactured dimensions, as for thick substrates the fields tend to propagate in the gap and for thin substrates, as in this case, in the substrate itself. The trace width for CBCPW W_{CBCPW} is determined to be 280 µm and 250 µm, and the gap G_{CBCPW} to be 250 µm and 250 µm for material type A and B, respectively. For CBCPW also the connection of the top to the bottom ground plane is important to keep in mind, as via placement and via spacing can degrade the measurements drastically.[1] The last mode is a TE10 in an SIW (see Figure 4c) where the entire field is in the substrate. For this design the width of the SIW W_{SIW} defines the cutoff frequency f_{cutoff}, and thus the frequency range of operation. W_{SIW} is set for both materials to be 1700 um as there is expected just a slight shift of f_{cutoff}, however, with the benefit of keeping the manufacturing dimensions entirely equal. Although all samples are manufactured on low loss materials, there should be an apparent impact on the losses if a significant amount of the field is in air as the LT of air is close to 0. Figure 4d provides an overview how the top copper layer of the evaluation boards looks like exemplary for the SIW lines.

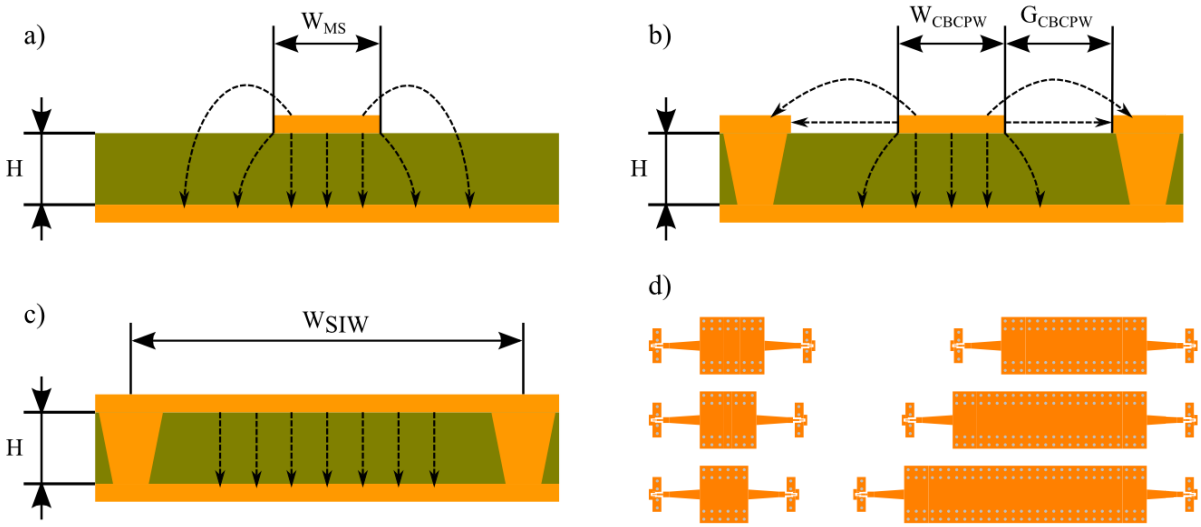

Figure 4: MS, CBCPW, and SIW designs with dimensions

Measurement Equipment

All measurements have been conducted using a production vector network analyzer (VNA) that is enhanced by two external W-band converters which allows continuous measurements up to 110 GHz (see Figure 5). The available wafer prober is a production semi-automatic probe system and tungsten probes with a pitch of 100 µm have been used. Furthermore, a W-band calibration substrate is used to relocate the reference plane for all S-parameter measurements to the probe tip.

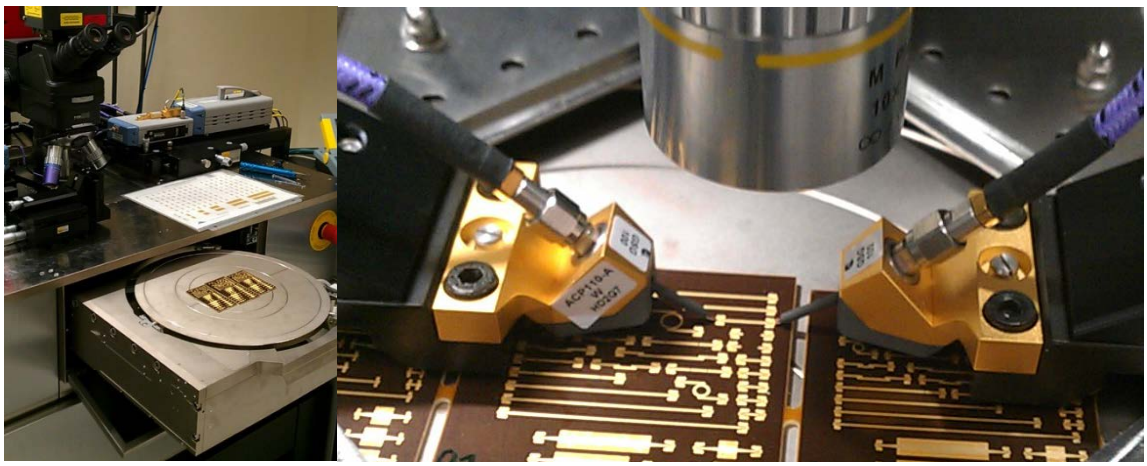

Figure 5: Measurement equipment

Analysis and measurement results: Fabrication Process

The evaluation boards have been manufactured using two different PCB fabrication processes, pattern platting and panel plating. The two main differences of these fabrication processes are firstly the manufacturing tolerances of trace widths and gaps, and secondly the shape of the traces itself. According to the micro-section analysis carried out on evaluation boards manufactured with the nominal dimensions of Figure 4, traces of the panel plating samples have a trace width of 241 µm on top and 269 µm on the bottom side for material type B, which is a width difference of 13%, with a total copper thickness of 30 µm ± 5 µm. The shape of the trace looks similar to a trapezoid. The results of the pattern plating process are 249 µm on top and 259 µm on the bottom side, which is a difference of only 3% in width at a copper thickness of 30 µm ± 3µm. The cross sections for MS of both fabrication processes are depicted in Figure 6. The stated dimensions are the ones of the copper width only, which means that the whitish immersion nickel/gold surface finished is not taken into account. Closer investigation of the micro-sections of the evaluation boards showed that both samples had a slight penetration by immersion nickel/gold into the dielectric surface on the trace edges, which will also impact the occurring losses.

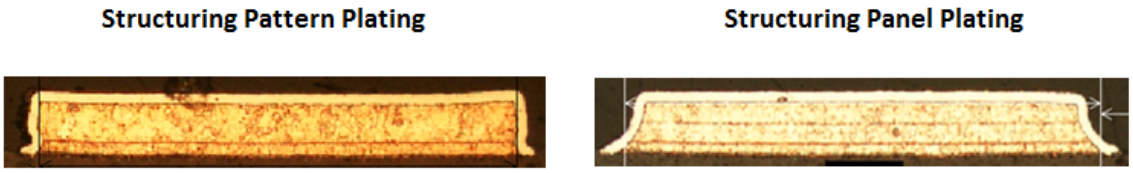

Figure 6: Trace cross section

The top surface of the traces is further evaluated by Scanning Electron Microscopy (SEM). It can be seen in Figures 6 and 7 that there is some overlap caused by the immersion of nickel/gold onto the dielectric surface on trace edges of the copper conductor. The panel plating evaluation board showed an overlap from the trace edge to dielectric surface of 9 µm ± 2µm while the measurement of the pattern plating test vehicle showed just 4 µm ± 2µm. The primary reason for this phenomenon can be found in the treatment process of the copper foil. Both structuring processes pictured in Figures 6 and 7 use the same base material and copper foil. Nevertheless, the slightly protruding copper residues are removed more thoroughly for the pattern plating process. Consequently, the end surface overlap into the dielectric material is reduced. A main result is the consequence that this observation has to be considered for the design preparation by the PCB manufacturer to preserve the line characteristics as well as to ensure low losses for the higher frequency domains.

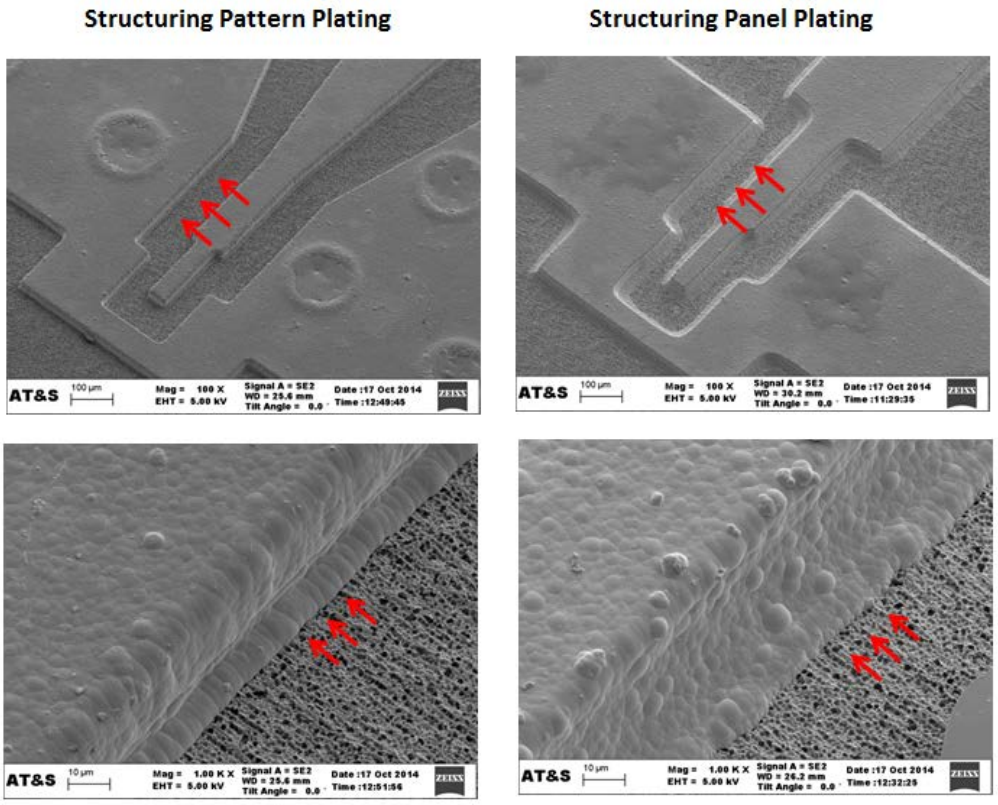

Figure 7: SEM analyses

Analysis & measurement results: RF-Losses

Firstly a process comparison is made for the MS line mode for three different line lengths L. As can be seen in Figure 8, for material type A for an MS line with L = 5 mm there is basically no measureable difference between the applied fabrication processes. However, for increasing line lengths there occur proportionally larger losses as shown for L = 10 mm and L = 25 mm. At the maximum measured frequency of 110 GHz, pattern plating shows about 0.65 dB more loss for L = 25 mm. For material type B (see Figure 9) the same observations can be made for L = 5 mm where there is no difference at all for the two manufacturing processes, and for L = 10 mm and L = 25 mm losses increase with L. It is interesting to note that at the maximum frequency the longest line shows approximately the same difference between the losses of the compared processes as has been reported for material type A. The insertion loss can be appropriately fitted in a least-square manner with $S_{12}(dB) = \hat{a} \cdot \sqrt{f} + \hat{b} \cdot f$ with $\hat{a}$ and $\hat{b}$ being the factors to be determined over frequency f.[2] By fitting the insertion loss, measurement deviations are reduced and a smooth curve for the additional loss of panel plating over pattern plating can be obtained. In Figure 10 this mathematical procedure has been exemplarily done for three different line lengths on material type A, wherein it can be seen that for low frequencies

there is basically no difference in between the fabrication processes. Below 20 GHz the losses for all manufactured lines are still smaller than 0.1 dB, however, as frequency increases losses grow substantially. It can be concluded that material type A exhibits about 20% more losses due the different fabrication process for L = 25 mm at 110 GHz.

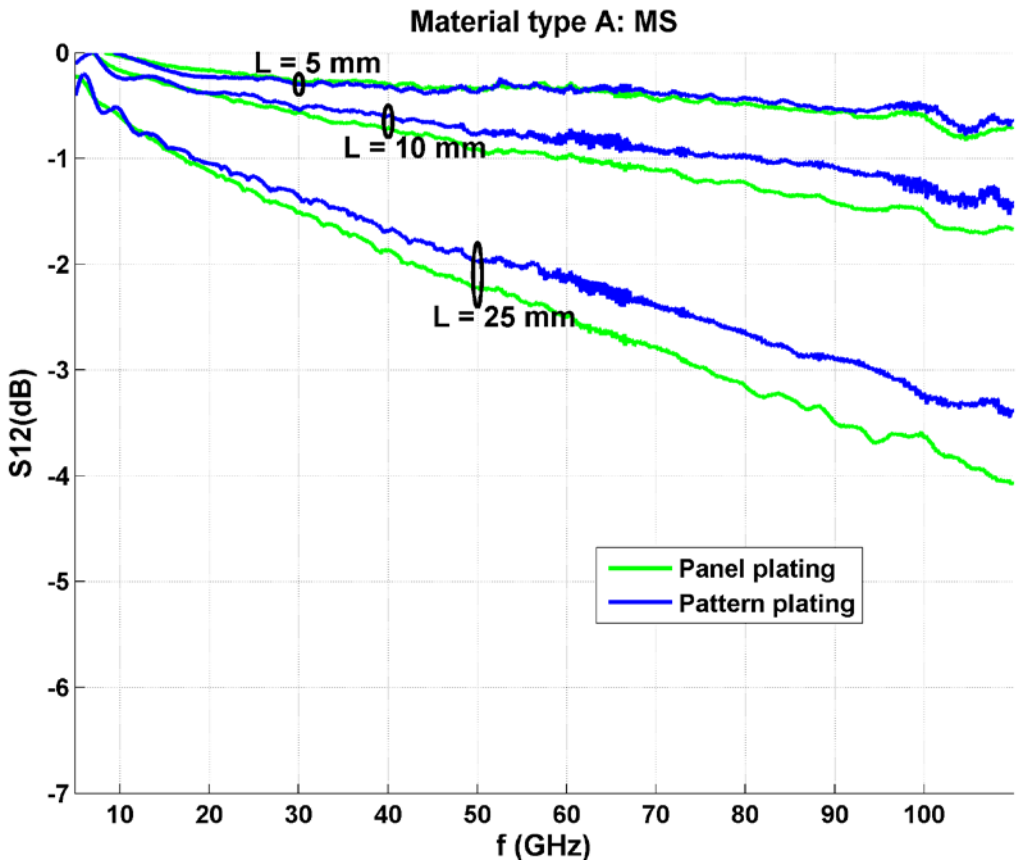

Figure 8: Material type A MS

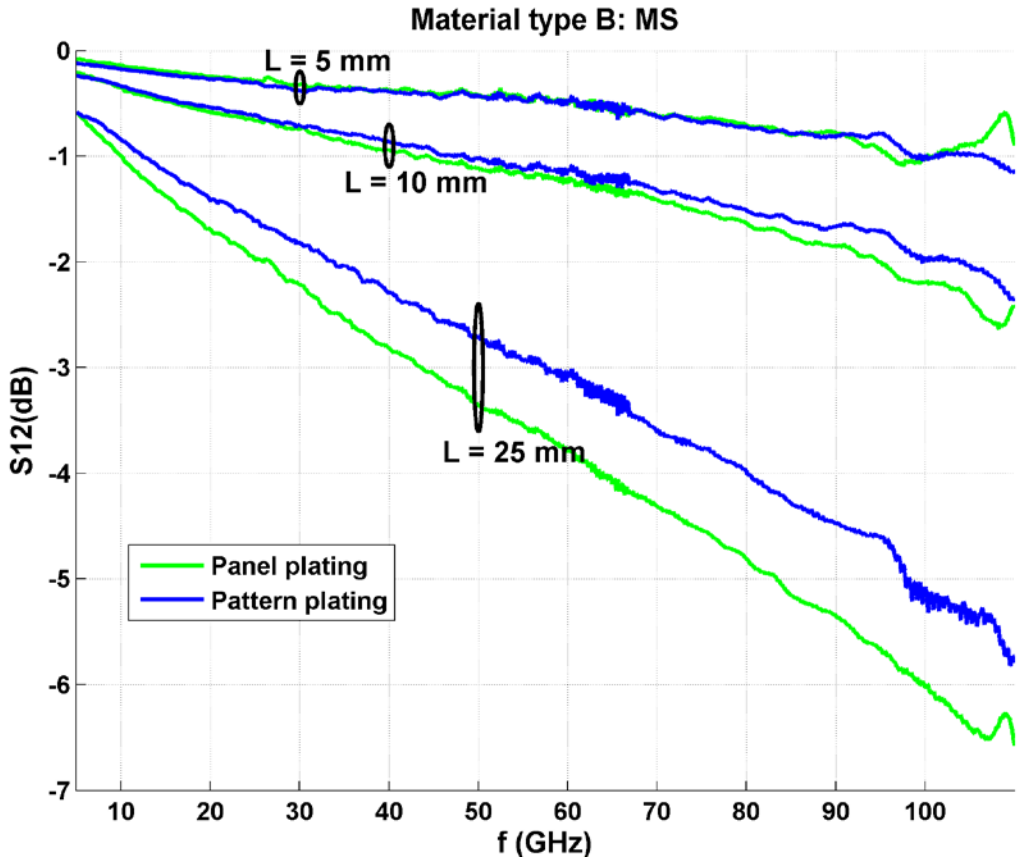

Figure 9: Material type B MS

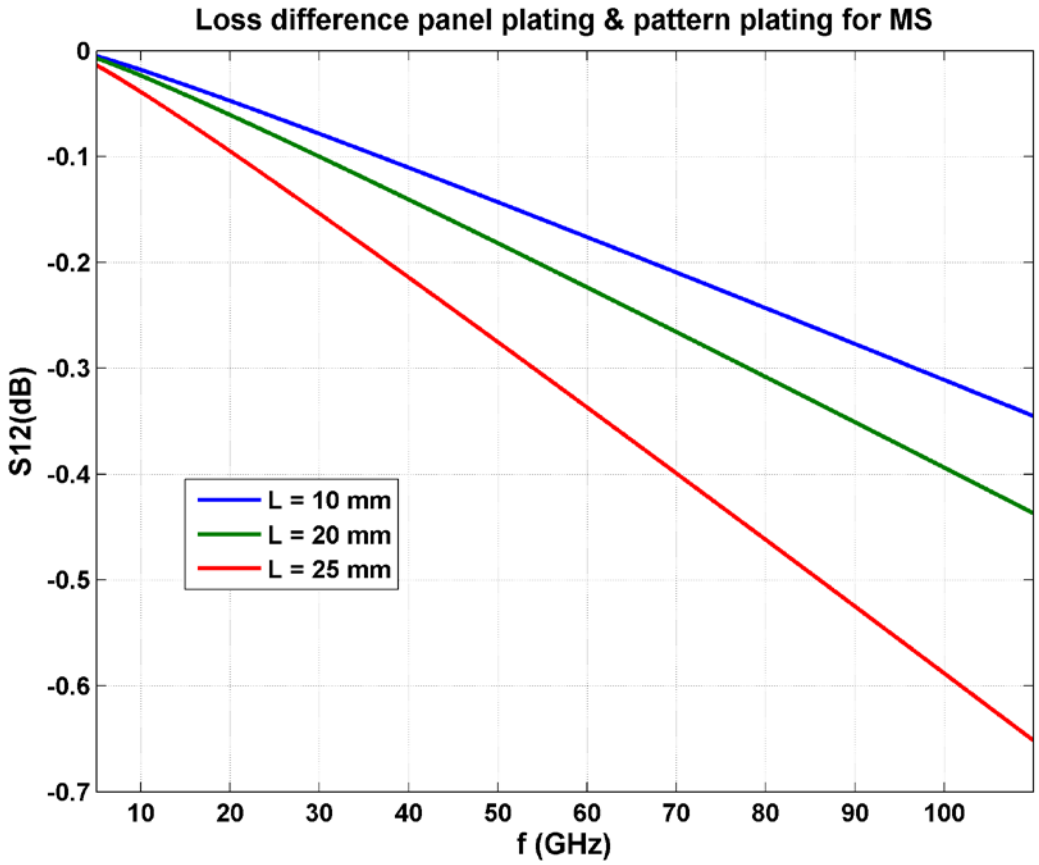

Figure 10: Loss difference MS

The second transmission mode is CBCPW. CBCPW typically exhibits larger losses over frequency for the same length L when it is compared to MS, as higher conductor loss occurs due to the additional ground planes on top of the structure.[3] In this case, as the dimensions of the measured samples imply a dominant wave propagation in the substrate, the total losses are just slightly higher as for the discussed MS lines. Figure 11 displays the measurement results for material type A. The difference of the losses of the structuring processes to be compared appears to be already present for very low frequencies and that for all three line lengths. For higher frequencies the impact of fabrication process does not seem to increase much. At 110 GHz for L = 20 mm the additional loss for pattern plating is approximately 0.42 dB, which is very close to the measured value for the similar MS line. For material type B (see Figure 12) resembling results as for material type A are achieved. By fitting the insertion loss for four different lengths of the CBCPW lines, in the same manner as it was done for MS, the results for material type B can be seen in Figure 13. The frequency dependence is quite different compared to MS as it seems that additional losses occur already at low frequencies, albeit, losses do not increase as steeply as for MS.

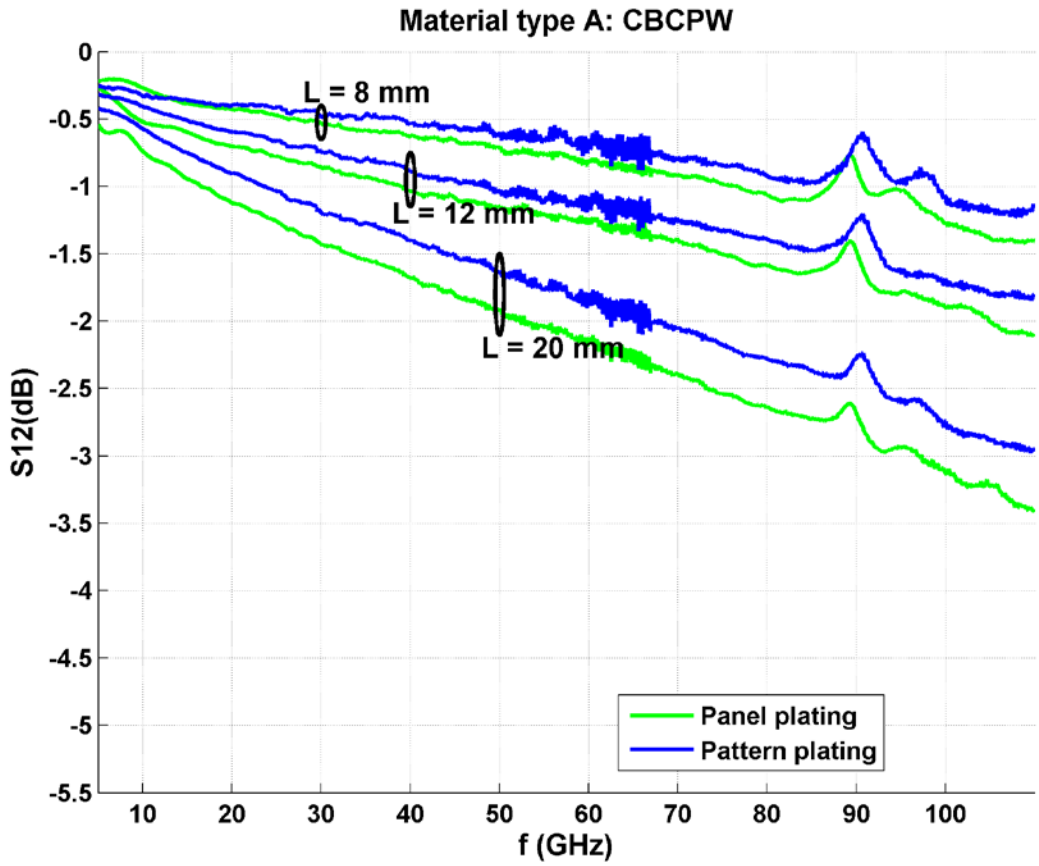

Figure 11: Material type A CBCPW

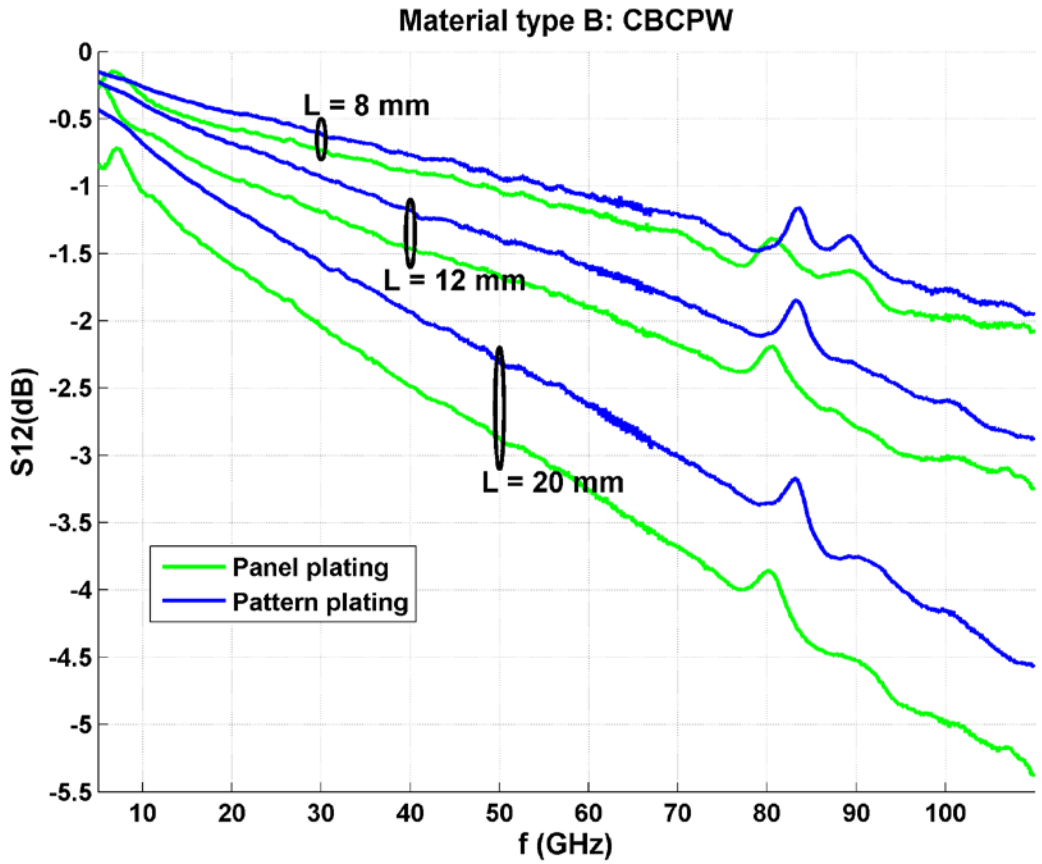

Figure 12: Material type B CBCPW

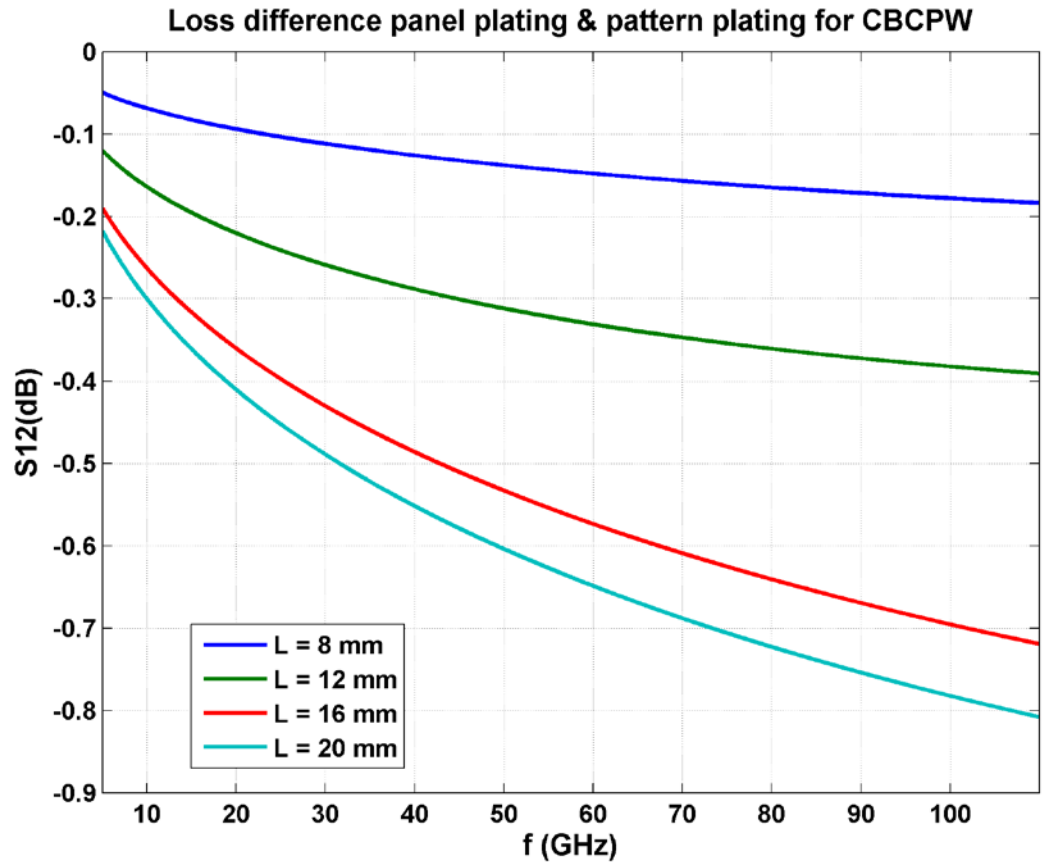

Figure 13: Loss difference CBCPW

The third transmission mode is SIW. The two investigated substrates have different values of Dk, however, for a comparison of the fabrication processes the same dimensions have been used for both materials. Therefore, the cutoff frequency slightly varies according to the difference of Dk. The measurement results for material type A are presented in Figure 14. For frequencies close to f_{cutoff} there is a slight difference noticeable in between the two manufacturing processes, nonetheless, this difference tends to be negligible as frequency increases. The losses for different SIW lengths are for 2.4 mm, 4.8 mm, 7.2 mm, and 9.6 mm, 0.34 dB, 0.73 dB, 1.06 dB, and 1.43 dB at 85 GHz, respectively. It can be concluded that there is a linear increase of the losses over L with an average of 0.358 dB for 2.4 mm SIW length. This value is valid from 65 GHz up to 100 GHz as losses are approximately constant for this frequency range. As the Dk of material type B is slightly larger than for material type A a small shift of f_{cutoff} can be noticed in Figure 15 compared with Figure 14. Material type B has almost overlapping results for both fabrication processes even for frequencies close to f_{cutoff}. Again a close to linear increase of loss can be observed for line lengths varying in between 2.4 mm and 9.6 mm with an average of 0.53 dB for 2.4 mm SIW length at 85 GHz. According to measurements, this value is valid from 60 GHz up to 90 GHz.

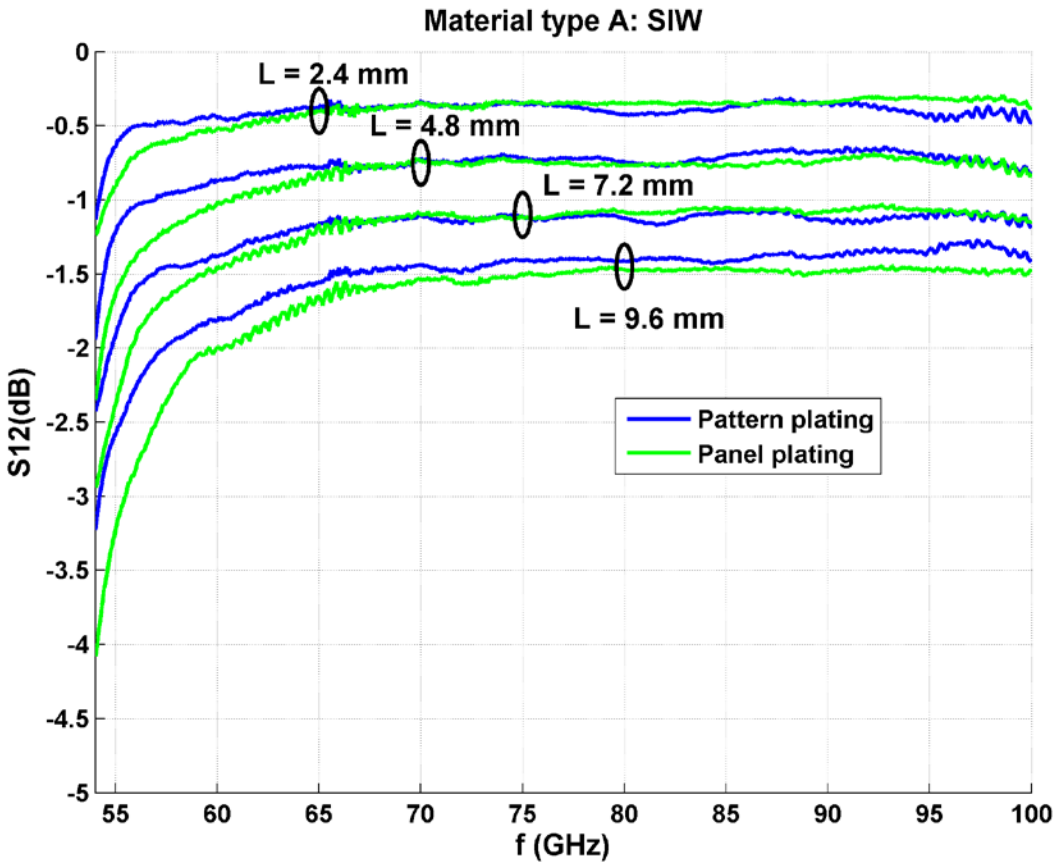

Figure 14: Material type A SIW

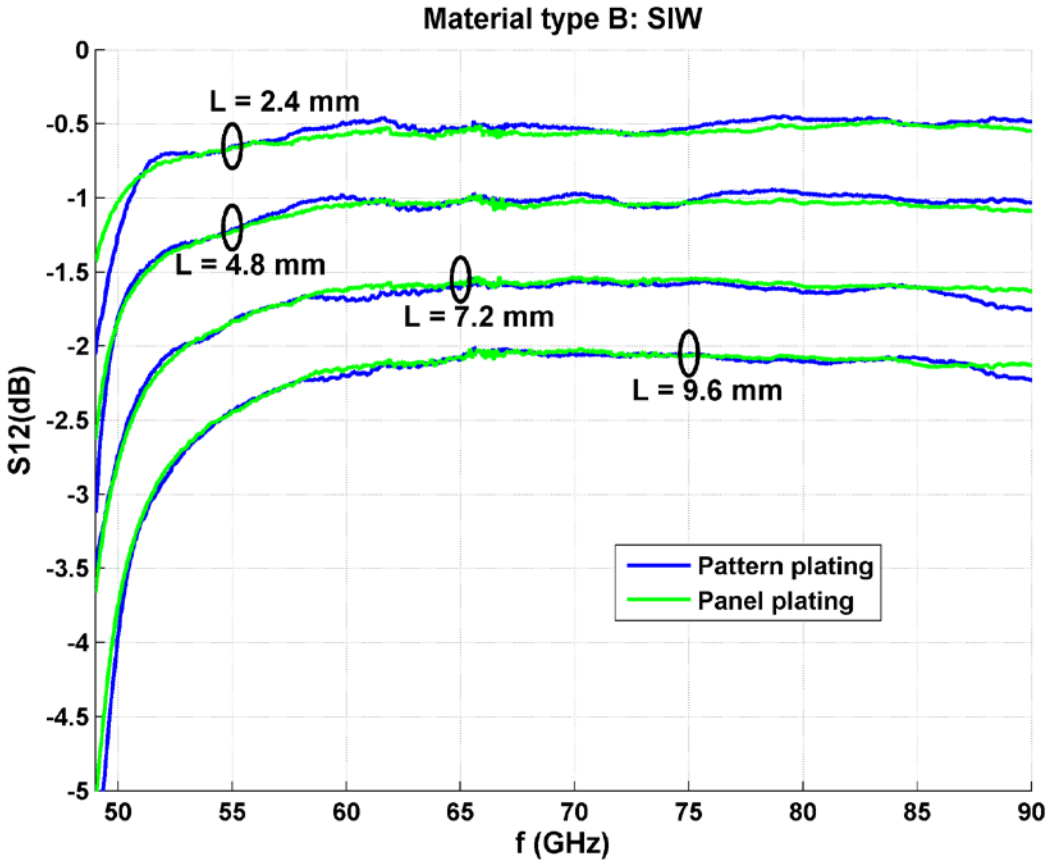

Figure 15: Material type B SIW

Conclusion and Outlook

Structuring processes show different deviations of line width and trapezoidal degree of the cross-section, which also impairs the applied immersion nickel/gold top plating. In a comparison of RF-losses, the fabrication processes have demonstrated certain characteristics for the investigated transmission modes, MS, CBCPW, and SIW. MS has shown that for lines lengths up to 5 mm there is no observable difference in terms of manufacturing process. Nonetheless, for longer lines a degradation of panel plating over pattern plating occurs, which increases quite linearly for the investigated materials. CBCPW exhibits slightly larger overall losses as MS. Due to the measurement results, the frequency dependence has shown a quite divergent behavior, as for low frequencies there is already a noticeable loss term present, however, with less overall increase over frequency than for MS. This behavior has been observed for both investigated materials. The SIW shows independent losses regarding the manufacturing process. For SIW, the losses can be assumed to be constant for frequencies above e.g. 65 GHz up to 100 GHz for material type A.

In a future work, these described observations will be extended to investigate the impact of different interconnection methods and top end surface platings. Additionally, for the CBCPW further designs will be made and measurements will be carried out for different gap widths. This is done to try to evaluate when the discussed change of loss difference starts to emerge compared to the MS line structure.

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