

CGA TRENDS AND CAPABILITIES

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ABSTRACT

The Column Grid Array (CGA) module is a high reliability JEDEC format package, with several options adaptable to end user needs. The dark or white ceramic thickness ranging from 1.4mm to 4.2mm and body sizes up to 52.5 mm JEDEC. The typical 42.5 mm CGA module is configured with a full array of 1089 I/O (33x33) with 1.27mm (0.050") pitch or 1657 I/O (41x41) with 1.00mm (0.040") pitch of 10/90 (Sn/Pb) columns and eutectic alloy solder connections. The CGA shows superior coplanarity and reliability compared to a BGA device and can be utilized on a JEDEC register package, bare chips, or capped modules with thermal management to include wire bond or Flip Chip C4 devices.

Substrate and System Level Reliability (SLR) is enhanced by a greater stand-off, flexible interconnection, improved thermal characterization, and improved thermal fatigue life of package solder joint. The contact integrity is where the Column Attach technology takes the lead over other Ball Grid predecessors. The need for complex, high density interconnects that can handle contact resistance, fatigue, CTE compliance, and ultra-high speed connectivity makes the process so valuable. The CGA has a proven long shelf-life and maintains wetting properties with proper board placement as well.

Description of the CGA Manufacturing Process and Flow

CGA modules (also called CCGA when referring to a ceramic substrate column grid array) are manufactured with a unique and precise tooling developed to be highly versatile to a number of module designs or configurations.

The repeatable process steps with inline inspections makes it a high yielding, robust, reliable interconnect operation. With this flexibility of operation, the process adjusts for low or high volume throughput when needed.

Highlights of the column joining process operation:

- a) Column loading in process boats as show in Figure 1
The process boats are designed to accommodate multiple parts simultaneously and may be configured to specific column patterns and footprints with customized overlay masks.
- b) Inspection of loaded column array:
This inspection step enables high yields particularly on complex array patterns.



Figure 1: Column loading operation

- c) The following step is a paste deposition on column tips as illustrated in Figure 2:

Unique carrier design gives repeatable and precise paste volume deposition to obtain regular solder fillets on finished products.



Figure 2: Paste screening for solder fillet

Inspection of Deposited Solder Paste Volume is a Guarantee of High Yields on Complex Array Patterns

d) Precise substrate positioning on paste array with a pick and place tool g column grid centrality and eliminates risks of solder bridging.

e) Solder reflow with inline convection oven:
In this process step, the substrate is unconstrained and benefits from a natural self-alignment of the solder as it is reflowed. This ensures a best fit array to accommodate the substrate tolerance.

f) Module extraction from process boat:

Precise automated vertical extraction eliminates solder column stress or shear.



Figure 3: Module extraction tool

g) CGA array cleaning removes flux residues.

h) Column planarization to a required array height in shown in Figure 4.

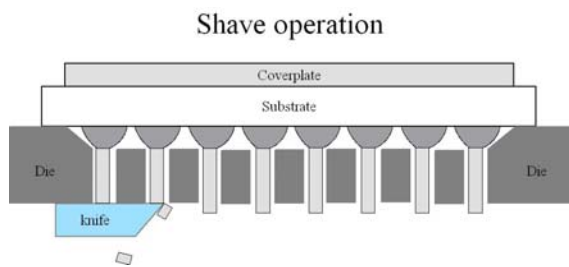


Figure 4: Column planarization concept

Example of the manually operated die used to protect the columns during the column shave operation is illustrated in Figure 5.

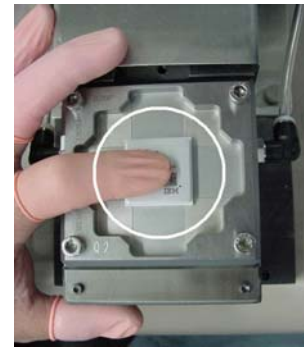


Figure 5: Die used for planarization in manual mode

i) Inspections – X -ray

Although the high lead columns do not permit a complete solder fillet inspection for voiding, it is the peripheral solder fillet voiding which is most critical for reliability. The high DNP (distance to neutral point) column locations of the package is also more sensitive to voiding from a reliability standpoint.

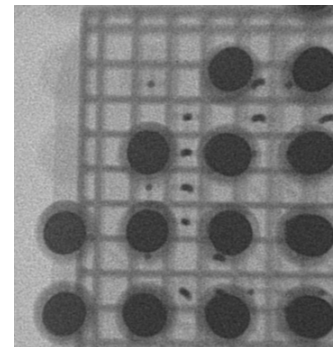


Figure 6: Typical image of a X-ray inspection

Inspections – Coplanarity:

The seating plane maximum specification is 150 μm however; the planarization process guarantees a uniform and repeatable column tip plane, which is optimal for module placement at card level.

An automated inspection and handling tool also guarantees the X-Y position and integrity of the column tips prior to safely positioning the modules in their transportation trays in JEDEC standard format.

The diagram (Figure 7) provides a schematic process flow of the complete bond and assembly steps from chip join to post test inspection.

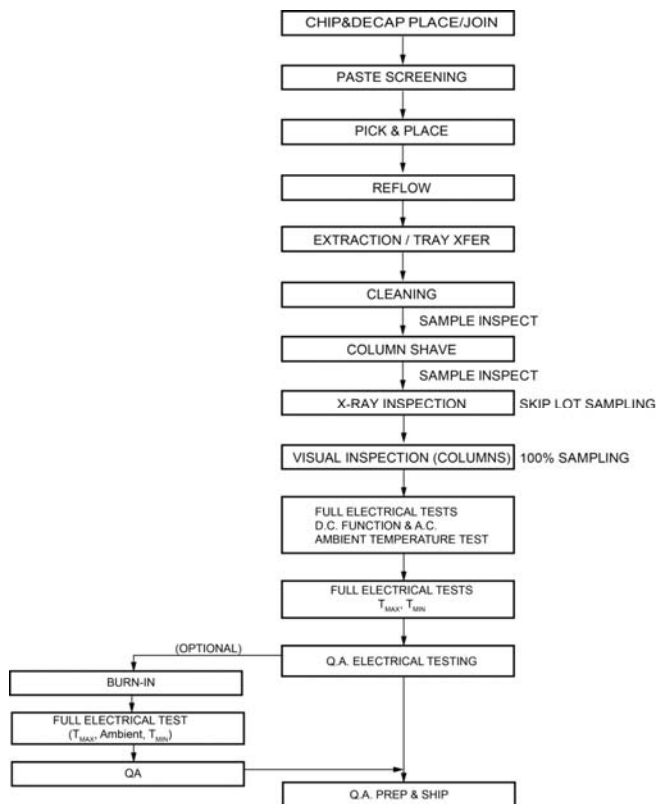


Figure 7: Complete Bond and Assembly process flow

Specific Advantages of the Column Joining Process:

As illustrated in the previous sections, the CGA tooling is adaptable to many product configurations, key inspections of the CGA process guarantees uniformity of the end product and high reliability. The shaving / planarization process can be adjusted to specific column heights depending on the end application. The final column height will modulate the reliability of the package.

Reliability Data

IBM conducted reliability monitors on CGA Test Vehicles modules for many years; typically between 20 to 60 modules per stress and per year. Modules were joined to a card before accelerated thermal cycling (ATC) and Highly Accelerated Temperature and Humidity Stress Test (HAST). Two groups of parts were stressed over the years: prime and rework modules. Prime modules were built using 1 pass of column joining (CGA process) while reworked modules saw a first pass of column joining followed by a columns removal step and then a second pass of column joining.

a) Hardware description:

The 42.5mm daisy chain multi-layer alumina carrier has a 41x41 grid array with 6 depopulated columns on each corner, 1.00mm pitch for a total of 1657 columns and an overall thickness of 3.75 mm. The 10/90 column geometry is an important design point that can modulate the final reliability, the nominal dimensions of the solder columns for the test vehicles are 2.21 mm in height (0.087in) and

0.51 mm (0.020in) in diameter on substrate pad sizes of 0.69 mm. Other dimensions of columns were tested, and it was found that the 87 mils column has the advantage of superior reliability while mitigating other drawbacks such as mechanical fragility or risk of electrical crosstalk.

b) Stress tests description:

Thermal cycling is used to address the fatigue of the connection between the module and the card. Thermal cycling conditions are the following: 0 to 100C with a minimum of 5 minutes in the low and high temperature range. Typical profile is illustrated in Figure 8.

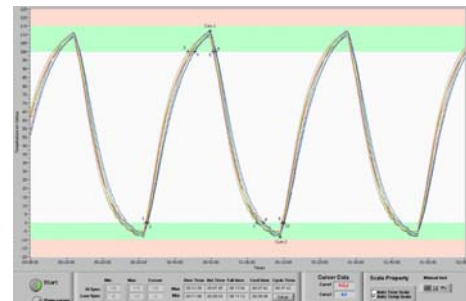


Figure 8: Typical ATC profile performed in a single chamber, about 1.5 cycles per hour

Biased HAST is used to address potential contamination issue between columns which can lead to a migration problem. HAST conditions used to stress CGA on card are: 130C/85%/5V/+33.3psia for 96 hours.

c) CGA stress data:

ATC data from the last 8 years (2007 to 2014) was used to draw the distribution graph shown in Figure 9:

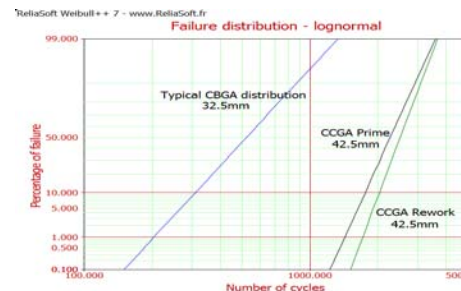


Figure 9: Failure distribution of CGA prime and rework compared to CBGA

The graph (Figure 9) shows a clear reliability improvement when columns are used instead of solder balls. It can be noted that there is a slight delta between prime and rework data sets which could be explained by the number of parts put in stress (20% less parts in the rework group) and by the fact that the residual solder on the I/O pads from the first pass of column joining helps the fresh solder from the second pass of column joining to wet higher on the column

resulting in a slightly different solder joint geometry. The more important height of the solder fillet on the rework parts could delay the failure by a few cycles.

Failure by fatigue occurs just above the solder fillet either carrier or card side as shown in Figure 10.

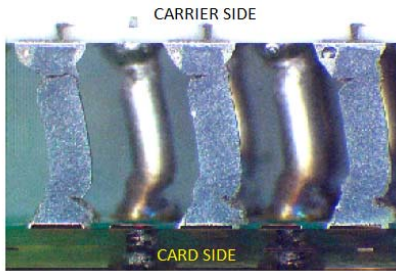


Figure 10: Typical fatigue mechanism

As for the biased HAST data, it can be noted that no fail on 286 modules is reported over the test years.

The reliability monitors performed on CGA modules show great reliability data and consistency of the results from the start of the CCGA program and all through the production years.

Field Applications for CCGA

As shown in Table 1, Column grid arrays can provide complex and high density interconnects that can handle contact resistance, fatigue, CTE compliance, and ultrahigh speed connectivity.

Table 2: Package Types and Products for CGA

Process	Advanced RF RF-CMOS and RFID Power Management	CMOS Image Sensors Non-Volatile Memory Solutions Mixed Signal
IP Technology	SRAM & DRAMM DDR1, DDR2, QDR Network Processors	Hyper Transport & Dual TDMS PCI Express & Serial ATA High Speed SERDES
Applications	Graphics & Audio/Video Automotive GPS Industrial	RFID Tags Medical Aerospace & Defense Automotive
Products	FPGA A/D & D/A SoC, MEMS, & RF SiP, SoC Integration	ASIC High-Speed Memory High-Density Memory Flash

TEST of the CGA:

Pre and post electrical test mandates the use of a dedicated load board designed to a 50-Ohms environment.

It facilitates testing accuracies at speed AC timings, SERDES testing, noise and jitters tests, and AC at speed binning.

THE CGA Testing Process:

Having very high test coverage and the ability to detect shifts in device performance is critical, as these parametric shifts could point to an underlying reliability issue that could potentially go undetected.

Test tools, state-of-the-art hardware, and software expertise, allows for development of robust test solutions to write comprehensive test programs for complex FPGA’s, processors, mixed signal, and RF devices. This will always result in providing the most accurate assessment of reliability of any semiconductor device no matter what the complexity.

For CGA ATE testing, STS’s proprietary “Hammer file,” is the differentiator in reliability of the CGA joint. This file is designed to program the CGA to its maximum combination and block configuration, and then test the completely programmed CGA for full dynamic, DC, and at-speed AC tests. Power and transient tests are also conducted under worst-case populated configurations. At-speed test and application-specific usage configurations are also used to assist in generating the worst-case electrical specification limits at worst-case environmental use.

Burn-In of Complex CGA’s

A unique approach is needed to overcome the temperature regulation barriers of high power dissipative devices that normally are associated with a CGA. ITC360™ is the most critical tool for conducting individual junction temperature regulation, as it provides heating and cooling test simulation. It is an alternative to the conventional burn-in test and unifies temperature gradients of specification temperature, actual operating temperature, ambient temperature, and surrounding temperature.

This unique solution breaks the boundaries of technology, performs Level II burn-in and tests high power dissipative devices enabling thermal regulation. ITC360™ can be conducted directly on the bench without the use of interconnect devices. Real-time monitoring allows the user to predict early detection of overheating to avoid deterioration and defective components, modules, or systems.

This product thermally manages a high power dissipation of 150W and 250W. ITC360™ controls individual temperature of the DUT (device-under-temperature) and temperature of the immediate surroundings to prevent the devices from overheating or under heating.

Level 2 Qualification Plan for CGA

It is important to understand the physics of surface mount solder joint failures during Level 2 (board) reliability testing. This qualification plan takes into consideration solder joint reliability as it relates to the environment and conditions in real application.

Most failures in electronic components that are mounted onto a circuit board occur at the solder-joint interface. These failures typically result directly from the strains developed at high and low temperature extremes. Different rates of expansion of different materials are exhibited during cyclic temperature variations typical of operational use. Temperature variations also result from different coefficients of thermal expansion, or cyclic differential expansion. Hence, temperature cycle plays a very important role in Level 2 qualification testing of the CGA mounted to the PCB.

CONCLUSION

The CGA remains the superior interconnect for thermal management and reliable interconnect for high complexity

devices used in high reliability applications. The IBM patented materials and processes that includes process control, accuracy, and precision of the CGA flow, offers the strongest and most reliable column attach process in the market place. Testing of the LGA and CGA provides the assurance of proper column attach and wetting, to ensure the device will operate at speed across specific temperature ranges and meet requirements per the data sheet. The reliability data supports that CGA remains a viable solution for the high reliability market place.

REFERENCES

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