CAVITY BOARD SMT ASSEMBLY CHALLENGES

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ABSTRACT
There is a continuing trend for notebook computers, cell phones and other handheld electronic devices to become thinner and thinner. One of the solutions to reduce the thickness is mounting the tallest components into a cavity in the printed circuit board (PCB). In this method, the lands of the package that needed a height reduction are fabricated in a recess in the mother board. Paste printing and components placement take place on the surface of the board and in the cavity.

The intent of this study is to identify the challenges related to assembly of a package into a cavity on the board, and establish the best known method for SMT assembly success. The paper will examine a System-in-Package (SiP) BGA (ball grid array) package assembly into a cavity in a mother board. The paper will describe the challenges facing the PCB design and fabrication. It will share the SMT assembly method and the impact of different board suppliers, stencil technology and squeegee design. It will discuss the warpage of the PCB and its effect to SMT results. Finally, the paper will summarize the challenges and provide best known method to overcome them to have a successful assembly in a cavity board.

INTRODUCTION
In mobile consumer electronics, there is a perennial need to reduce the space consumed by the motherboard. This need is commonly driven by the desire to shrink a product's form factor, while also increasing battery capacity. Notebook computers are certainly not immune to this challenge.

Reducing the space consumed by a notebook computer motherboard can be approached along several vectors. Reducing the size and spacing of components placed on the motherboard is a logical first step. Many components have continued to be introduced in progressively smaller packages while assembly capabilities have evolved in parallel to allow these components to be placed closer together. These efforts certainly have a positive impact in reducing the area consumed by the motherboard. The thickness of the motherboard assembly to a first order is limited by the tallest component. In many designs then, the tallest components will receive a great deal of focused effort in searching for thinner alternatives. When these efforts are exhausted, there may still be a need to reduce the motherboard thickness, and that is what drove the effort to evaluate placing components into a cavity on the motherboard printed circuit board (PCB), or what is referred to as Component-in-Cavity (CiC).

The concept behind CiC is straight-forward. If the tallest component(s) on the motherboard can be placed into a recession created in the motherboard, their thickness relative to the components on the surface of the PCB will thus effectively be reduced (Figure 1).

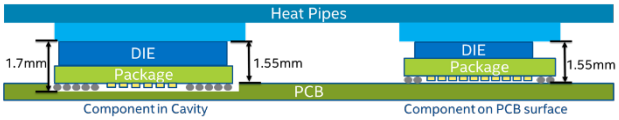


Figure 1. CiC example problem

While this concept may be straightforward, its implementation is not, and that implementation is the focus of this paper.

This paper will discuss two primary challenges to the successful implementation of CiC. In the next section, challenges associated with the PCB test vehicle will be discussed while subsequent sections will focus on the SMT assembly of components into the cavity and the impact of the PCB design on assembly.

TEST VEHICLES
The board design used in the study had 14 layers, was 0.93 mm thick, and 127 mm x 127 mm in size, with an OSP surface finish. The board had identical land patterns for a BGA at two different locations. One was placed on the board surface and the other inside a cavity in the board. The cavity size was 30 mm x 48 mm. It was on the fourth layer of the board with a nominal depth of 187 µm. There were also four DRAM land patterns outside of the cavity. In order to study supplier-to-supplier variations that occur during high volume manufacturing (HVM), the boards were ordered from three different board suppliers. Figure 2 shows the top view of the board test vehicle.

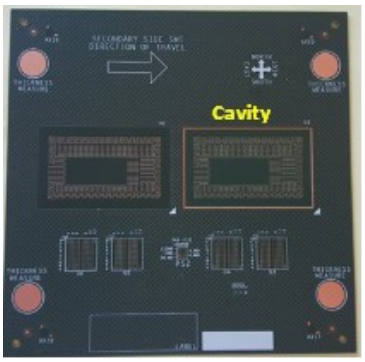


Figure 2. Top View of the Board Test Vehicle

The packages used in this study were Flip Chip Ball Grid Array (FCBGA) packages for a SiP design containing three silicon die. The package has 1168 balls, which were arranged in a non-regular grid array with a minimum 0.65 mm pitch. The package size was 24 mm x 42 mm. It had a stiffener to control the package warpage during reflow. The top and bottom view of this package is shown in Figure 3.

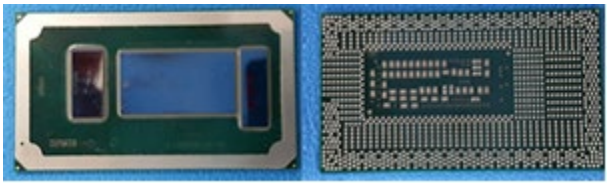


Figure 3. Top and Bottom view of the FCBGA SiP Packages

CiC PCB CHALLENGES – INCLUDING THE FORMATION OF THE CAVITY (LASER STOP, ETC.)

The fundamental challenge with fabricating the CiC PCB is that it is necessary to remove a limited number of layers of material from an area of the PCB, to expose a component footprint consisting of copper pads and soldermask. Intel has significant experience working with high volume (HVM) PCB fabricators to enable the removal of layers from a region of the PCB. When all layers in the region are removed the design is termed Hole in Motheboard (HiMB). When only a partial number of layers are removed the design is termed Recess in Motherboard (RiMB) [1]. These designs are currently utilized on notebook motherboards when system architects are working to achieve a reduction in thickness.

The unique attribute for CiC is that the bottom of the cavity requires both component pads and soldermask, which significantly increases the complexity of the fabrication process, when compared to HiMB and RiMB designs.

Cavity Stackup

In order to develop a process for CiC, a test vehicle (TV) was developed as a proxy for a real product design. This test vehicle was focused on a specific application so some details described will be specific to that application. However, where possible, the results described will be generalized. The PCB stackup for the CiC test vehicle is shown in Figure 4. This stackup consists of a 6 layer buried core with plated through hole (PTH) vias as well as a single layer of microvia. Additionally, 4 build-up layers are added to either side of the buried core, resulting in what is referred to as a 4-6-4+ stackup.

L	Layer name	Thickness (um)	drill
	Soldermask	20	
1	Copper	25	
	Prepreg	40	
2	Copper	16	
	Prepreg	45	
3	Copper	16	
	Prepreg	45	
4	Copper	16	
	Prepreg	46	
5	Copper	22	
	Prepreg	45	
6	Core-Copper	16	
	Core	50	
7	Core-Copper	31	
	Prepreg	74	
8	Core-Copper	31	
	Core	50	
9	Core-Copper	16	
	Prepreg	45	
10	Copper	22	
	Prepreg	46	
11	Copper	16	
	Prepreg	45	
12	Copper	16	
	Prepreg	45	
13	Copper	16	
	Prepreg	40	
14	Copper	25	
	Soldermask	20	
	Thickness	940	

Figure 4. CiC Board Test Vehicle Stackup

For the specific application, the component placed into the cavity was required to have an effective thickness reduction of 200 µm, including any manufacturing variation. Additionally, to support fabrication of a cavity with a component footprint at its bottom it was necessary for the bottom of the cavity to align to one of the copper layers in the stackup. Further, the PCB fabricators who could build this cavity would rely on a laser to define the perimeter of the cavity. This would require the use of a copper ring surrounding the perimeter of the cavity at the desired depth to act as a laser stop. This resulted in two cavity designs that could potentially be utilized.

The cavity design shown in Figure 5 removes 3 copper layers in the cavity area so the component footprint would be located 4 layers deep into the stackup. The nominal depth of this cavity is only 187 µm which does not meet the 200 µm target.

9	Core-Copper	16					
	Prepreg	45					
10	Copper	22					
	Prepreg	46					
11	Copper	16	187um cavity depth		-tol	Recess Depth	+tol
	Prepreg	45			30	45	60
12	Copper	16			6	16	26
	Prepreg	45			30	45	60
13	Copper	16			6	16	26
	Prepreg	40			25	40	55
14	Copper	25			15	25	35
	Soldermask	20					
	Thickness	940	Cavity depth	RSS	156	187	218

Figure 5. TV Cavity design with 3 copper layers removed

The cavity design in Figure 6 is the result of removing 4 copper layers from the cavity area so the component footprint is located 5 layers deep into the stackup. The nominal depth of this cavity design is 249 µm which is sufficient to meet the 200 µm depth requirement.

9	Core-Copper	16				
	Prepreg	45				
10	Copper	22	249um cavity depth	-tol	Recess Depth	+tol
	Prepreg	46		31	46	61
11	Copper	16		6	16	26
	Prepreg	45		30	45	60
12	Copper	16		6	16	26
	Prepreg	45		30	45	60
13	Copper	16		6	16	26
	Prepreg	40		25	40	55
14	Copper	25		15	25	35
	Soldermask	20				
	Thickness	940	Cavity depth	RSS	213	249	285

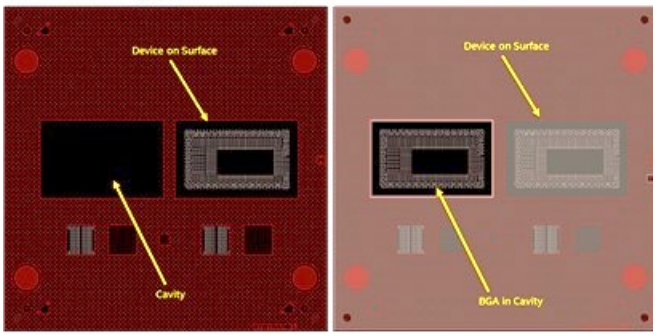
Figure 6. TV Cavity design with 4 copper layers removed

The details around considering these two cavity depths will be described in a following section.

TV Design

The TV that was created to support development of the cavity SMT process is shown from the bottom side in Figure 7.

Figure 7(a) illustrates the PCB bottom artwork layer. The cavity area as well as a BGA footprint located on the PCB bottom surface are visible from this perspective. Clearly there is no information in the cavity when viewing only the PCB bottom, as the cavity is defined on layer 10 of the PCB. The PCB having component pads and soldermask on multiple layers introduces some complexity to the PCB fabrication and to some steps in assembly process. These processes are accustomed to having component pads and soldermask defined on at most two layers. Determining a method to communicate this information to PCB fabricators, fixture fabricators, solder paste inspection tools, and other processes that are dependent on the PCB artwork is crucial to avoid additional cost and delays.



(a) Bottom layer artwork **(b)** Bottom layer and layer 10

Figure 7. CiC Test Vehicle PCB artwork

Figure 7(b) illustrates the BGA footprint in the cavity which is located on the PCB layer 10. Including BGA footprints inside and outside of the cavity provided the opportunity to evaluate the SMT process capability for the device placed in the cavity relative to the same device placed on the PCB surface.

PCB SUPPLIER CHALLENGES

Fundamentally, the 4-6-4+ stackup can be built by a large number of potential HVM fabricators. Creating a cavity in the PCB reduces the number of potential HVM fabricators, but the capability is still readily available in high volume. Requiring that the cavity have both copper pads and soldermask in the bottom of it dramatically reduces the number of potential fabricators. In early 2017, 14 HVM PCB fabricators were contacted to assess their capability. Of the 14 fabricators contacted, 4 were able to demonstrate experience building boards with similar cavities. They were targeted to support the build. Of those 4 fabricators, 3 were ultimately chosen to build the TV.

As described previously, there were two cavity depths under consideration for the TV design. One removed three metal layers and resulted in a nominal cavity depth which was slightly less than needed. The second removed four metal layers and had a nominal depth that was sufficient.

As can be seen in Figure 8, removing 4 metal layers from the 4-6-4+ stackup would place the bottom of the cavity on the surface of the buried core layer. This would require all the BGA pads to be connected to a plated through hole (PTH) via. For some fabricators this would require the PTH vias be plugged and plated over which was not feasible for their cavity manufacturing processes. For that reason the TV design with 3 metal layers removed was pursued.

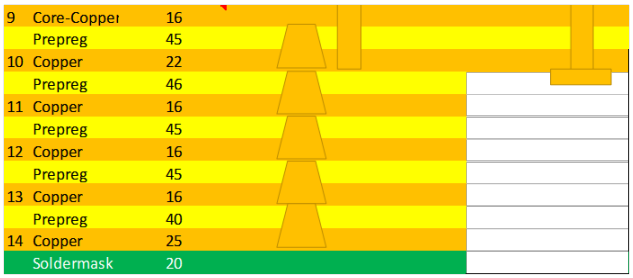


Figure 8. Cavity with 4 metal layers removed

CAVITY MEASUREMENTS

Cavity Depth

Cavity depth was initially seen as critical if using a two level 3-D stencil for applying solder paste. Ideally, the stencil and PCB cavity are designed for the same depth. However, the stencil itself will have some tolerance between the two levels, and the PCB will also have some tolerance to the cavity depth. In the extreme condition where the cavity is at its minimum depth while the stencil is at a maximum (or vice versa), the resultant stencil stand-off could affect paste printing either inside the cavity or on the surface, as illustrated in Figure 9.

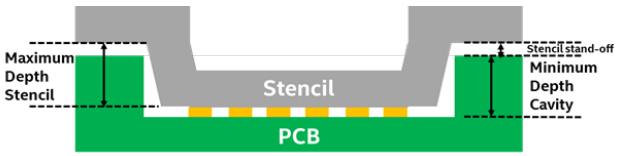


Figure 9. Illustration of PCB and stencil tolerance impacting stencil stand-off

The designed cavity depth was 0.187 µm. On average, however, the measured cavity depths were much greater for all suppliers. Additionally, through measurements of the cavity depth, it was observed that the cavity could have a complex shape which could also be fabricator dependent. These shapes are shown in Figure 10. The impact of this shape on SMT yield will be discussed in a later section.

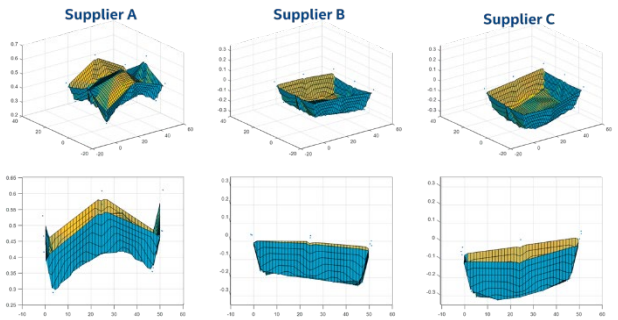


Figure 10. Cavity shape comparison for three PCB suppliers (at room temperature)

Surface to Cavity registration tolerance

Again if using a 3-D stencil that applies solder paste to both the PCB surface and the cavity bottom in the same pass, the positional tolerance of features on the PCB surface and cavity would need to be well controlled. The X-Y position of four alignment fiducials, four BGA pads inside the cavity, and four BGA pads on the PCB surface were measured on several boards. Measurements for the same points were also extracted from the PCB computer aided design (CAD) database to serve as a reference for evaluating the difference between the cavity and surface locations. The approximate locations of these points in the cavity is shown in Figure 11.

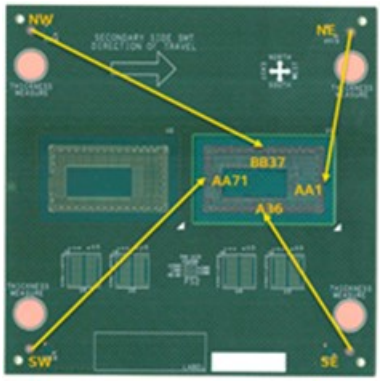


Figure 11. Approximate location of cavity registration measurement points and their associated labels

The distance between an alignment fiducial and BGA pad was calculated and compared to the same distance calculated from the PCB CAD database. For example, looking at the surface to cavity registration tolerance for BGA pad BB37:

$$Distance = \sqrt{(Fiducial\ X - BGA\ X)^2 + (Fiducial\ Y - BGA\ Y)^2}$$

$$Cavity\ Registration\ Tolerance = Distance\ PCB(Fiducial\ NW \rightarrow Cavity\ BGA\ BB37) - Distance\ CAD(Fiducial\ NW \rightarrow Cavity\ BGA\ BB37)$$

Similarly,

$$Surface\ Registration\ Tolerance = Distance\ PCB(Fiducial\ NW \rightarrow Surface\ BGA\ BB37) - Distance\ CAD(Fiducial\ NW \rightarrow Surface\ BGA\ BB37)$$

It would be expected that since the fiducial and surface BGA are created in the same fabrication steps, there should be minimal difference in their locations relative to the CAD database. However, given that the cavity features are three layers below the surface, it would be possible for layer to layer imaging tolerances to accumulate as the PCB layers are built-up. The results of these measurement calculations are shown in Figure 12.

There has previously been no design rule in place for this surface to cavity registration tolerance so the effort with the test boards has been to bound the amount of mismatch and determine if it is impactful to the SMT process. In these test boards, the worst case surface to cavity registration tolerance was <75 µm.

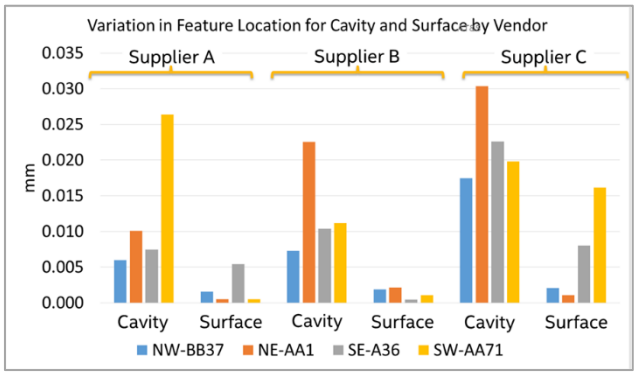
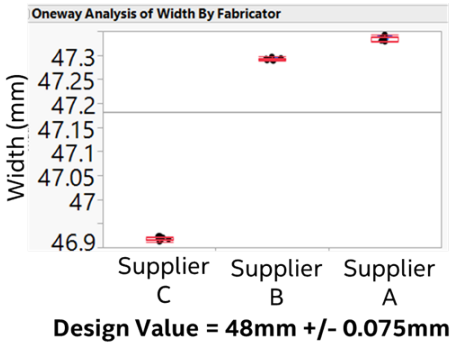


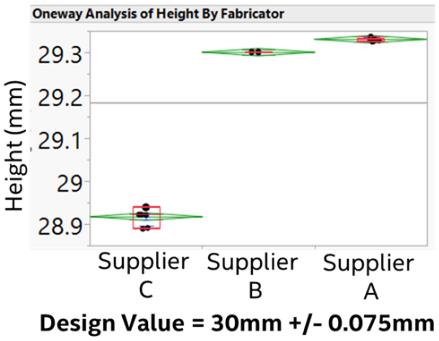
Figure 12. Measured vs Drawn registration error

Cavity opening tolerance – The tolerance on the size of the cavity opening was initially deemed important as it was unknown at the time of the TV design how tight a fit the stencil would require to the cavity opening. A surface profile tolerance of 150 µm was added to the cavity x-y dimensions in order to minimize the variation.

None of the suppliers met the 150 µm surface tolerance as all the cavities measured were smaller than allowed by the surface tolerance, as shown in Figure 13.



(a) Cavity X-Dimension



(b) Cavity Y-dimension

Figure 13. Box Plots of Cavity Dimensions

While the dimensions were smaller than the surface tolerance allowed, it was noted that within a given supplier the x-y size was generally repeatable. This is shown in Table 1. But to have a design specification that would work across multiple fabricators a larger nominal surface tolerance of 400 µm would be more achievable.

Table 1. Cavity Dimensions' Tolerance

Supplier	X - Tolerance (mm)	Y-Tolerance (mm)
A	+/-0.065	+/-0.011
B	+/-0.003	+/-0.008
C	+/-0.012	+/-0.016

STENCIL SELECTION AND DESIGN

In order to print solder paste into a cavity on a two level board, a 3D stencil is required. A 3D stencil is a stencil comprised of different print levels [2]. In this case, there are two levels: the board surface and the board cavity. This differentiates it from a step up and step down stencil that has only one level, the board surface, which is used to print paste to achieve a thinner or a thicker deposit by varying the thickness of the stencil foil.

There are a few technologies available to build 3D stencils. The experiments in this study focused on three stencil technologies: electroformed, machined, and welded. Electroformed stencils use a metal deposition process to build a stencil and cavity around a built mandrel. The foil thickness grows as a function of time so the process can create any stencil thickness. It forms a good quality stencil with a very smooth surface. A machined stencil requires using a machine tool to remove material from the original metal sheet to create a cavity. Some of the advantages to this method are that it provides options to selectively define the stencil thickness and to have a different thickness inside the cavity. It can also selectively machine a chamfer or have straight walls as selected by the design. Finally, a welded stencil has a hole cut into the foil where the cavity is needed. A cup is spot-welded on the foil to cover the hole. In this technology there is larger keep out zone (KOZ) needed for the welding process. It also provides limited cavity depths due to set foil thickness and alignment challenges. Figure 14 shows images of the stencil cavity from all three 3D stencil technologies.

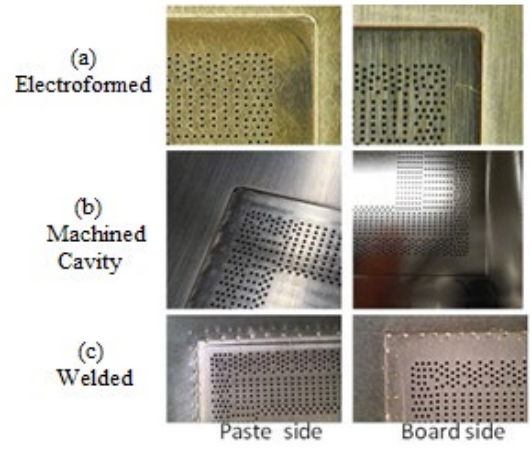


Figure 14. Stencil technology

Each stencil technology has a unique signature that can impact the selection of that technology. Fig 14(a) shows an electroformed stencil with a smooth surface and a taper on both the paste and board side of the cavity walls. This taper is required in the electroforming process for easy release from the mandrill. Figure 14(b) shows a machined cavity where the paste side has round corners while the board side has flat walls due to the machining process. The welded stencil in fig 14(c) has flat walls with no taper and a couple rows of spots from the welding process. The surface near the welded area is coarser, and the KOZ from the BGA aperture is smaller compared to the other stencils. There is no one stencil technology solution that can fit all applications. Selection should be made to fit the particular application in terms of build quantity, lead time, budget, cavity depth and KOZ. Table 2 provides comparisons of one design case for the different stencil technologies to a standard laser cut stencil in terms of cost and lead time. These estimates can change depending on the design.

Table 2. Stencils cost and lead time

Stencil technology	Estimated Cost	Lead Time
Laser Cut POR	1X	3 days
Electroformed	15X	4 weeks
Machined	5-8X	2½ weeks
Welded	1.5X	4 days

In this evaluation, the stencils' apertures on the BGA were 330 µm square. The stencil thickness was 100 µm (4 mils). Since excessive paste was expected in the cavity, an additional machined stencil was made with reduced stencil thickness in the cavity area. The thickness was only 90 µm (3.5 mils) to reduce the risk of bridging. As mentioned, stencils from all three technologies were used in the evaluation.

SMT SET UP CHALLENGES

In order to use a 3D stencil with a cavity on a paste printing machine, a metal blade squeegee with a two slits is used. Figure 15 shows a squeegee with two slits. The part of the squeegee between the two slits is the section that is riding inside the cavity. It has a clearance of about 0.15mm from the cavity wall on each side in order to compensate for positional errors and be able to apply the full pressure to the cavity.

Figure 15. Slit squeegee

It is critical during the printer set up to align the slit with the cavity. This may require a few trials and needs to be done to each blade separately since each blade has its own holder. A good practice is to run the blade with low pressure and low speed on the stencil and observe the position of the slit. After adding the paste to the stencil, the paste lines will help to determine the correct position.

(a) (b)

Figure 16. Slit Squeegee Alignment

Figure 16 (a) shows an improper set up where the squeegee blade needs to move to the right. The slit to the left of the cavity is riding outside of the cavity walls, causing excessive solder paste. Figure 16(b) shows the proper setup of the squeegee slit in the cavity where both slits are riding inside the cavity. Some paste printing machine suppliers offer a lateral squeegee adjustment, which makes this task much easier. Figure 17 illustrates a squeegee blade holder with a lateral squeegee adjustment installed.

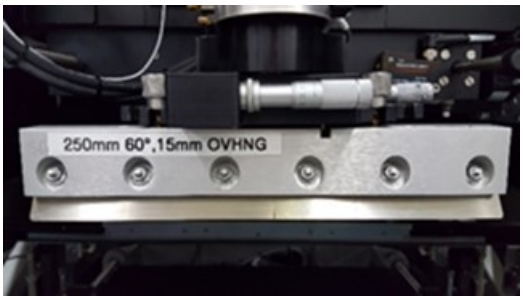


Figure 17. Slit Squeegee with a lateral adjustment head

There are no special considerations for setup in the pick and place (PnP) machine or the reflow oven due to the cavity. It is worth mentioning that in the board file the BGA pads in the cavity are non-existent on the first layer as they normally are on standard boards. Some SMT tools cannot deal with multilevel BGA pads. For example, solder paste inspection (SPI) tools will need to have a modified board file which transfers the paste layer to one level. The board file image in Figure 7 illustrates this issue. Figure 7(a) is the information typically provided to the SPI tool, which clearly provides no reference to the BGA pads located in the cavity. Figure 7(b) is the result of merging the PCB bottom and the cavity layer artwork such that all of the necessary information can be provided to the SPI tool.

PRINT EVALUATION AND RESULTS

Stencil Technology Experiment

In the evaluation of solder printing into the cavity, five different stencils were used from four different suppliers. Three different stencil technologies were used (electroformed, machined, and welded). The stencils are listed in Table 3.

Table 3. Print study

DOE leg	Stencil Supplier	Stencil technology
1	Supplier 1	4 mil E-formed
2	Supplier 2	4 mil E-formed
3	Supplier 3	4 mil machined
4	Supplier 3	4 mil machined with 3.5mil at the cavity
5	Supplier 4	4 mil welded

Each experiment leg consisted of nine cavity boards, three from each PCB supplier. The boards were printed, and the printed solder paste volume deposited was measured with Solder Paste Inspection (SPI) equipment. The goal of this study was to determine the effect of the stencil on the print volume and quality. The print volume coefficient of variation (CV) was used for comparison and assessment of each leg category. The solder print CV% is defined as the standard deviation of the paste volume divided by the average paste volume. The goal for good printing process is CV of less than 15%.

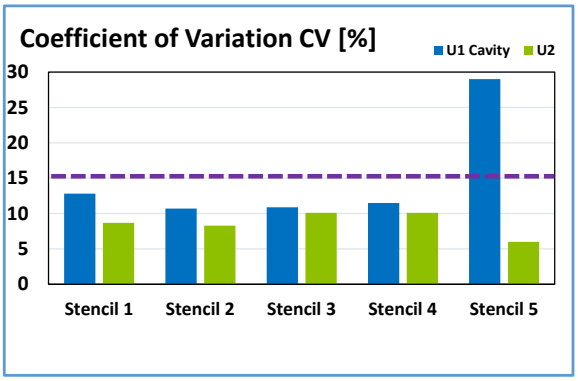


Figure 18. Stencil technology print CV study

Figure 18 presents the results of CV% from each stencil category. It shows both BGA locations, in the cavity U1 and outside the cavity U2. As expected, the BGA outside the cavity showed better CV% than in the cavity, however, four stencils provided adequate print quality for HVM process meeting the 15% target. The welded stencil showed comparable solder volume mean to the electroform stencils, but with more paste variation. However, there were no wet paste defects with the welded stencil, and the paste volume variation was not random. It showed excessive paste at the BGA edges with some tall solder joints. This was probably the result of a geometry mismatch (the stencil cavity depth was on the short side while the boards had a deeper cavity) (see table 4). Another cause for the welded stencil excessive solder was the reduced KOZ for the spot-welding and the bumps near the welded spots. Figure 19 provides the paste volume distribution on the BGA in the cavity. It indicated that all the high solder volume areas were at the corners and along the short side of the component.

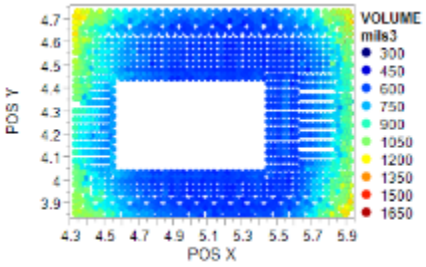


Figure 19. Paste volume distribution (welded stencil)

The stencil aperture in this study was a single size. In a case of a non-randomize pattern of paste, similar to the one seen on the welded stencil, optimization of the aperture size will be beneficial. By reducing the aperture size at the corners, the required volume of paste would be more evenly distributed.

The print CV % data was analyzed in Figure 20 by PCB supplier, and it indicated the impact of the cavity shape and cavity size tolerance on the print. PCB supplier C had consistently higher CV than others due to smaller XY dimension of the cavity. Printing at the edges was harder for both electroformed stencils (stencil 1 and 2).

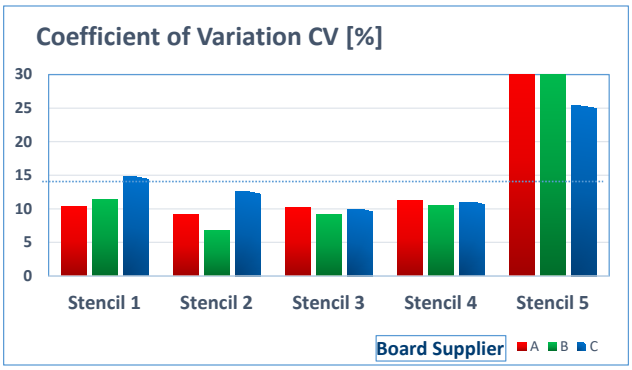


Figure 20. Board Supplier impact on print

The electroformed stencil had tapered walls which required appropriate clearance. The machined stencil had straight outside walls and provided better CV% for supplier C. Table 4 contains X&Y measurements data from all the stencils outside packet and the board inside packet. The cavity depth for the boards in Table 4 was measured by cross section near the cavity wall. As mentioned, stencil 5, the welded stencil, had depth mismatch in the cavity which is shown in Table 4. This resulted in high CV value on all board suppliers (see Figure 20).

Table 4. Dimensional analysis board/stencil

Board/Stencil	X [mm]	Y [mm]	Depth [µm]
Target	48	30	187
Supplier A	47.34	29.3	272
Supplier B	47.3	29.3	215
Supplier C	46.92	28.91	232
Stencil 1	47.3	29.3	212.6
Stencil 2	47.6	29.7	178.2
Stencil 3	47.3	29.3	207
Stencil 4	47.3	29.3	232.8
Stencil 5	46.8	28.9	148.3

In summary, this experiment showed that there is an impact to the stencil and board tolerance in addition to the shape which is difficult to quantify due to the shape complexity of the board and the stencil. The mismatch was tolerated by the process, and 4 out of the 5 stencils were meeting the CV% target.

Keep out zone (KOZ) Study

The test vehicle used in the study had a fixed KOZ from the BGA aperture to the cavity inner wall (Ci). It was 3 mm, and it was designed based on the need to have sufficient space to apply corner glue or underfill. See Figure 21 for Ci.

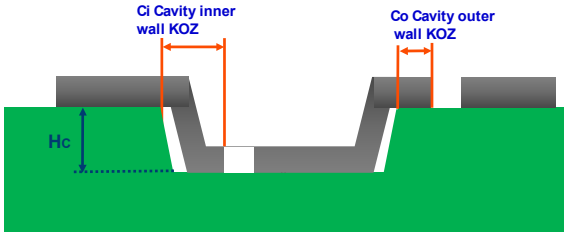


Figure 21. Cavity KOZ

In order to find how close a cavity could be from the printed aperture (in cases were no underfill or corner glue are needed), a black anodized aluminum fixture was fabricated with 200 µm cavity depth. A 3D stencil was fabricated to apply solder at 0.5 mm pitch. The spacing at the cavity level, Ci from the cavity wall to the first row of pads, started at 0.75 mm. The spacing from the cavity wall on the surface layer Co was evaluated by pads array of 6 x 6 with a distance of 100,200,250,300 µm from the edge. Figure 21 illustrates the KOZ on the fixture, Co and Ci.

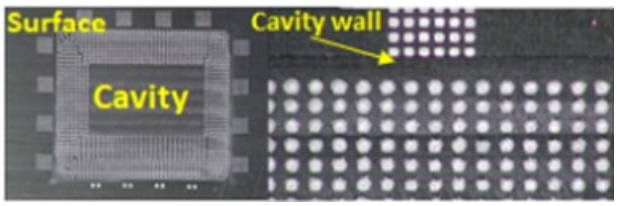
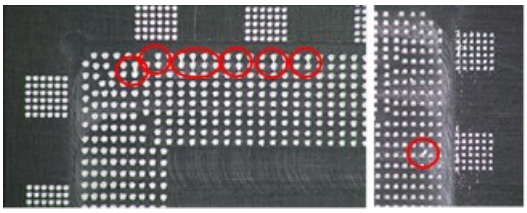


Figure 22. Print on cavity fixture

The KOZ experiment consisted of eight runs of four aluminum fixtures. The fixtures were printed, and paste was applied to the BGA in the cavity and to the surrounding 6 x 6 arrays on the surface level with different distances from the cavity walls. The solder volume was inspected by SPI machines, and the print was evaluated for wet bridging. The picture in Figure 22 shows a printed coupon and a close up view of the cavity wall. The results from this experiment indicated that the cavity level experienced excessive solder as the pads are closer to the cavity walls Some locations had wet bridging. All wet bridging occurred on the first 4 rows away from the wall which translates to ~ 2 mm (Figure 23a).



(a) (b)

Figure 23. Wet Bridging

On the surface level the print was good on all the 6 x 6 pads array but started to smear on the first row after multiple print cycles due to improper under cleaning of the stencil near the cavity wall (dead area from the cleaner) as shown in Figure 23b.

To define the minimum cavity KOZ at the cavity it is recommended to multiply the cavity depth (Hc) by 2 to take into account the 45 deg cavity wall, cavity tolerance stencil thickness and positional errors. Finally, adding 0.3 mm (0.15 mm for clearance necessary between the blade slit and the cavity wall and another 0.15 mm between the cavity and the stencil wall). Depending on the conservativeness of the design, it is recommended to add 2 mm for HVM material and process variation. For example multiple PCB or stencil suppliers, different printer set up and parameters or different operating shifts. See Figure 24 for the formula.

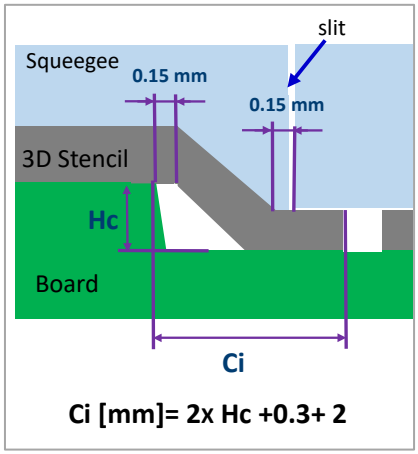


Figure 24. Cavity KOZ

This formula is based on experiments with 200µm cavity depth and can be used as a good starting point for cavity design. It may need additional experiments and adjustments for deeper cavities. For the KOZ outside the cavity (Co), as mentioned in the experiment results, the smearing was the only issue. To minimize the smearing, a KOZ of 0.5 mm and additional 0.5 mm for HVM variation would be recommended. Note that if a welded technology is used for the stencil, a welding KOZ is also necessary which will add 1.5mm.

Squeegee Experiment

The impact of the squeegee slit length (Figure 15), blade thickness, as well as the use of a soft polyurethane squeegee were evaluated. Nine boards, three from each PCB supplier, were printed with paste. The paste volume was measured in the SPI machine. Electroformed stencil 2 was used with this study. Five different squeegee types were evaluated. Table 5 lists the experiment's legs.

Table 5. Print Study

Leg	Squeegee Slit Length	Squeegee Thickness
1	10 mm	0.2 mm
2	5 mm	0.2 mm
3	15 mm	0.2 mm
4	10 mm	0.25 mm
5	Polyurethane	70 durometer

The chart in Figure 25 provides the experiment results of the different squeegees. Leg 1 – 10 mm slit and 0.2 mm thick blade showed the best print volume CV.

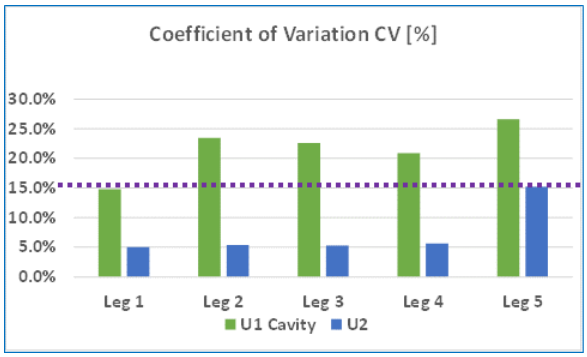


Figure 25. Squeegee Type Print CV Study

Using Polyurethane squeegee with no slit (leg 5) showed high solder print CV for the BGA outside of the cavity as well as the one inside the cavity. The chart in Figure 26 consists of the different squeegee blade legs and solder volume measured at U1 inside the cavity and U2 on the surface outside the cavity. The solder paste volume at leg 5, the polyurethane squeegee, had some low paste points and had difficulty in printing the two levels at the same time without causing solder scooping and insufficient solder volume.

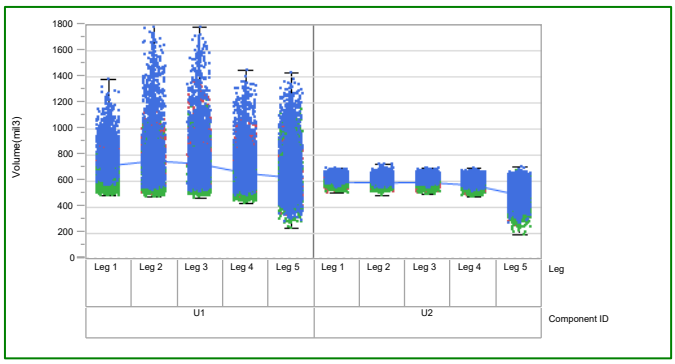


Figure 26. Squeegee type print CV study

COMPONENT ASSEMBLY IN THE CAVITY

The assembly yield of a BGA SiP into a cavity was compared to a control BGA SiP outside the cavity which was placed just 6 mm away from each other, as shown in Figure 27. BGA U1 was placed in the cavity while BGA U2 was outside of the cavity.

Figure 27. Assembled board

The data was collected from multiple builds with stencil 2 using slit squeegee blade 0.2 mm thick and 10 mm slit. After assembly, the boards were examined by X-ray for opens and shorts. Selected units went through failure analysis for cross sections. To add HVM variability multiple board supplier were used. The results are summarized in Table 6.

Table 6. SMT Assembly Yield

Board Supplier	Quantity	Yield	
		U1 Cavity	U2
A	48	37.5%	100%
B	23	100%	100%
C	58	100%	100%

FAILURE ANALYSIS

There were two surprises: the first one was that all defects came from one PCB supplier regardless of build time and shift although the same process was used at SMT to mount all boards. The second surprise was that the defects were open due to head on pillow (HoP) with a signature indicating excessive warpage. The SiP BGA that was selected had a stiffener to control its warpage during reflow to a minimum. The initial risk for defect was presumed to be bridging due to the excessive paste and large paste volume variation at the edges and corner of the cavity lands. Figure 28 shows stretched joints at the package corners with classic HoP defects, which has been shown in many industry papers [3] as an indication of high warpage of the package. However, this was not the case in this experiment.

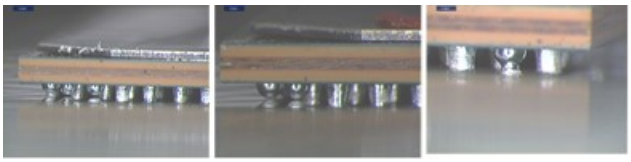


Figure 28. BGA Head on Pillow Defect

This defect, shown in Figure 28, is a result of localized warpage of the board in the cavity area, and not the BGA package. It was known that local warpage is a contributor to open HoP defects in SMT [4,5] but it has not previously been shown as being the only cause for this defect.

Cross Section

Figure 29 is a picture of a cross section of a board from supplier A showing the two corners (side left and right) of the SiP BGAs that are mounted next to each other. U1, that was in the cavity, is showing the warpage and stretched solder joints. On the other hand, U2, the BGA on the surface outside the cavity, is mounted on the same board, just 6 mm away from U1 which is flat with normal solder joints.

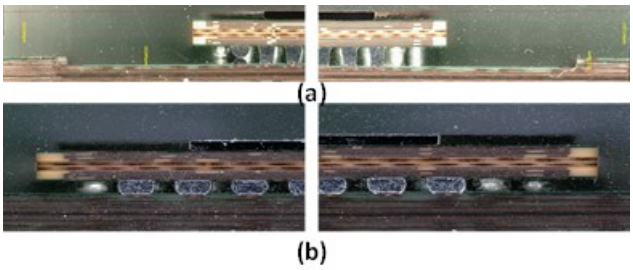
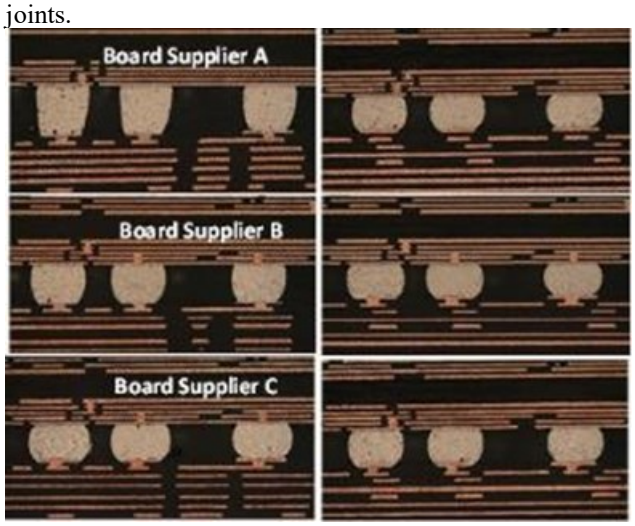


Figure 29. (a) Cross section U1 corners in the Cavity; (b) Cross section U2 corners on Board Surface

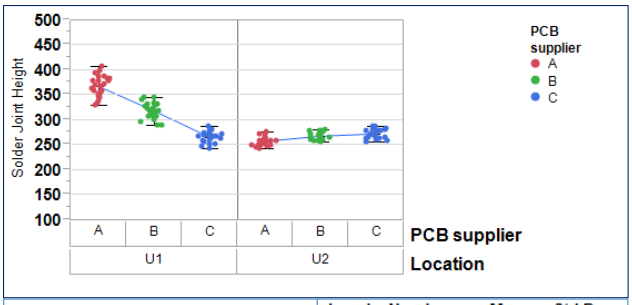
Furthermore, failure analysis points out that each one of the three board suppliers impact the BGA solder joints in a unique way. However, only supplier A caused SMT failures. The cross section in figure 30 of passing boards indicates that the joints' shapes of the packages that are on the PCB surface, (not in the cavity), Figure 30(b) are very similar between the three different board suppliers. They all have a normal joint shape and collapse. The BGA joints inside the cavity figure 30(a), however, had a unique shape for each PCB supplier. Supplier A showed stretched joints. Supplier B had normal to slight stretched joints, and supplier C had normal to slight compress joints.



(a) Cavity level U1 **(b) Surface level U2**

Figure 30. Comparison of BGA Solder Joints' Cross Section

The plot in Figure 31 consists of measurements of the BGA joints' height in the cavity from the three board suppliers. Comparison of the data indicates that the solder joint height of supplier A was 38.1% higher than supplier C.



Level		Number	Mean	Std Dev
A	U1 cavity	24	368.917	20.6480
B		24	319.750	15.7377
C		24	267.083	10.3961

Level		Number	Mean	Std Dev
A	U2	24	259.333	8.56518
B		24	269.625	7.56314
C		24	274.250	9.22779

Figure 31. Solder joints height

BOARD LOCAL WARPAGE

The dynamic warpage characteristic of the boards during the reflow cycle was assessed using Shadow Moiré metrology. The topography map of the warpage value across the cavity was measured. Figure 32 indicates the localized board warpage and shape at the cavity area. The dynamic warpage profiles in the cavity area show notable differences between the boards obtained from different suppliers. Supplier A had the highest warpage with convex shape at room and reflow temperature, explaining the defects seen during assembly. Board supplier B was fairly flat during room and reflow temperature and board supplier C had concave shapes which shows some compressed joints at the corner, but no failures occurred.

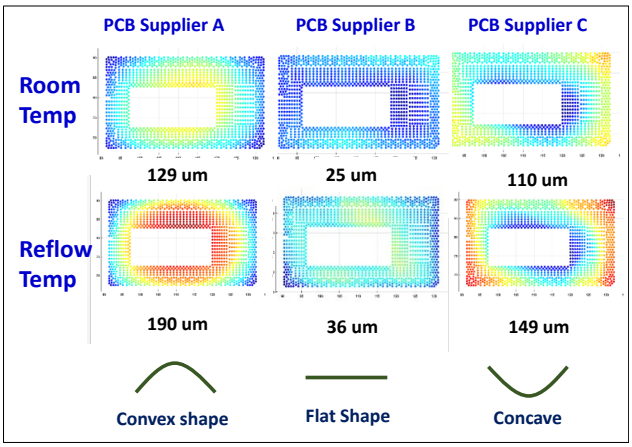


Figure 32. Warpage Shape and Magnitude for Boards from Three Different Suppliers

PACKAGE Z-HEIGHT

The package Z-height is a critical parameter for the product. The total package Z-height is defined as the height between the tallest points on the package to the top surface of the board. Figure 33 shows the total Z-height of the two packages: the one on the board surface and the one in the cavity after assembly. In both cases, the height is measured from the board surface to the top of the silicon die.

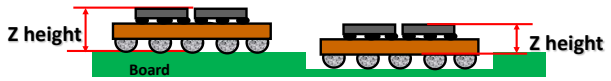


Figure 33. Package Z-height

The total Z-height was measured by an Optical Coordinate Measurement Microscopy (OCMM). Measurement data points were taken from three points on each die as a reference to a nearby point on the top surface of the board. Figure 34 illustrates the measurement points on the triple die package.

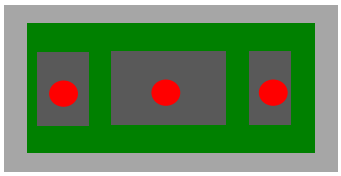


Figure 34. Package Z-height

The Z-height data comparison between U1, the package in the cavity, to U2, the package on the board surface, is shown in Figure 35. The Z-height of U1 is trending down as a function of the board supplier, following the solder joint height in the cavity.

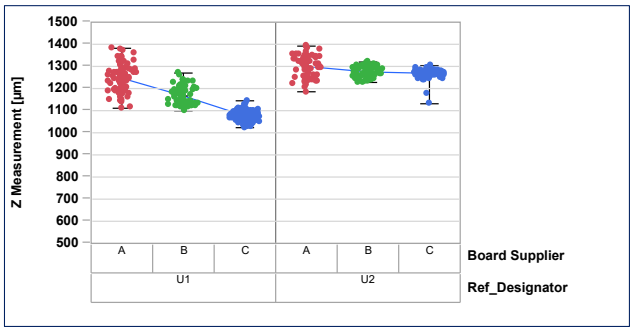


Figure 35. Package Z-Height

In summary, the mean Z-height of all packages on the PCB surface (outside the cavity) were higher than those in the cavity. Board supplier C had the largest mean Z-height reduction of 15%, while boards from supplier B had 8.5%. Board supplier A had the least reduction in mean Z-height of 4 %. Supplier A also had the greatest Z-height variation (Figure 35). In fact, because of the large variation of height on supplier A's PCBs, the assembled height of some components in the cavity was the same as the component on the surface.

CONCLUSION

This paper describes the details of a study of assembling SiP BGA packages into a cavity. It points out the challenges involved in the board cavity design and assembly of components in a cavity.

The paper discussed the board design challenge of having a cavity and defining the proper depth of the cavity to accommodate the board fabricator, the product design, and the SMT assembly.

The paper reviewed 3D stencil technologies to allow solder print on two levels. It analyzed the pros and cons for each technology and compared their performance. There is no one selected technology which will fit all needs. The 3D stencil needs to be well designed and selected for the unique application and use.

The section of print evaluation of the cavity board provided print results comparing a BGA in the cavity to an identical one on the surface of the board. The paper discussed the KOZ required for successful process and looked at different stencils, squeegees, and PCB suppliers.

In summary the print process of cavity shows that paste volume CV in the cavity is on the high side compared to a BGA on the PCB surface. The complexity of shapes and tolerances between the stencil cavity and the board cavity are a challenge to measure and analyze, and they will have an impact on the print results which will require apertures' optimization in some cases.

PCB supplier plays a large role in SMT yield. It impacts the print CV and the SMT yield. The warpage signature could be problematic in reflow. Some work still needs to be conducted to understand the critical parameters impacting the shape of the cavity in reflow.

The paper demonstrated a successful process for board assembly with 187 um depth cavity. It provided design and process solutions in addition to recommendations to overcome the challenges and have a robust successful solution to anyone desiring to use cavity in the board.

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