ANAYLYSIS OF MECHANISM ABOUT DATA RETENTION CHARACTERISTIC IN TANOS STRUCTURE

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ABSTRACT

Recently, as the data usage increases, the memory usage for storing the data also increases. A lot of researches have been done to reduce the production cost of the solid state drive (SSD) using NAND structure, which is widely used as a storage device along with the hard disk drive (HDD). One of them is to change the NAND structure from 2-D to 3-D by using the charge trap flash (CTF) technology, which is using nitride material (i.e., TANOS) in the floating gate instead of the conventional poly-silicon (i.e., SONOS). As the structure and material are changed, the characteristics of the device are also changed. One of the important functions of memory is the ability to preserve the data. Thus, in this paper the long-term evaluation of TANOS structure is investigated and the prediction of retention characteristic can be evaluated through the accelerated tests. We analyzed the behavior characteristics through experiments and Technology Computer Aided Design (TCAD) simulation to improve the accuracy of long-term data retention in TANOS (Tantalum-Alumina-Nitride-Oxide-Silicon) which is one of 3-D NAND. We also examined the effects of time and temperature about data retention by dividing them into four mechanisms: Schottky emission, Fowler-Nordheim (FN) tunneling, Poole-Frenkel (PF) emission, and trap-assisted tunneling.

Key words: NAND, TANOS, CTF, Data Retention, Reliability, Compact modeling, TCAD Simulation.

INTRODUCTION

The performance of recent CPU processes has improved and the amount of data that can be processed has increased, which is called the big data era. As the data usage increases, the amount of memory used to store it is also increasing. Currently, most popular memories are SSD made using NAND and HDD using magnetic force. SSDs are increasing its share of memory markets with its strength in fast speed. However, there is a limit to replacing hard disks due to the disadvantage of high cost. So there's a continuing study going on to develop high capacity and reduce the production cost to solve this. In the past, research continued to reduce the line width of cell in the NAND, and after that, we started changing the NAND from 2-D to the 3-D structure [1, 2]. In this way, the Nitride-based charge trap flash (CTF) technology instead of poly-Si, is applied to the floating gate material that saves data as well as shape while changing 3-D NAND [1, 3].

In this paper, I would like to study the data retention characteristics of TANOS-based NAND, which is one of the CTF technologies. In order to make more accurate prediction of the data retention, we analyzed the mechanism of the data retention through experiments and simulations. As a result, we want to check the data retention behavior more accurately and quickly by the proposed compact modeling.

BACKGROUND

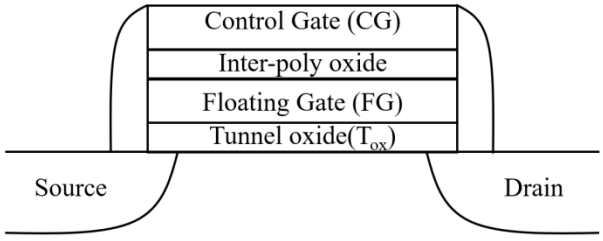

Figure 1. Schematic cell configuration of NAND flash memory [4]

FIG. 1 is a diagram schematically illustrating a cell of a general NAND flash memory. It is the structure that has the second gate in the conventional transistor structure. The operating principle of NAND flash memory is based on FN tunneling [4]. When a strong voltage is applied to the control gate, FN tunneling causes electrons can penetrate the tunnel oxide and move to the floating gate from channel. FIG. 2 is the schematic energy band diagram of FN tunneling [5, 6]. This leads to a rise in the threshold voltage (V_{th}), which is called the write operation. On the contrary, when voltage is applied to the channel side, electrons move in the opposite direction and resulting in V_{th} reduction, which is called the erase operation. During the operation, the response is divided

into 1 or 0 and stored using the difference in V_{th} caused by the principle.

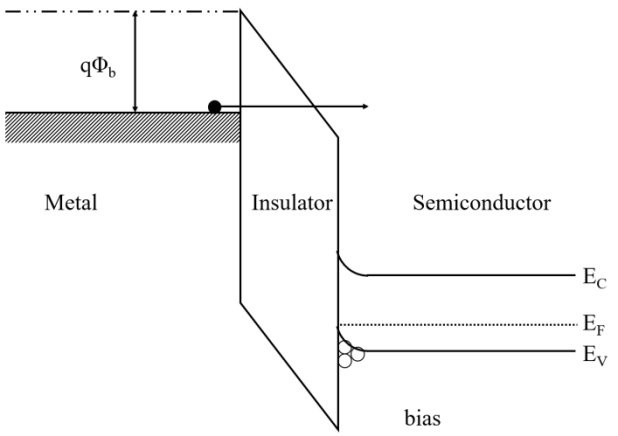

Figure 2. Schematic energy band diagram of FN tunneling [5]

As mentioned earlier, the poly-Si was used as the floating gate material for storing data in the 2-D structure. However, it is difficult to separate between cells and cells in the 3-D structure. Therefore, the charge trap flash (CTF) technology was developed using Nitride, which is used as an insulator instead of Poly-Si. As shown in FIG. 3, one of CTF technology is TANOS, which is stacked in order of Tantalum-Alumina-Nitride-Oxide-Silicon, so it is called TANOS after the initial letters [3, 7].

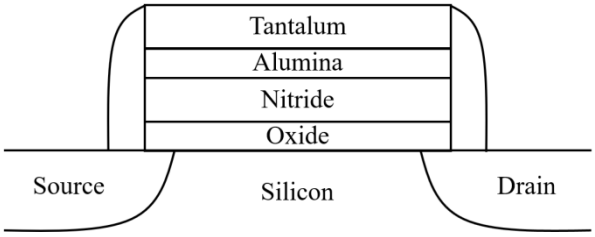

Figure 3. Schematics of TANOS Structure [4]

In this way, not only the structure but also the characteristics of the device changed significantly due to the change of materials. There are three items to evaluate the cell reliability of NAND Flash memory: endurance, read disturbance, and data retention. The endurance evaluates the number of write and erase operation capability and the read disturbance evaluates the number of possible read times. The data retention evaluates the data storage capability. Among these, since the data retention evaluation requires the long-term evaluation, the accelerated evaluation is required to estimate the characteristic within the proper time period [4, 8].

In general, when the acceleration constant of temperature is calculated using the Arrhenius equation as follows [8]:

$$k_{acc} = A\exp\left(\frac{-E_a}{RT}\right) \quad \text{--- (Eq. 1)}$$

However, as the cell size of the device became smaller, it became difficult to explain all the phenomena with only this equation alone. In this paper, we investigate the effects of the temperature and time by classifying phenomena by the conduction mechanisms.

MECHANISM THEORY

In the case of TANOS, the device is built with the insulating film. Thus, I analyzed how the conduction mechanism in the insulating film affects it. There are the four main mechanisms, such as, Schottky emission, FN tunneling, Pool-Frenkel emission, and trap-assisted tunneling which affect the characteristics of NAND devices when reviewed through the previous research papers [6, 9, 10].

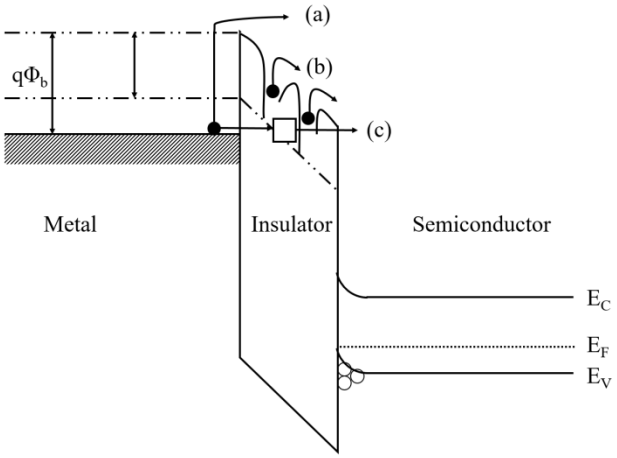

Figure 4. Schematic energy band diagram in metal-insulator-semiconductor conduction: (a) Schottky emission, (b) Poole-Frenkel emission, and (c) Trap-assisted tunneling [5, 6]

FIG 4. (a) shows the schematic energy band diagram of Schottky emission. Schottky emission is conduction mechanism when electrons can get enough energy provided by thermal activation, the electrons in the metal can move to the dielectric by overcoming the energy barrier at the metal dielectric interface [5, 6, 9]. The equation of Schottky emission is as follows:

$$J = A^*T^2\exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}}{kT}\right] \quad \text{--- (Eq. 2)}$$

$$A^* = \frac{4\pi qk^2m^*}{h^3} = \frac{120m^*}{m_0} \quad \text{--- (Eq. 3)}$$

where J is the current density, A^* is the effective Richardson constant, m_0 is the free electron mass, m^* is the effective electron mass in dielectric, T is the absolute temperature, q is the electronic charge, $q\phi_B$ is the Schottky barrier height, E is the electric field across the dielectric, k is the Boltzmann's constant, h is the Planck's constant, ε_0 is the permittivity in vacuum, and ε_r is the optical dielectric constant [5, 6].

Fowler-Nordheim (FN) tunneling was schematically represented in FIG. 2. FN tunneling is a kind of direct tunneling but FN tunneling requires high electric field. High electric field results in thinning of the barrier and it is associated with transversal of triangular barrier. It makes penetrate through triangular barrier [4, 5, 6, 9]. The equation of the FN tunneling current is as follows:

$$J = \frac{q^3 E^2}{8\pi h q \phi_B} \exp\left[\frac{-8\pi(2qm_T^*)^{1/2}}{3hE}\phi_B^{3/2}\right] \quad \text{--- (Eq. 4)}$$

where m_{T^*} is the tunneling effective mass in dielectric; the other notations are the same as defined before.

FIG. 4 (b) shows the schematic energy band diagram of Poole-Frenkel (PF) emission. PF emission is the thermal excitation of electrons may emit from traps into the conduction band of dielectric. Considering an electron in a trapping center, the Coulomb potential energy of the electron can be reduced by an applied electric field across the dielectric film. Reduction of potential energy can increase the probability that electron will excite from trap to the conduction band of the dielectric [5, 6, 10]. The equation of PF emission is as follows:

$$J = q\mu N_C \exp\left[\frac{-q(\phi_T - \sqrt{qE/\pi\varepsilon_i\varepsilon_0})}{kT}\right] \quad \text{--- (Eq. 5)}$$

where μ is the electronic drift mobility, N_C is the density of states in the conduction band, $q\phi_T$ is the trap energy level, and the other notations are the same as defined before.

FIG. 4 (c) shows the schematic energy band diagram of the trap-assisted tunneling (TAT). TAT is the most famous tunneling mechanism since it does not require specific conditions. If traps are located in an insulator or the interfaces, then TAT can be occurred through the trap sites even low electric field region [5, 6, 10]. The equation of TAT is as follows:

$$J = \frac{C_t q N_t p_2}{A}\left[Ax_1 - \ln\left(\frac{1+p_2\exp(Ax_1)}{1+p_2}\right)\right] \quad \text{--- (Eq. 6)}$$

$$p_2 = \exp\left(-\frac{4(2qm_{ox})^{1/2}}{3\hbar E}\phi_t^{3/2}\right) \quad \text{--- (Eq. 7)}$$

$$C_t = \left(\frac{m_{nitride}}{m_{ox}}\right)^{5/2}\left[\frac{8E_1^{3/2}}{3\hbar(\phi_t - E_1)^{1/2}}\right] \quad \text{--- (Eq. 8)}$$

$$A = \frac{2(2qm_{ox})^{1/2}}{\hbar}\phi_t^{1/2} \quad \text{--- (Eq. 9)}$$

$$x_1 = \frac{(V_{appl} - \phi_t)}{E} \quad \text{--- (Eq. 10)}$$

where ϕ_t the trap depth, E is the electric field, m_{poly} and m_{ox} are the effective electron mass, E_1 is the energy of traps and V_{appl} is applied voltage.

METHODS OF EXPERIMENTS & SIMULATIONS

Experiments and simulations were conducted to examine how the above four mechanisms affect the data retention temperature and time. In the experiment, a total of 12 chips were tested with 4 chips for each bake temperature of 25 ºC, 55 ºC and 85 ºC. The device was initially written and erased 100 times and assumed a certain state of the device use condition. After the write and erase cycling, the initial fail bit of the programmed cell was measured at a temperature of 25 ºC. Later, each chip was baked at 25 ºC, 55 ºC and 85 ºC, and the fail bit was measured at the regular interval.

FIG. 5 represents the V_{th} distribution and counting fail bits. This was converted into the metric of V_{th} variation and used as the data for the data retention behavior.

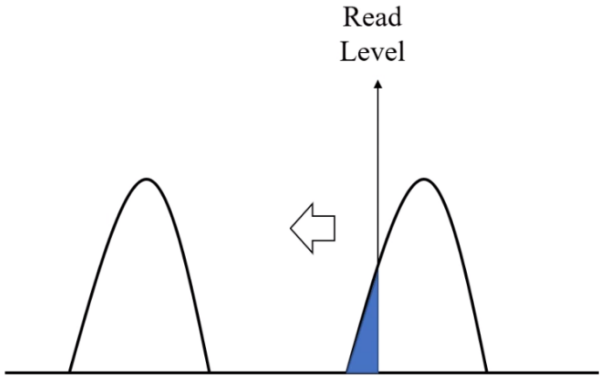

Figure 5. Schematic of V_{th} distribution and counting fail bits [4]

In the case of this fail bit, the amount of change was determined by the relative value obtained by dividing the fail bit by the initial state in order to calibrate the deviation for each sample according to the initial state. At this time, it was assumed that the fail bit is caused by only V_{th} loss.

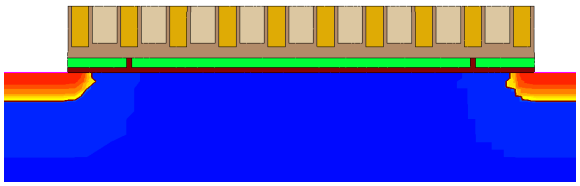

Figure 6. Schematic cell structure for simulation

In order to analyze this mechanism, a simulation was performed using the commercial TCAD Tool [10]. As shown in FIG. 6, the cell was made up of 9 cells, and the distance between the gate and spacer was set to 20 nm. The tunnel oxide was 4 nm thick, the floating gate nitride was 8 nm, and the inter-poly oxide was 12 nm thick.

FIG.7 shows the energy band diagram of the simulated TANOS structure. For the device simulation, the program voltage of 20 V and the erase voltage of -20 V were applied in the same manner as the experimental conditions, and after repeating 5 times, the written state was set to the initial state. As in the experiment, we investigated how trapped electrons move with the time according to the temperature.

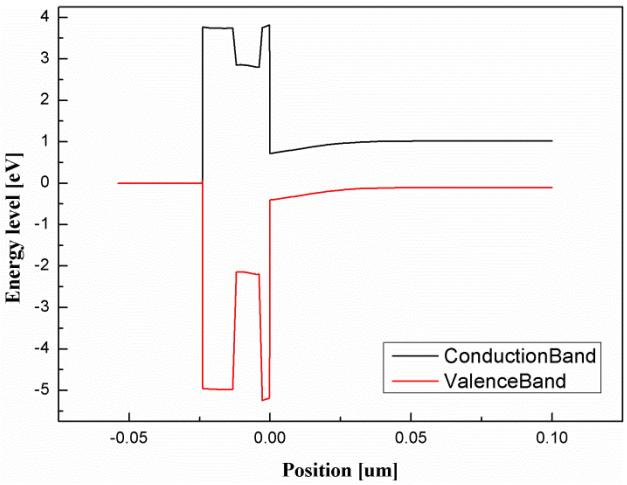

Figure 7. Energy band diagram of the simulated TANOS structure (vertical direction)

RESULTS AND DISCUSSION

As a result of the experiment, it can be confirmed that it has acceleration according to the temperature as follows. As the temperature increases, the increment of the fail bits also increases. By using eq. 1 which is the Arrhenius equation, obtained the acceleration coefficient for temperature, the activation energy (E_a) value obtained in this experiment can be calculated as 0.53 ~ 0.65 eV.

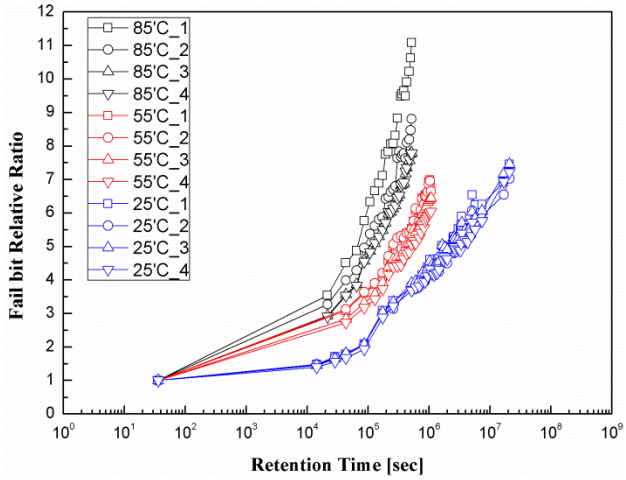

Figure 8. Fail bit trend of data retention experiment

In the TCAD simulation, after repeating write and erase operations of the device having the structure described above, the data retention results were observed for each temperature. FIG. 9 is the TCAD simulation results of the trapped charge profiles at 85 ºC, and you can see that only the floating gate at the bottom is trapped. Even if these trapped electrons are not applied with voltage, if they are left in a high temperature environment, it can be confirmed that the trapped electrons are increasingly spread as shown in FIG.9 (b).

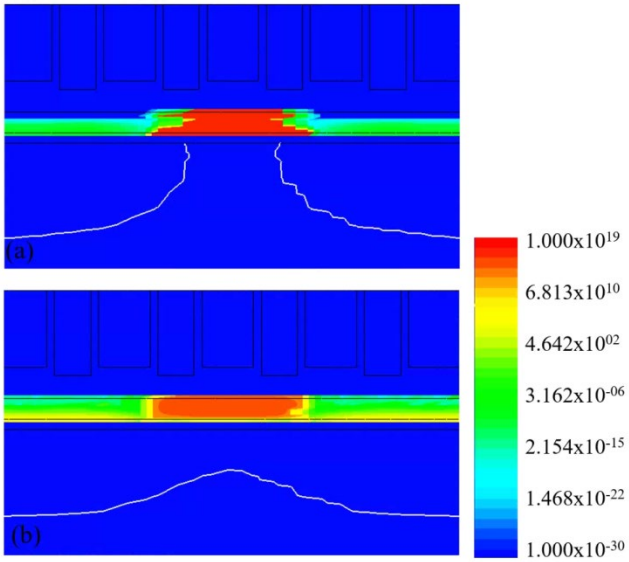

Figure 9. Variation of trapped charges by data retention simulation at 85 ºC: (a) initial, and (b) 10 year later

For more detailed observations, the distribution of the electron trapped charges was examined by cutline profile in the vertical direction. As shown in the FIG. 10, the left side is the upper control gate side and the right side is the lower

substrate side. The operation voltage is strongly increased at the time of writing. In the initial stage, the very large amount of the electron trapped charges in both the upper and lower parts of the floating gate can be seen, and the constant electron trapped charges at the maximum was observed. As the time passes, the tunnel oxide part at the bottom of the floating gate is relatively thinner than the inter-poly oxide at the top, so the charge trapped in this direction is lost and the amount of electron trapped charge decreases from the right.

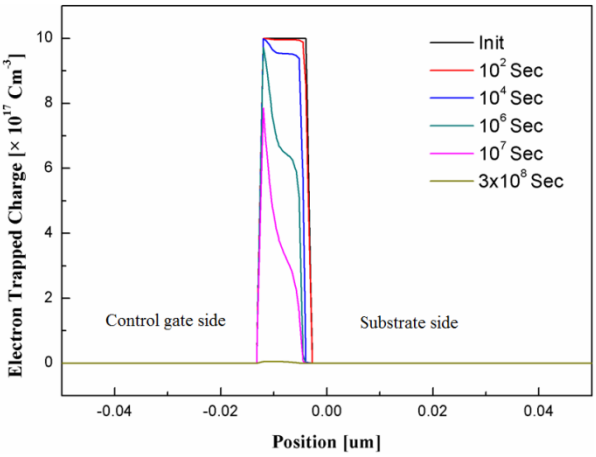

Figure 10. Electron trapped charge profile by the location over time (vertical cutline direction)

When the data retention simulation is executed, the amount of electron trap charge varies as shown in FIG. 11 [11]. The detrapping of charges in the floating gate proceeded rapidly as the temperature increased. Before this, when comparing the value of the fail bit of the experimental result converted into the trap charge amount, it was confirmed that they show in good agreement as shown in FIG. 12.

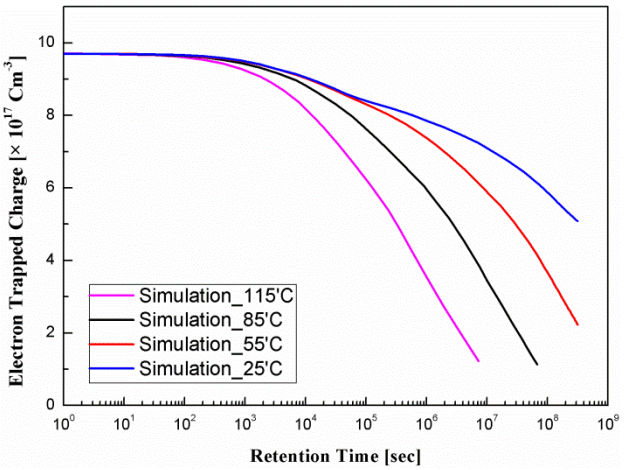

Figure 11. Results of electron trapped charges varying with different temperature over time

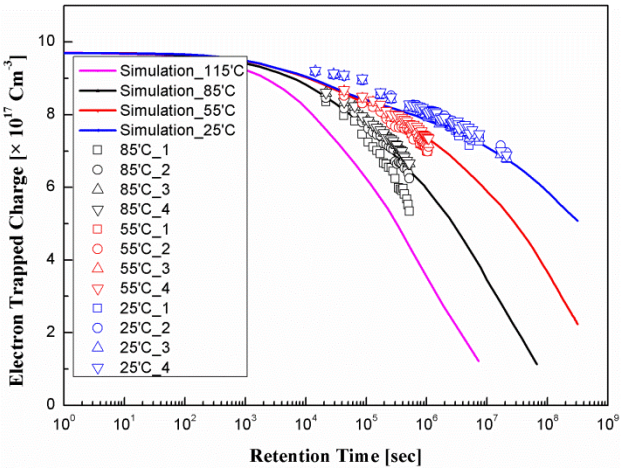

Figure 12. Comparison of experimental and simulated data by temperature over time

COMPACT MODELING

In the previous study, compact modeling was proposed to quickly calculate the data retention behavior. However, it was not possible at that time to explain what factors each term describes [11, 12, 13]. In this study, compact modeling was re-analyzed to improve compact modeling and to analyze it in connection with each mechanism. On the basis of the equations of Schottky emission, FN tunneling, PF emission, and trap-assisted tunneling based on the above-mentioned mechanism formulas Eq. 2 to Eq. 10. The proposed compact model for data retention is as follows:

$$y = A_0 + A_1 \times T^2 \times \exp\left(-x/t_1\right) + A_2 \times \exp\left(-x/t_2\right)$$
$$\text{xp}\left(-x/t_1\right) + A_2 \times \exp\left(-x/t_2\right) + A_3 \times \text{ex} \quad \text{---(Eq. 11)}$$

In the case of the TAT term, the exponential function is included inside the log function, and other than the exponential function. In the term of A_0, the starting point of the electron trapped charge and each term is based on the literature formula of each mechanism.

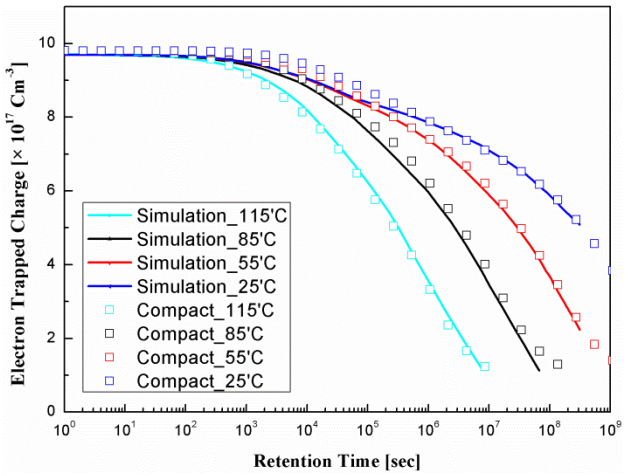

Figure 13. Comparison of simulation results and compact modeling results

A_1 and t_1 are the intensity and decay constants of Schottky emission, A_2 and t_2 are the intensity and decay constants of FN tunneling, A_3 and t_3 are the intensity and decay constants of Poole-Frenkel emission, and A_4 and $t4$ are the trap-assisted tunneling, respectively. Equation is composed of four terms with intensity and decay constant. Compact modeling was carried out as in eq. 11. Comparison between simulated and compact modeling results are shown in FIG. 13.

MECHANISM ANAYSIS

Compact model was carried out according to the simulation results, and each term of this equation was classified. In the case of the first term calculated by Schottky emission, A_1 is 6.95×10^{11} based on 85 ºC, and even though multiplying T value by 9.01×10^{16}, A_1 value is small and t_1 value is relatively large. As can be seen from FIG. 14, this indicates that the contribution to the whole is small but the influence on temperature is large. When E_a was obtained, it showed about 1.02 eV, and it was found that trapped electrons were rapidly removed at the early stage depending on the temperature, but the effect did not proceed continuously.

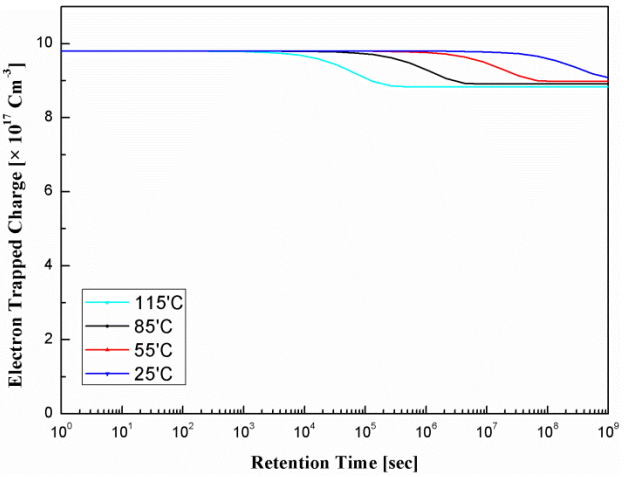

Figure 14. Compact modeling behavior of the first term by temperature

The A_2 and t_2 terms, which are assumed to be FN tunneling, showed negligible levels because they did not contribute significantly because of the data retention that does not apply bias due to the characteristics of FN tunneling, which are strongly influenced by the bias.

In the case of A_3 and t_3 terms assuming Poole-Frenkel emission, A_3 is 2.43×10^{17} at 85℃ and A_3 is bigger than A_1 as shown in FIG. 14. Based on the result, E_a was found to have a value of about 0.86 eV, and it was analyzed that the size of A_3 affected more than Schottky emission.

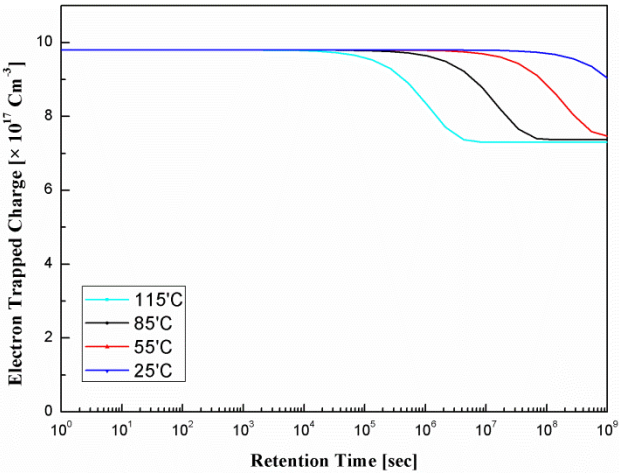

Figure 14. Compact modeling behavior of the third term by temperature

A_4 and t_4 terms in the case of TAT are shown in FIG. 15. In this case, A_4 is 4.67×10^{16}, which is smaller than the other terms and it was based on the logarithmic function. When the change of the initial value was analyzed to compare with

other mechanisms, the E_a value has 0.35 eV, which is similar to that based on other research cases [11].

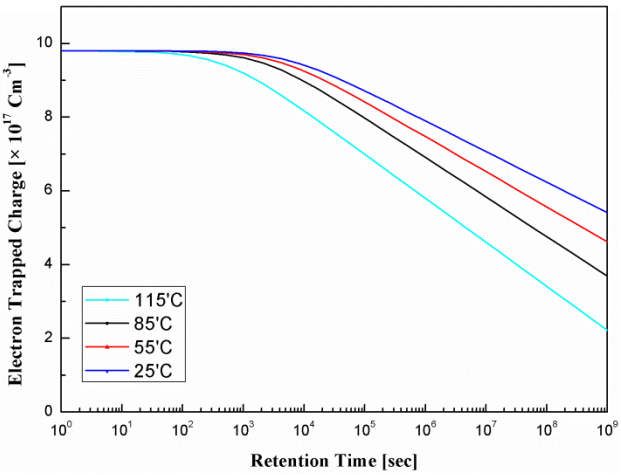

Figure 15. Compact modeling behavior of the 4th term by temperature

In order to confirm this, when we simulated the change of electron trapped charge for each mechanism, the result is shown in FIG. 16. It was confirmed that this result affects the absolute value of the amount of change in trapped charge in the order of TAT, PF emission, Schottky emission, and FN tunneling as in the compact modeling as a result value at 85 ºC.

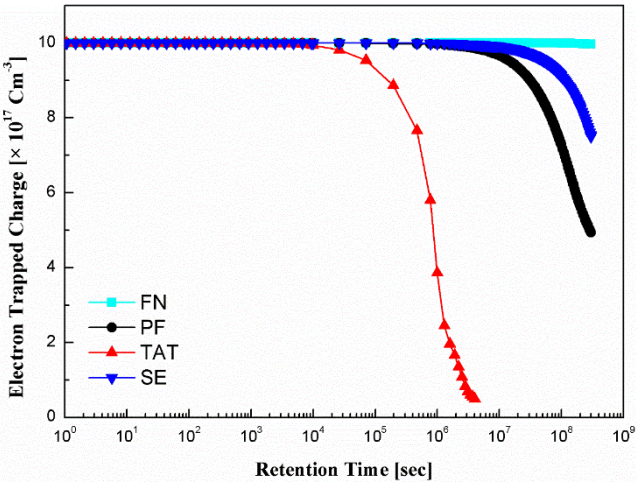

Figure 16. Simulation results by each mechanism

CONCLUSIONS

In this paper, as NAND Flash memory is changed from 2-D structure to 3-D structure to increase storage capacity, data retention characteristics change due to material change of the floating gate. We analyzed changes in retention characteristics and tried to accurately and quickly predict changes in long-term device reliability. For this purpose, the experiments for data retention were performed at three temperatures, and the results confirmed that there was an acceleration factor according to the temperature. When using the Arrhenius equation, which is used for the acceleration evaluation due to the temperature factor, it was confirmed that the activation energy is ranged from 0.53 to 0.65 eV.

In order to classify them by mechanism, we simulated them using TCAD and analyzed their behaviors by comparing them with actual experiments. First of all, the simulation confirmed that the results could represent the experimental results. Based on this, the compact modeling was applied to make it easier to apply the equations. In addition, this study classified the behavioral characteristics by mechanism. In the early stage after the program, the effect of Schottky emission was big, but it was confirmed that detrapping of electrons due to TAT had the biggest effect over time.

By analyzing precisely the mechanism influence on the data retention behavior with time and temperature, the accurate initial behavior of data retention was analyzed by increasing the accuracy of compact modeling. Through compact modeling, data was measured for the actual behavior of the device with only performing the relatively short initial test, and the result of the long-term reliability estimation can be calculated for a long time of more than 3 years, which is the actual life of the current electronic products.

FUTURE WORK

This study was conducted specific case of the data loss behavior which is caused by only charge loss at single level cell (SLC). Currently, in case of NAND Flash memory, Multi Level Cell (MLC) technology is widely used. In this case, the case of rising V_{th} should be considered in the same manner.

ACKNOWLEDGEMENTS

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