ADVANCED SUBSTRATE TECHNOLOGY FOR HETEROGENEOUS INTEGRATION

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ABSTRACT

The rapid development of semiconductor technology and multi-function demands of end products has driven IC foundry industry toward 7nm node process, and even next generation of 5nm.[1] The I/O pitch of chip is reduced accordingly but the interconnection of build-up of IC carrier is still large to fit the IC interconnects (Fig. 1). In order to overcome the gap of I/O pitch between IC chip and carrier, the interposer technology has been considered as a solution to resolve the issue.

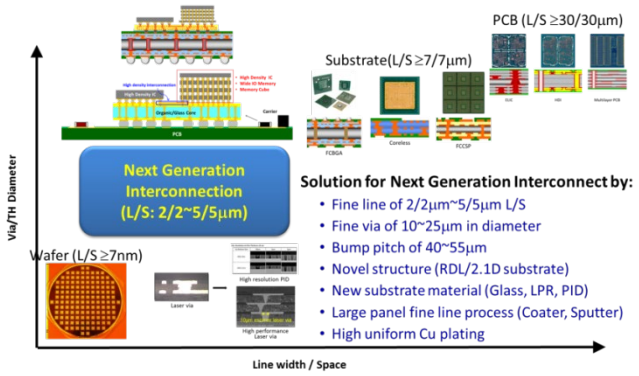

Fig. 1 Challenge and needs for next generation interconnect

Traditional semiconductor components include active chips, passive device, silicon interposer, organic substrate, and printed circuit board. How to package these components as a module is based on the product requirements. In recent decades, lots of assembly technologies and structure solutions for high density packaging (Fig. 2) have been evaluated, such as flip-chip assembly, Fan-out/Fan-in, InFo (Integrated Fan-out), CoWoS (Chip on Wafer on Substrate), SWIFT (Silicon Wafer Integrated Fan-out Technology), SLIM (Silicon-Less Integrated Module), EMIB (embedded multi-die interconnect bridge), 2.1D/2.3D/2.5D/3D IC packaging and so on. All of these package technology solutions were considered to the electrical routing interconnection. The scaling of interconnection including trace and via is always the trend for the semiconductor industry supply chain.

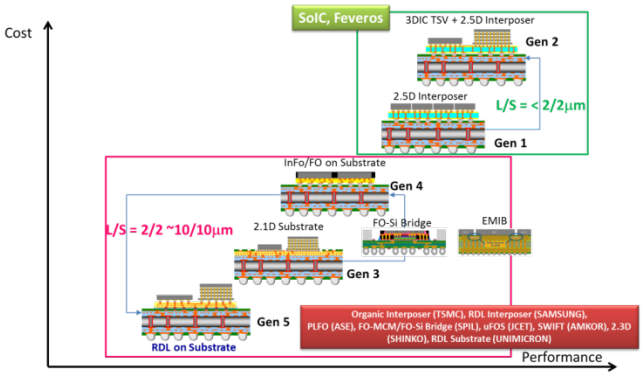

Fig. 2 High density interconnection trend

To achieve the dimension scaling in IC substrate and PCB industry, glass as the removable carrier played a very important role for the next generation interconnection. Benefits to apply glass as the carrier[2] or substrate core[3,4,5] such as low profile surface suitable for high density application and good size effect for large form factor compared with Si wafer had attracted many researchers' attentions to develop. Besides, good dimension stability of glass also shows lower warpage in the process and high control level in fine line/space and via formation through traditional IC carrier and PCB process. However, there are still many challenges need to be overcome.

INTRODUCTION

Heterogeneous Integrations are driven by Moore's Law. Advanced Packaging plays a critical role for semiconductor supply chain. Enable diverse AI models and Neural network applications drive performance requirements which lead to 7nm wafer capacity severely shortage.

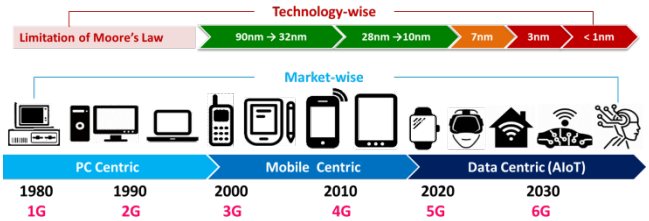

Fig. 3 Technology redefines industry

The trend of advanced heterogeneous integration substrate are :

- Substrate size becomes bigger than 100mm × 100mm
- More chips will be integrated on substrate
- More than 20 layers build-up layers
- Challenges: Long lead time, low yield & high cost

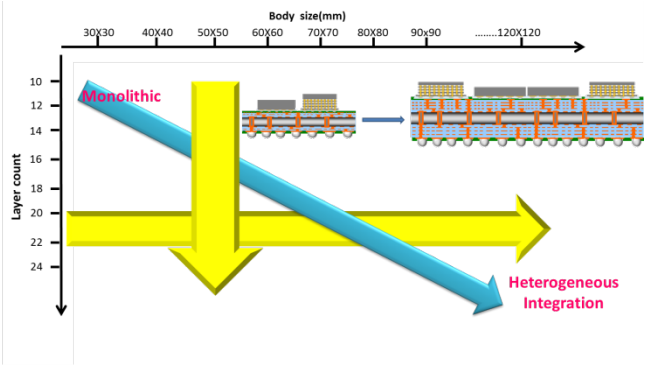

Fig. 4 Trend of advanced FCBGA Substrate

ADVANCED IC CARRIER TECHNOLOGY DEVELOPMENT TREND

Driver:

1. Heterogeneous integration: large body size (112x112mm) and high layer count (15/6/15), finer L/S with small via pad.
2. High power consumption: thick Cu (MLC), high PTH/laser via density, thermal bar design.
3. High speed transmission: low Df dielectric, smoothness Cu pretreatment, LtL alignment, tight Cu thickness and trace width tolerance.

Development direction:

1. Advance equipment for better alignment, fine L/S, uniformity, inspection.
2. Material: high stiffness core, low Dk/Df dielectric, anti-crack SR, chemicals.
3. Process module development for better uniformity (Cu thickness, trace width, dielectric thickness)
4. Process integration for warpage, reliability and L1/L2 package performance.

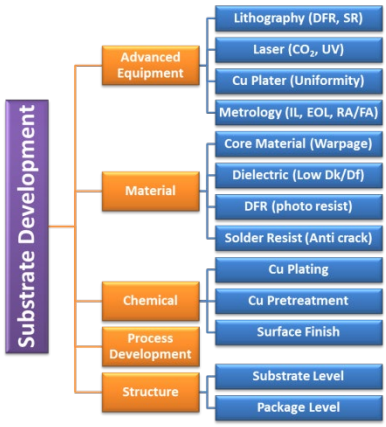

Fig. 5 IC Carrier Technology Development Trend

CONCLUSION

Market:

- 5G and AIoT are booming in next 5 years, US is in the leading position while China will be the strongest competitor in the markets.

Technology:

- Heterogeneous integration of high-end products existed from 2.5D planar interconnect (Si interposer, EMIB) to 3D die-to-die stacking (WoW, SoIC, Foveros).
- Substrate technology is driven by extreme body size/high layer counts, heat dissipation, low loss material…etc.

Investigating in long-term growth market and technology

- Intensive CapEx for advanced package: 2.5D, EMIB, 3DIC, Chiplet, RDL SBT.
- Fab-like substrate manufacturing will be coming soon.

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