ADVANCES IN PACKAGING FOR EMERGING TECHNOLOGIES

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ABSTRACT

A review about latest advances in packaging and drivers for the development of novel packaging technologies will be given in this paper. Starting with a description about the trends in miniaturization of IC packaging and the demand for heterogeneous integration in the following a focus on commonly applied processes like System-on-Chip, Flip-Chip packaging, Fan-out packaging and 3D-Integration will be presented. A brief explanation about process characteristics, followed by an explanation of the main process steps is described. The latest version of the heterogeneous integration roadmap is short introduced. The link to corresponding fields of application like high performance computing and AI processing, mobile electronics and 5G, and automotive is given. Here, main requirements for each technological sectors are worked out followed by a description of commonly applied package types. Each sector is round up by mentioning key challenges for future developments.

Key words: Advanced packaging, future technologies, automotive, 5G, AI.

1. INTRODUCTION

Semiconductor downscaling of transistor size is becoming more challenging as R&D seems approaching the limits of Moore's Law. This is due to physical challenges as industry is approaching ever-smaller technology nodes. The effort to further decreasing the transistor size is increasing massively which makes new product development for IC manufacturers very expensive. Therefore, two paths have been set in order to overcome this issue. The one of further downscaling transistor size despite of increasing costs is "More Moore". The focus lies on further integrating different kinds of functionality on a single chip, namely System-on-chip (SoC) integration. The second path is to integrate functionality by packaging multiple chips in an intelligent manner, e.g. by stacking them on top of each other or placing them next to each other on a separate substrate called System-in-Package (SiP) [1, 2].

In [3] two major approaches have been proposed, the transistor focus and the system focus. As stated, industry is shifting towards system focus due to better cost efficiency. More and more effort is put on further downscaling the package size and integrating much more functionality on a smaller footprint size [4]. This trend is further supported by increasing market needs for smaller packages powered by mega trends like 5G development, consumer electronics, IoT sensor development and Artificial Intelligence (AI) [5].

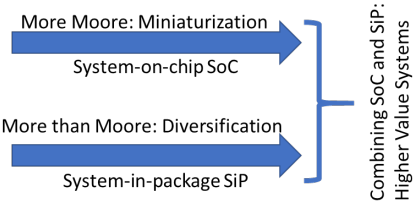

Figure 1: Combining „More Moore" and „More than Moore" approach [3]

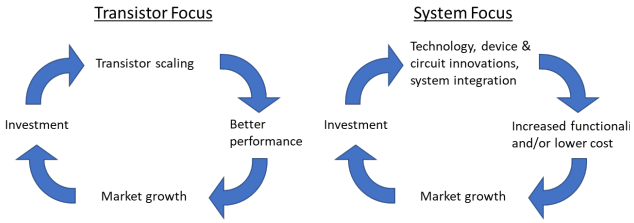

Figure 2: Comparison of "Transistor Focus" and "System Focus" approach [3]

When it comes to deciding which kind of package should be chosen, one has to assess the possibilities by looking at the main functions of a package according to its applications. Main functions are signal distribution, power distribution, heat dissipation and protection of the IC. Mechanical, chemical and electromagnetic behavior of the package is important to ensure sufficient reliability of the system [1].

Here we aim to give an overview about the most important packaging technologies for heterogeneous integration and to introduce their application in the fields of current key technological drivers. In the first section, the main processes are introduced. System-on-Chip, Flip-Chip Packaging, System-in-Package, Fan-Out Packaging and 3D Packaging is explained. In the following section, the application of the key packaging technologies for some of the current technology trends is introduced. Technological fields in focus are high performance computing and AI processing, smartphone integration and 5G communication and automotive electronics. The requirements and main challenges for each application is introduced. Afterwards, current packaging technologies are presented and an outlook about future development drivers is given. At the end of the paper, a summary about the key findings is given.

2 Process Technologies

In the following, several key packaging processes will be introduced. In [6] the landscape of different packaging technologies is grouped according to I/O count and footprint. For low IO count and low footprint Flip-Chip Chip-Scale-Packages (FC CSP) and Fan-Out Wafer-Level-Packages (FOWLP) are commonly applied, whereby FO technologies are providing an even smaller footprint compared to FC technologies. Both package types find their application in the mobile/wireless communication sector. For consumer electronics, FC CSP and FO WLP with higher I/O count and bigger footprint can be applied for increased performance. Furthermore, SiP designs find an application in this sector by combining several chips in one package. For computer/networking applications, 2.5D/3D build-ups are commonly used next to SiP with increased I/O count and increased footprint [6].

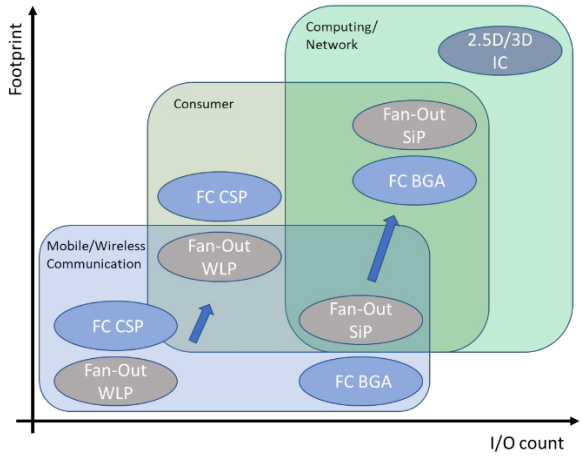

Figure 3: Packaging landscape for different fields of application sorted by I/O count and footprint [6]

System-on-Chip

One common approach to integrate functionality on chip level is the System-on-Chip architecture. Here, all kinds of modules, e.g. memory and logic, can be combined monolithically on a single chip. The main benefit by doing so is a very compact and lightweight system if computing, communication and several functional blocks can all be integrated on one chip [1, 7, 4].

On the other hand, disadvantageous are long design times due to complexity, fabrication and test costs, mixed-signal processing complexities, huge number of mask steps and dissimilar process technologies. One task of system designer is to find the optimum either by integrating functionality in a SoC approach or by integrating multiple chips via System in Packaging [4].

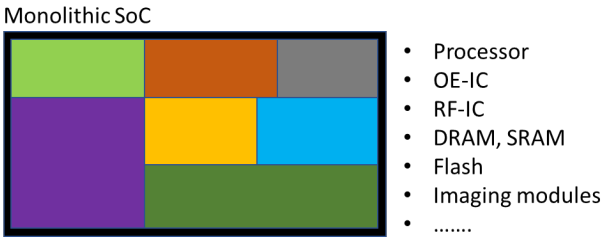

Figure 4: Schematic of monolithic System-on-Chip integration of various modules [4]

Flip-Chip Technology

Packages from the 80s, like lead frame based solutions, came over with the disadvantage of limited systems performance. Flip chip packaging was and is offering better form-factor performance. The main characteristic of a flip chip package is that the active area of the chip is facing the substrate or another chip. In Figure 5, a Flip-Chip package is shown. The balls are placed directly on the chip face side, which makes it necessary to "flip" the chip in order to assemble the chip to the substrate. After aligning chip and substrate, the bumps are reflowed to form a connection. The solder balls act as electrical and mechanical connection between chip and substrate. The advantageous of WLCSP over traditional packaging technologies are e.g. higher cost efficiency, smaller form factor, simpler structure and lighter systems [1, 7, 8].

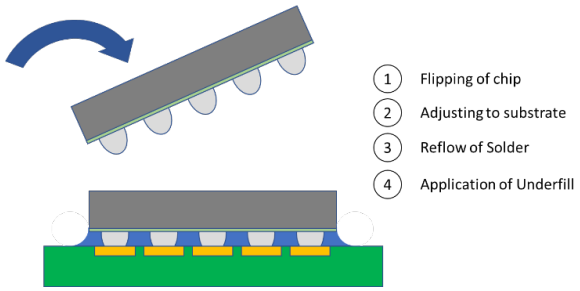

Figure 5: Flip-chip technology – process principal [7]

Commonly applied are C4 bumps, which stands for "controlled collapse chip connection". Wafer bumping is mostly done via electrochemical deposition or electroplating processes (see Figure 6). Therefore, a passivation is put on the Si-Die followed by sputtering a UBM metallization, coating and structuring of a photoresist. Then, Sn-bumps are electroplated, photoresist is stripped and the remaining UBM layer is etched away. In order to achieve the characteristic form of the bumps, the build-up is reflowed [7].

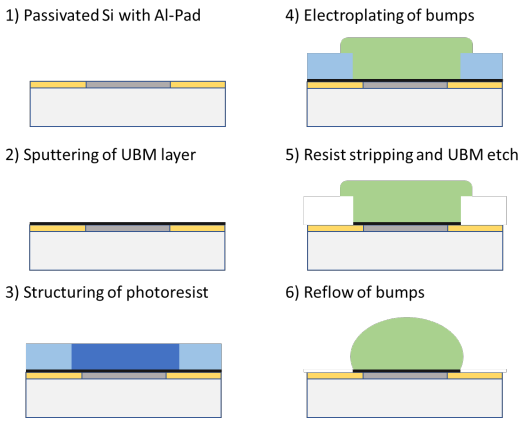

Figure 6: Wafer bumping via electroplating – process principal [7]

Development effort is put a lot into increasing the number of balls and decreasing pitch (ball to ball). Achieving smaller form factors means also to decrease the thickness of the chip and the package. At a certain level, soldering technology can no longer provide the required placement accuracy so that Thermal-Compression-Bonding needs to be applied. Fan-In Packaging is used when additional redistribution layers are needed for arranging the pads on the chip (peripheral-arrayed) to a much larger pitch (area-arrayed) with larger balls [7].

System in Package

System-in-Package is the integration of various similar or dissimilar chips on a common substrate, mostly placed next to each other but also vertically stacked. Either packaged chips or bare dies can be used for integration. This approach brings the huge benefits of simplifying design requirements for individual dies and therefore reduced costs and time-to-market while at the same time remaining high integration levels. The following figure illustrates the approach of SiP technology [1, 4, 7].

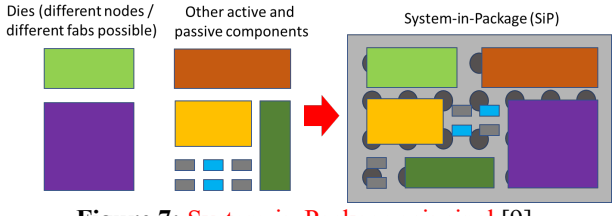

Figure 7: System-in-Package principal [9]

Fan-Out Packaging

Fan-out Packaging was first introduced by Infineon under the name of embedded wafer-level BGA (eWLB) in 2001. The main advantage was that no wire bonding or package substrates are needed anymore which results in a huge cost reduction, better performance and higher-density packaging. Furthermore, the technology has been adopted for multi-chip integration, which is a key technology enabler for highly integrated System-in-Package designs. Three major process technologies exist which will briefly be introduced [7, 10]. The "die-first, face-down" approach is the most common one. Known-good-dies (KGD) are placed on a release layer and molded via compression molding. Afterwards, the sacrificial carrier is removed and the molded dies are bonded to another supporting wafer. Next, the KGDs are redistributed using photolithography and electroplating processes, which will be introduced in a later section [7, 10].

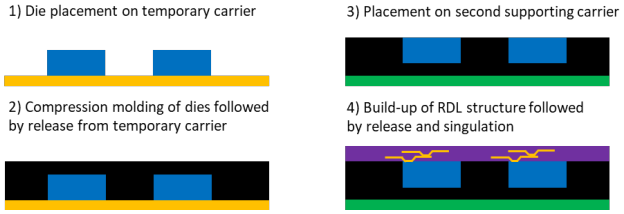

Figure 8: Fan-Out process principal "die first, face-down" [7]

The second approach "die first, face-up" is aiming at eliminating one debonding step. Therefore, the die needs to be equipped with copper contact pads. The backside of the KGDs are equipped with a Die-Adhesive-Film and are bonded to the release layer on the sacrificial wafer. The KGDs are embedded using compression molding technology. As the copper pads are molded as well, consecutive grinding of the molded substrate is needed to make pads accessible. Afterwards, the RDL can be build up accordingly [7, 11].

The third approach "RDL first, die last" is based on the AMKOR SWIFT™ technology. For the other processes, it cannot be guaranteed that the KGDs will survive RDL processing which consequently reduces manufacturing yield tremendously. Furthermore, full testing after RDL build-up is cost intense. Therefore, building the RDL first and connecting the dies to the RDL afterwards is a promising approach to increase manufacturing yield [7].

Next, the RDL build-up will be introduced. First, photosensitive PI is spin coated on the molded dies. The PI is partially exposed and developed afterwards. A seed layer is sputtered on top of the PI. Afterwards, the photoresist is applied and structured by using traditional photolithography processes. Then, the RDL is electroplated. Finally, the resist is stripped and the remaining metal layer is etched. Consecutive RDL layers can be build-up accordingly [7].

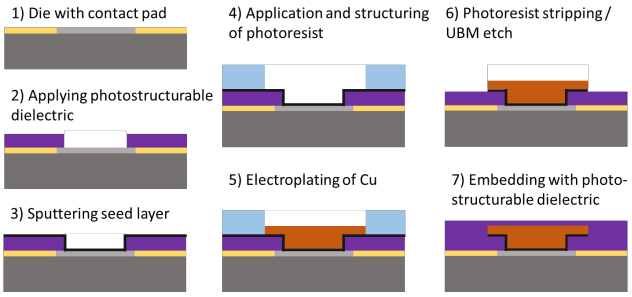

Figure 9: RDL build-up – process principal [7]

3D Packaging

As integrating functionality horizontally is becoming ever more challenging as stated above, vertical integration is gaining huge popularity. Two approaches are commonly applied: Wire bond-based stacking and Package-on-Package stacking. Wire bonded stacks are especially famous in memory stacking. PoP processes are often used for placing the processor closer to the memory. This is especially suitable when footprint is limited, e.g. in smartphone applications. Both concepts are illustrated in the following figure [7, 12].

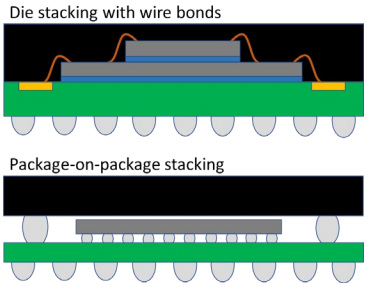

Figure 10: Comparison of wire bonded stack and PoP approach [7]

For high-bandwidth memories, the single DRAM dies are stacked using TSVs and micro bumps. The HBM is than placed directly next to the processing chip on a Si interposer. TSV stacking allows faster communication and lower energy consumption compared to wire bonding technology [7, 13].
In the following, the TSV fabrication process will briefly be discussed. First, a SiO_2 layer is put on the Silicon. Afterwards, a photoresist is applied and structured accordingly. The SiO_2 is etched and a DRIE process is used to etch the TSV structure into the Silicon. In the following, another layer of SiO_2 and a barrier layer followed by a seed layer of Cu are deposited uniformly. The Cu is then electroplated over the entire surface in order to fill the TSVs entirely. In a final process step, the top part of the electroplated Cu and the barrier layer is polished using CMP. In further processing, the TSVs can be rerouted using RDL processes [7, 13].

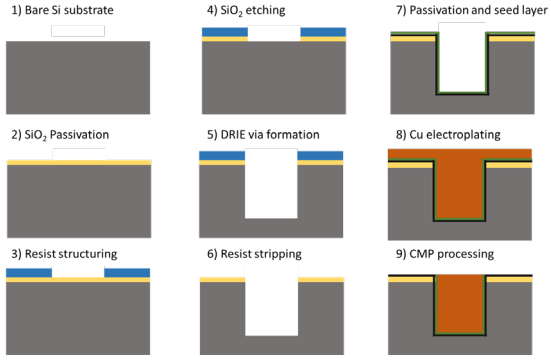

Figure 11: TSV formation using Cu electroplating [7]

3. Heterogeneous Integration Roadmap

The aim of the heterogeneous integration roadmap is to give a guideline for technological advances for the next 15 years. This should stimulate collaboration between industry partners and thereby shorten development cycle times. Heterogeneous integration is gaining interest due to Moore´s Law ending leading to higher costs for further downscaling transistor size. The approaching end of Moore's law also lead to ending work on the International Technology Roadmap ITRS in 2016 which has been the main roadmap for technological developments since 1991 [9, 14].

In [9], Heterogeneous Integration is defined as:
"[…] integration of separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics."

Therefore, small functional components are packaged separately in order to build-up the system level functionality. The need for further integration is powered by demanding applications of several industry sectors. These research fields and their key building blocks are illustrated in the figure below [9].

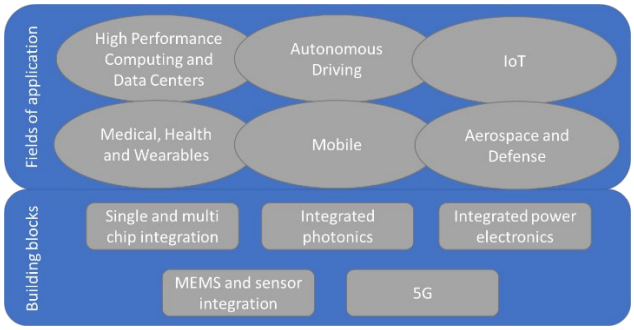

Figure 12: Fields of application and underlying building blocks for heterogeneous packaging [9]

As can be seen, when it comes to further integrating functionality on smaller footprint, heterogeneous integration is gaining significant importance. Especially for advanced node technology, splitting monolithic SoCs in their building

blocks and couple them via interposers can already be more cost efficient (depending on application). There is a vast variety of technologies to integrate the 3D and heterogeneous integration. To select the right process technology for a certain application, detailed understanding of the advantages and disadvantages of each kind is necessary [4, 9, 14].

4. Applications

Overview about Megatrends

Currently, many promising megatrends are being foreseen by industry and academia based on recent technological advances. Powered by massively increased computing performance and improved algorithms, artificial intelligence is one of the recent trends with the potential to change all industry sectors. In the following, recent chip architecture to power artificial intelligence computing will be discussed. In Automotive, autonomous driving is currently one of the hot topics. One issue to tackle is the sensing of the surroundings of the car. Therefore, many MEMS sensors are needed which are improved by advanced packaging methods. To enable the mentioned technology and furthermore the Internet of Everything, 5G communication is seen as one of the main technology enablers. Due to the integration of RF functionality in the packages, technological challenges need to be overcome. The following sections are introducing some of the applied technological solutions for packaging such devices.

High performance computing and Artificial Intelligence

Each industry sector has their own motivation for demanding increased computing power. IoT applications need high IO connectivity to sensors/actuators, processing of sensor fusion and cloud data analysis. Data analytics like used in e-commerce or financial services are applied to data sets, which have to be processed and analyzed. The use of FPGAs and GPUs is meanwhile widespread here for processing. Machine Learning is using GPUs, FPGAs and special purpose accelerator chips for neural networks. Distributed ledger technology can be applied beyond finance, e.g. for voting, governance, healthcare. They demand highly parallelizable, specialized engines [15].

The idea of providing software with a certain kind of learning capability like AI is not a new idea [16]. What was always missing is the needed computing power to process a huge amount of data. Necessary hardware requirements could just be fulfilled due to technological advances in the last couple of years. Artificial Intelligence is generally described as the ability of computers to perform tasks, which normally require human intelligence. Deep Learning and Machine Learning can thereby be seen as sub-branches of AI. Providing this kind of computing power needs highly integrated packages [17].

First AI packages were using high performance FPGAs and GPUs. Meanwhile, the packages changed to integrating highly specialized ASIC dies. One of the main issues to tackle is the high amount of energy needed. In [18] it is stated, that the worlds data centers make roughly 10% of the world's total energy demands. The amount of energy consumption can be reduced significantly by placing chips closer to one another [18].

Further steps in high performance computing are limited by the performance gap between DRAM memory and processing chips. This obstacle is mostly overcome by hard- and software approaches. When it comes to packaging, the metrics are low latency and high bandwidth demands. This is challenging when placing the DRAM next to the chip due to the wiring characteristics. Therefore, high pin count and low wiring length are needed. Using Si interposer integration is decreasing wiring length significantly. Another approach is to stack the DRAM dies directly on the ASIC, which is more challenging due to thermal management. Furthermore, most AI ASICs are equipped with a buffer memory like stacked SRAMs. The schematic of a standard AI processor with buffer memory can be seen in Figure 13 [15,18].

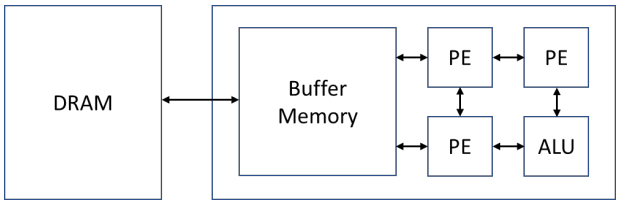

Figure 13: Architecture of an AI ASIC with buffer layer for communication with DRAM (PE = processing element; ALU = arithmetic logic unit) [18]

Another downside of SoC chips used in AI packages is caused by the monolithic design. Each block of the die is having its own challenges when it comes to the manufacturing technologies. These requirements all have to be met on a single die using only one process technology for all blocks. This can lead to having to make compromises on some end. Therefore, it can be more cost efficient to manufacture single units like CPU or SRAM on different platforms or even by different Fabs and combining them via SiP technology [4, 18].

When it comes to data center technology where many data has to be handled, the HBM2 memory is an incremental part of the architecture. Most manufacturers are thereby combining the memory stack with an FPGA or an ASIC die on a Silicon interposer. The Chip on Wafer on Substrate architecture (CoWoS) is one of the best representatives of using a Si interposer to connect HBM2 and processing unit (see figure below) [7, 17].

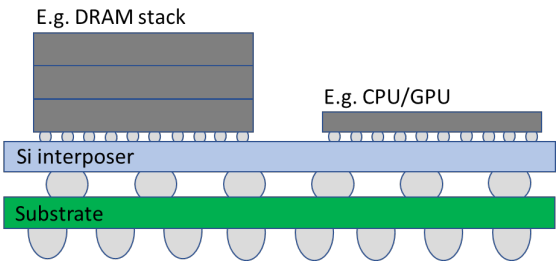

Figure 14: CoWoS packaging principle [19] [7]

Future technologies will focus on eliminating the Si interposer from the package due to cost intense processing and its thickness. The most common approach is to replace the interposer with an RDL-based interlayer. This would provide very fine pitch which is promising but still in the research phase. By using high-density Fan-Out technologies, latency and power loss due to wiring length can be decreased tremendously. The move to organic substrates for cost reduction is another area of interest [15, 17, 18].

Intel's approach for not having to use Si interposers are bridge dies embedded during substrate fabrication process (so-called EMIB dies). During the manufacturing of the board substrate, Si dies are integrated in order to "bridge" the top dies, which are assembled to the board later [15, 20].

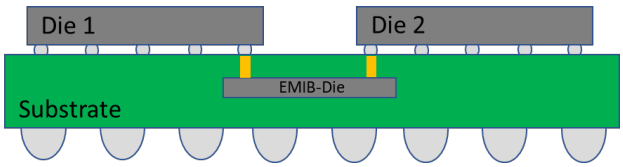

Figure 15: Intel EMIB packaging principle [20]

Another area of research are denser and improved vias. The smaller the vias are getting, the more important will be the characteristic impedance for high-speed signals. Further research will be done on embedded die bridges to incorporate materials like glass to make this technology even more economical. When it comes to TSV scaling the aspect ratio of 10:1 is likely to remain. Hybrid bonding is a further important technology gaining more and more interest from industry. Wafer-to-wafer or die-to-wafer bonding is used to connect opposing dies or wafers via temperature and pressure so that Cu pads are connected which can be used for very high-density packages [15, 21].

Smartphone Technology and 5G

The mobile market is one of the major innovation drivers in the electronics industry. Key areas of electronics development are thereby OLED display technology, multi-camera systems, 5G modules, AI capability, 3D sensing and AR/VR. There are roughly 20 SiPs in each smartphone. The following figure illustrates key components in a standard smartphone [5, 22].

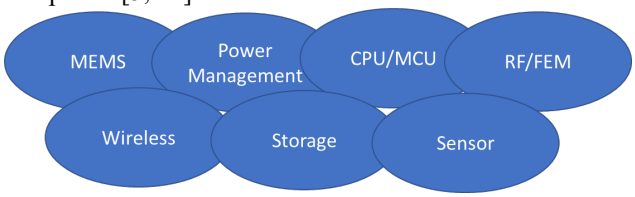

Figure 16: Key electronic components in a Smartphone which need to be miniaturized [22]

Three types of packaging are commonly applied for the application processor: Stacked-die-in-Package, Flip Chip Package-on-Package and Fan-Out PoP technology (Apple only). The Stacked-die approach is used to place DRAM and processor in close proximity. The processor could for example be an FC CSP placed on the substrate and a memory chip can be placed on top of the processor and be contacted using wire-bonding [22, 23].

PoP technology is mainly used for high performance processors with high I/O count. TSMC is packaging the Apple iPhone processor using their very own InFO technology, whereby Qualcomm is using a flip chip PoP approach to package their chips. PoP technology compared to FO packaging is limited due to heat dissipation and memory bandwidth [5, 7, 17, 24].

To provide the smartphone with 5G capability a 5G baseband component, RF module and antenna/transceiver modules need to be added to the boards. In general, SiP approach is commonly applied to combine the vast variety of technological requirements in one system [25]. For the integration of the Antenna, two approaches can be taken: Antenna on Chip or Antenna in Package. The first one offers the advantage of integrating all modules on a single chip, which results in a very small footprint. Disadvantages are the radiation characteristics of Si. Antenna in Package is placing the antenna module on a separate substrate, which allows high element density. New materials have to be introduced also due to the need for enhanced EMI shielding. An AiP using PoP technology can be seen in the following figure [22, 26, 27, 28].

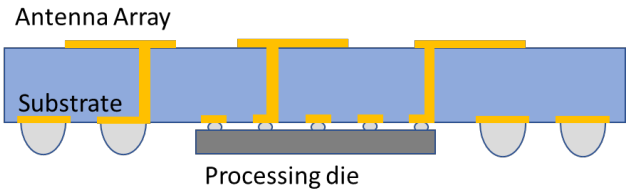

Figure 17: Antenna-in-Package system principal [27]

The main challenges for 5G packaging are the close integration of multiple components, low surface roughness for improved signal quality, reduced CTE mismatch, the

demand for novel materials and accurate multi-physics modeling. Challenging is the fact that digital communication demands higher IO count which results in the need for fine-pitch IO and therefore L/S reduction. Current 4G LTE modules are build using FC technology whereby finer pitch and thinner substrates are needed for 5G [22].

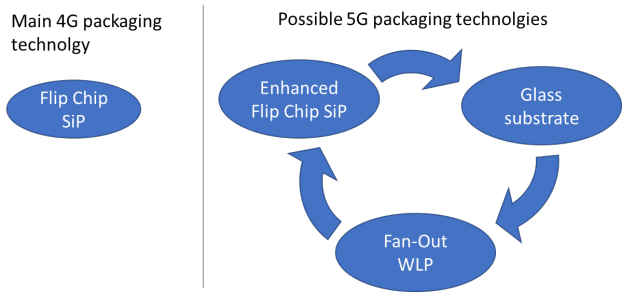

Figure 18: Main technologies for 4G and 5G packaging [29]

Possible substrate materials for 5G packages are LTCC (ceramic), low-loss laminates, fan-out or glass. Glass offers best signal quality due to its low surface roughness. The material has to be chosen dependent on microwave properties, cost, manufacturing yields, scalability, and reliability [22].

There are different technologies applied in order to tackle the EMI-shielding issue: metal caps, plating, spray coating, sputtering, and wire bonding [26]. The underlying principle is comparable to a Faraday cage. Parasitic EMI radiation cannot penetrate through the shielding. In the following figure a Henkel technology for compartmental shielding is shown [30]. Molded sections can be divided by laser ablating and consequent filling, e.g. with Ag-based shielding materials. In contrast, spray coating or even sputtering can be used for conformal shielding [30, 31].

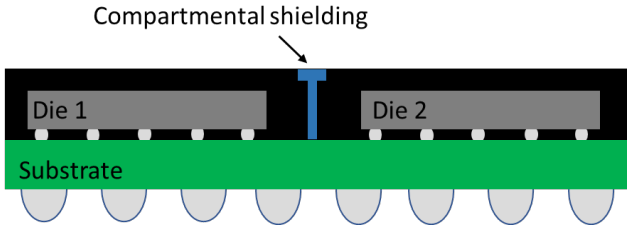

Figure 19: Compartmental shielding [30]

Automotive Technologies

Nowadays, a significant percentage of innovation in automotive comes from the electronics in the car. This refers to power conversion, ADAS sensors, MEMS & Sensors, Lighting, Processing & Storage, connectivity, and Displays. The following table gives an overview about the different electronic components in a car [32, 33].

Table 1. Main electronics in a car [32]

Application	**Components**
Power conversion	MOSFET, IGBT, converters, BMICs
ADAS sensors	Radar, LiDAR, CIS, Infrared Imager
MEMS & sensors	Accelerometer, Gyroscope, Microphones, Micromirror, Magnetometer, Humidity sensor, Pressure sensor, Micro bolometer, IMUs, Ultrasonic sensors
Lighting	Front light, Rear light, Interior lighting
Processing & Storage	CPU/GPU, Memory, ECU, MCU
Connectivity	Antenna, Wi-Fi, Switch, GPS
Display	Screens and ToF

Nowadays, electronics make around a third of total costs in a car. The main drivers for technological advances in the car are autonomous driving, communication and infotainment, and electrically powered cars. The limiting factor for electronics is weight and volume so that more integration is needed. Hundreds of sensors and computing processors have to be combined, electronics for all-electric driving have to be developed further, data handling has to be taken care of and cost, safety and reliability challenges have to be tackled [33, [34].

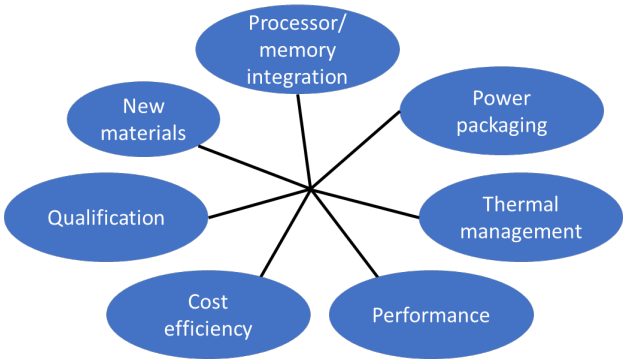

Figure 20: Main challenges for automotive packaging [34]

The number of assistance-systems in the car is constantly rising. These developments aim to bring fully autonomous cars to the market. To structure this process, the levels of automation have been defined according to the following table. The cars currently available on the market can reach level 2. However, tremendous research is done trying to reach higher levels [35, 36].

Figure 21: Main challenges for automotive packaging [36]

When it comes to connectivity & communications there are three major types: Intra Vehicular, Vehicle-to-vehicle (V2V) and Vehicle-to-X (V2X). Intra vehicular communication is mostly wire based mainly via CAN and Ethernet communication, but new standards with higher communication rate are about to be used widely. A challenge that comes with this kind of performance is to manage power and heat within the packages. V2V communication aims to exchange information between cars on the road and thereby raise awareness of the surrounding. This will lead to a lower risk of crashes. Range will be more than 300 m and communication is Wi-Fi-based or cellular. V2X is the communication with other vehicles, pedestrians, infrastructure, internet and the access to information in the cloud [34].

When it comes to driver-assisted systems, the fusion of information from several different sensor systems is crucial. Especially for autonomous driving a clear digital representation of the surroundings of the car needs to be generated [33, 34].

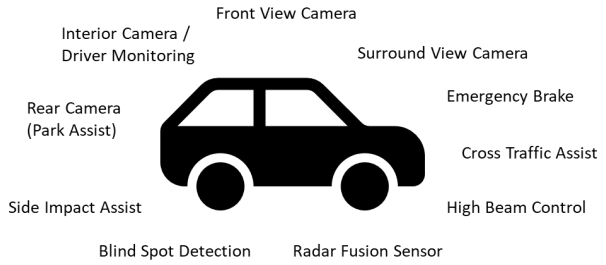

Figure 22: Examples for some common ADAS sensors [34][33]

The HIR is also looking at the processor roadmap for the next 5 to 15 years. It is mainly driven by the development of ADAS processors (high performance processing of sensor data and AI). Two trends can also be seen here, higher transistor density or SiP processing. SoC results in higher costs, which is also to be avoided in automotive industry. SiP results in increased integration risks, higher costs and challenges for reliability. Now common is the use of PBGA and wire bonding technology. Heat spreaders becoming more often applied to tackle increased thermal management demands. Higher density Cu pillar connects are likely to be applied as well as multi-die and stacked die approaches. As for performance computing memory will be integrated into the packages. Materials with better thermal performance need to be applied. In the next 5 years, PoP technology is expected to be integrated widely and looking at the next 10-15 years approaches from high performance computing will be implemented. The integration of 2.5D/3D packaging drives costs and the footprint is increasing due to integrating more components. This is in contrast to the demand for smaller footprints due to weight constraints and thermal management. Increased cooling requirements will consume power, which will have a negative impact on overall efficiency [34, 37].

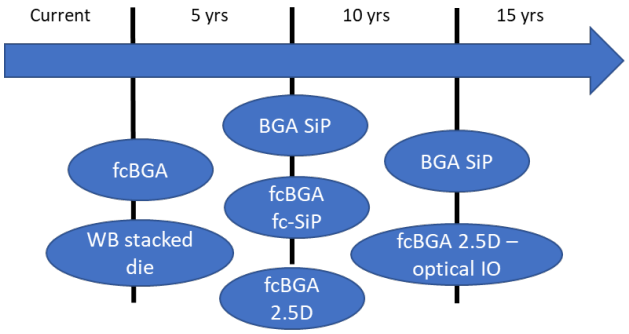

Figure 23: Packaging roadmap for automotive - 15 years forecast [34]

When it comes to reliability, high temperature usage, harsh environments, and long usage-life need to be considered. Therefore, understanding usage scenarios better will be a huge challenge. When it comes to autonomous driving it is possible that cars may drive more than 18 hours per day, so current standards for life time prediction of 15 years based on a much lower daily usage can no longer be applied. Therefore, electronics manufacturers have to guarantee longer lifetime of components while on the same time deliver shorter time to market [34, 37].

Beside the increased challenges for processor packaging, ADAS sensor integration is another huge field of development. There are mainly four types of sensors to analyze the cars surroundings: cameras, Radar, LiDAR and ultrasonic sensors. Cameras are used for lane marking detection, traffic sights, traffic lights, animals, and pedestrian detection. Unfortunately, their performance is limited when challenging weather conditions appear like rain, fog etc. [34]. Imaging cameras are crucial for sensor fusion technologies. Therefore, the demand for high reliability and cost-effective packaging of CMOS image sensors is increasing. Traditionally, ceramics have been used to place the die and use wire bonding for contacting. This is a very cost intense approach. Therefore, in [38] an approach using laminated substrates with bumps is presented [38].

Radar (Radio Detection and Ranging) is working with EM-waves in mm-range and are widely independent from weather and light. LiDAR (light detection and ranging) sensors are

using light from laser diodes, not mm-waves. The light is transmitted using a pulsed-mode and reflections are detected. Using the time-of-flight measurement, information about the surrounding can be gathered. To scan the environment, a scanning device is needed. Currently, three main types are used: Mechanical, MEMS based or Flash-based scanning systems [34].

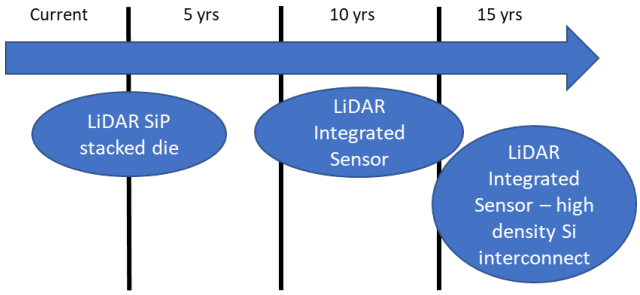

Figure 24: Packaging roadmap for LiDAR sensors - 15 years forecast [34]

Ultrasonic measuring is using the emission of soundwaves and a corresponding time measurement to determine the distance of objects. The range is below 2m so that this kind of sensor is only used for the close environment, e.g. for the parking assistant [34].

A combination of all different sensors is needed for fully autonomous vehicles. Sensor fusion is necessary to process this huge amount of data. There is a huge trend to equip sensors directly with processing chips for direct data analytics or for sensor enhancement by adjusting the sensor parameters for increased measuring quality [34].

Reliability demands in automotive are known to be very challenging. Upcoming trends will have to fulfill these expectations. For electrification of the drive train, the use of SiC is a promising approach as it provides higher efficiency and higher operational temperatures. New encapsulation materials need to be developed to ensure high reliability. Autonomous driving will enable increased operational time, which is further challenging for the reliability of the components. Connectivity electronics are based on consumer electronics technology but they are put in harsh environmental conditions, which has to be taken into account. New methods based on condition monitoring and prognostics and health management will be applied more often in the future to understand failure mechanisms of electronics better. Numerical simulations and machine learning for fault detection and classification will be an integral part of future methodologies [34, 37].

SUMMARY

The demand for further miniaturization of electronic packaging has been introduced. The two approaches “More Moore” and “More than Moore” have been revised. The packaging landscape for further heterogeneous integration has been laid out. Key process technologies (Flip-Chip technology, System-on-Chip, System-in-Package, Fan-out packaging, and 3D integration) have been introduced and their main process steps have been described. Based on that, the heterogeneous integration roadmap was introduced. In the last section, advanced packaging technologies for some of the technological drivers were explained. High performance computing is mainly limited by DRAM processing speed so that processor and memory have to be assembled as close together as possible. Therefore, Si interposers are commonly applied but are comparably cost intense. Development focus is mainly put on finding cost efficient alternatives with high reliability. Smartphone technology is mainly about integrating electronics on a footprint as small as possible. Currently, PoP technology is commonly applied. First manufacturers already moved to Fan-out packaging for even higher integration. 5G packaging comes with many technological challenges. Advantageous for both, Antenna on Chip and Antenna in Package have been stated. When it comes to packaging for automotive, the integration of numerous sensors, processing of the data and the demanding reliability requirements of this industry are the biggest challenges to tackle.

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