MULTI-FACETED APPROACH TO MINIMIZE PRINTED CIRCUIT BOARD WARPAGE IN BOARD ASSEMBLY PROCESS

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ABSTRACT
Customer demands for smaller form factor electronic devices are driving the use of thinner electronic components and thinner printed circuit board (PCB) in the assembly process. The use of thinner components and thinner multi-up panel PCBs (≤ 32mils) has led to warpage issues in the surface mount (SMT) assembly process, which in turn impacts the board assembly yield. PCBs with excessive warpage impact paste print quality in print process and solder joint formation during reflow soldering leading to SMT assembly defects. This publication presents solutions to address the PCB warpage issue. Results from detailed studies on PCB design (multi-pack design, Outrigger copper density), reflow pallet design (material, design) and methods to control and contain PCB warpage are shared. Implementation of the proposed PCB and reflow pallet design recommendations and process control will reduce the impact of PCB warpage and provide improved margin to the board assembly process.

Key words: PCB warpage, PCB design rules, SMT reflow pallet design rules, Warpage mitigation

INTRODUCTION
PCB warpage plays a significant role in the SMT assembly process. The drive for thinner systems and form factor devices has led to use of thinner PCBs (≤ 32mils). Adoption of thinner PCBs has led to multiple issues in the SMT assembly process. Publications [1, 2] have focused on the PCB warpage for thick boards. There is insufficient information in the industry's published literature on how to mitigate the assembly risks associated with thinner PCBs.

The use of thinner PCBs leads to challenges at the solder paste print process (Room Temp) and during the reflow process (High Temp) in the SMT assembly process flow. Uncontrolled or excessive PCB warpage at room temperature creates a gap between the PCB and stencil, preventing constant contact (i.e., gasketing) which results in paste print defects (wet bridging, shifted print deposits and insufficient paste volume). For an acceptable HVM fine pitch print, the stencil and PCB should be in constant contact during the print process (on-contact printing with zero snap-off distance), creating a gasket and more controlled release of the solder paste from the aperture. Excessive PCB warpage prevents proper gasketing between the stencil and PCB. Print defects from high PCB warpage leads to the need for washing off the mis-printed solder paste from the PCB which adds to the through put time (TPT). Print defects may also lead to assembly defects during the SMT process. In the high temperature reflow process, PCB warpage can occur due to PCB design, reflow pallet design and other boundary conditions. Warpage can lead to reflow process related solder joint defects (Head-On-Pillow, Open and solder bridge defects) for Ball Grid Array (BGA) packages [3]. In additional to the defects on BGA packages, excessive warpage at high temperature causes shift/skew defects for leaded, no-lead, and passive components (quad flat package (QFP), quad flat no-lead package (QFN) and connectors). As the temperature increases, the PCB and package expand at different rates due to the coefficient of thermal expansion (CTE) mismatch of the different materials within them, and this mismatch leads to their warpage. Excessive warpage in PCB and or/package can lead to SMT manufacturing related defects.

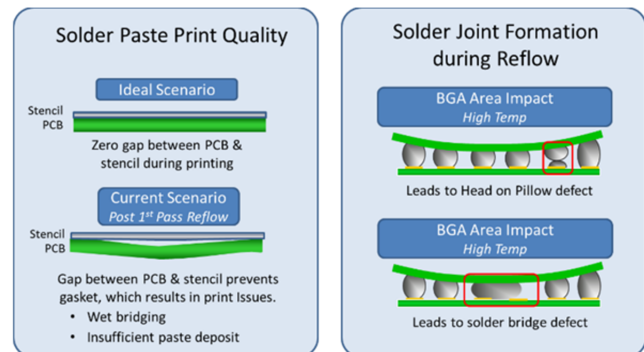


Figure 1. PCB warpage impact to solder paste print process (room temp) and reflow process (high temp**)**

Control of PCB warpage at room temp and high temp is very critical for a successful SMT process. This publication will provide various approaches to minimize or reduce PCB warpage and help improve the SMT process for PCBs with thickness ≤ 32mils.

ADDRESSING PCB WARPAGE
PCB design factors (PCB thickness, PCB dimension, copper layer balance, copper density mismatch, router tab dimension and location, and multi-up PCB design) and SMT assembly process parameters (reflow pallet design, reflow temperature, number of high temperature cycles) can lead to PCB warpage. To reduce PCB warpage and improve SMT assembly process margin, a multi-faceted approach was taken as shown below.

Reduce PCB warpage in design

- Panel/board design guide
- PCB supplier process & conditioning (residual stress)

Control of PCB warpage in assembly process

- SMT reflow pallet design
- 3D vacuum fixture design to flatten the PCB during the paste print process
- Selective de-panelization to minimize PCB warpage for print process

Contain defects

- Monitor & screen solder paste volume
- Non-destructive automated X-ray inspection

Subsequent sections will share the results from each of these approaches.

Shadow Moiré metrology was used to measure & characterize PCB warpage [4, 5]. Warpage measurements were performed at incoming (as received) and after the PCBs were subjected to one reflow cycle (also termed 1st pass reflow). The metrics below were used to characterize warpage in this study

- Absolute warpage = Abs (End of Line 1st pass warpage – Incoming warpage)
- End of Line (EOL) 1st pass warpage

Use of absolute panel warpage eliminates the impact of incoming warpage and enables the true warpage from the DOE variables to be studied.

PCB DESIGN

PCB design plays a critical role in modulating the warpage at room temperature and at reflow temperatures [1]. This study focused on the importance of copper density in the board area and outrigger areas and its impact to warpage. Two PCBs with varying designs were used for the study. Figure 2 shows the image of PCB Design A and Figure 3 shows the image of PCB Design B. PCB design A is a type 3 design (i.e., PTH via design) and PCB design B is a type 4 design (i.e., µvia design). These PCBs will henceforth be referred to as Design 'A' and Design 'B', respectively. Table 1 summarizes the attributes of the PCBs used for the warpage evaluation. In Figure 3, the areas highlighted by the blue boxes refer to the board area (i.e., circuit area) and the outriggers are highlighted by the red boxes. Outriggers in multi-pack designs are used primarily for handling. After assembly, the outrigger is removed (i.e., de-paneled) and the singulated boards move to next assembly process.

Table 1. PCB design attributes

PCB	PCB size (LxW) in	PCB Thickness (mils)	PCB Design Type	Multi-pack design
Design A	10.69x7.00	32.0	Type 3	2 – up
Design B	7.90x5.50	32.0	Type 4	4 – up

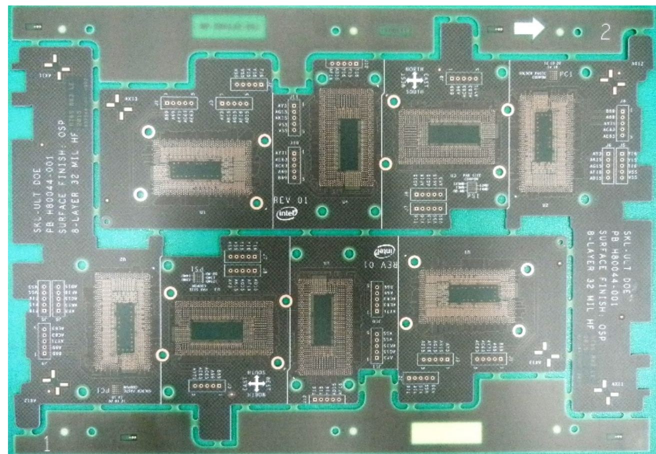


Figure 2. PCB Design A

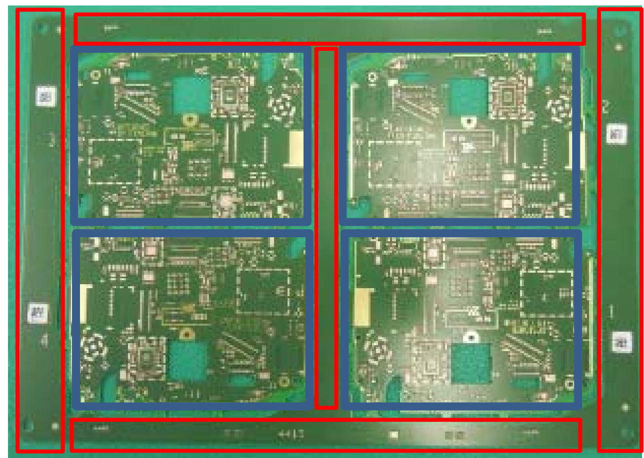


Figure 3. PCB Design B

Copper balance across PCB layers

One approach to minimize PCB warpage is to balance the copper distribution across the PCB layers. Balancing of copper distribution helps minimize the CTE mismatch and warpage at both room temperature and reflow temperature. However, it might not be always possible to match the copper distribution across layers due to design constraints. Table 2 shows the copper distribution across the PCB layer for Design A and it is apparent that layer 1 is matched to layer 8, layer 2 is matched to layer 7 and so on for rest of the layers. Copper distribution difference of ≤10% is considered matched and helps minimize PCB warpage. However, due to design constraints copper balancing across the PCB layers was not achievable for Design B. Copper distribution by layers is shown in Table 3.

Table 2. PCB copper distribution by layers for Design A

Layers	Board area copper density [%]	Layers	Board area copper density [%]
Layer 1	32%	Layer 5	89%
Layer 2	89%	Layer 6	25%
Layer 3	26%	Layer 7	88%
Layer 4	89%	Layer 8	28%

Table 3. PCB copper distribution by layers for Design B

Layers	Board area copper density [%]
Layer 1	69%
Layer 2	80%
Layer 3	85%
Layer 4	67%
Layer 5	91%
Layer 6	72%
Layer 7	86%
Layer 8	77%
Layer 9	81%
Layer 10	78%

Outrigger Copper Density impact to PCB warpage

Another factor that plays a critical role in modulating PCB warpage is the copper density in the outrigger area when compared to the board area. Below is an example of the same PCB design (Design B) manufactured by the same supplier (supplier A) at two sites (site A & C). Design notes for the PCB called out for metallization presence in the outrigger without detailing the copper density requirement. Since there were no requirements, each site used their own rules which drove different PCB warpage signatures for the same PCB design. Site A fabricated the PCB where the copper density distribution in the panel outrigger for each layer was significantly different from the board area (Table 4). This led to a PCB warpage of 2913 um post 1st pass reflow. Site C fabricated the PCB with the copper density distribution in the panel outrigger matching the board area for few layers (6 layers were matched out of 10 layers) (Table 4). Site C had more layers matched when compared to Site A, which led to a reduction in PCB warpage for the same design to 738 um when compared to Site A (2913um). An unbalanced copper ratio between the outrigger and board area leads to varying rates of thermal expansion during reflow and drives the warpage signature of the PCB.

Table 4. Outrigger copper density compared to board area copper density

Supplier 'A' Site 'A'

Layer	Outrigger (%)	Board (%)	Board+Outrigger (%)
Top	85.52	66.00	64.03
L2	32.24	76.00	56.71
L3	32.38	81.00	59.30
L4	33.74	64.00	50.47
L5	33.88	87.00	61.99
L6	33.74	69.00	52.02
L7	32.38	83.00	59.58
L8	32.24	74.00	55.04
L9	32.38	78.00	56.93
Bottom	85.52	75.00	68.84

Supplier 'A' Site 'C'

Layer	Outrigger (%)	Board (%)	Board+Outrigger (%)
Top	72.50	64.88	67.82
L2	67.63	76.29	72.95
L3	67.54	81.06	75.85
L4	68.56	65.02	66.39
L5	33.81	86.89	66.41
L6	67.73	69.38	68.75
L7	33.95	82.71	63.89
L8	66.91	74.92	71.83
L9	66.77	78.12	73.74
Bottom	68.37	74.46	72.11

To validate the hypothesis of unbalanced copper distribution in outrigger in driving excessive PCB warpage, 2 design of experiments (DOEs) were designed. 1) DOE 1, whose goal was to validate the impact of outrigger copper density to panel warpage. 2) DOE 2, whose goal was to rule out the impact of supplier site/manufacturing process.

For DOE 1, PCB Design A was designed with 3 different copper densities in the outrigger when compared to the board area. These are given below.

- Unbalanced – Copper density in outrigger varies significantly from board area for each layer
- Balanced – Copper density in outrigger matches to board area for each layer (1:1)
- Full Metal – 100% copper density in outrigger irrespective to board area copper for each layer

A sample size of 5 PCBs were used for each condition. PCBs were sent through the reflow oven to simulate 1st pass reflow and warpage measurements using Shadow Moiré was performed on the boards. Figure 4 below shows the PCB warpage as a function of outrigger copper density. DOE 1 results show that an unbalanced copper condition drives significant warpage in the PCB when compared to a balanced and full metal condition, as expected.

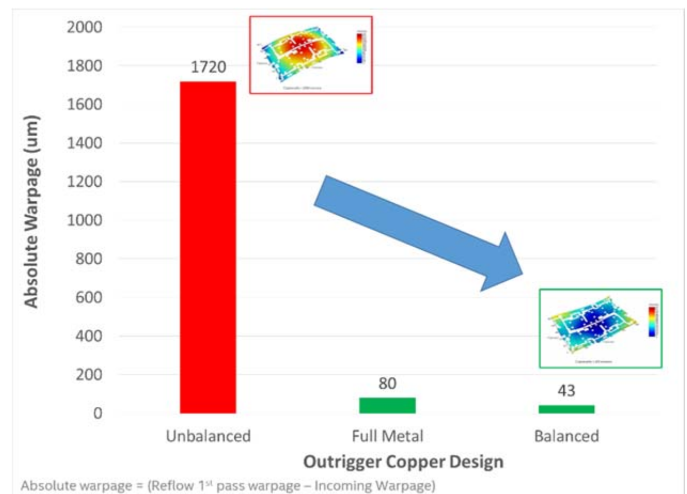


Figure 4. PCB warpage as a function of outrigger copper design

In DOE 2, PCB Design B with the balanced outrigger copper design was manufactured at site 'C' and at site 'A'. Unbalanced outrigger copper design from site 'A' was used as a control leg to reproduce the high warpage. As with DOE 1, a sample size of 5 PCBs was used for this DOE and the warpage data was collected using Shadow Moiré on post 1st pass reflow PCB. Figure 5 shows the PCB warpage as a function of outrigger copper design and manufacturing site. DOE 2 results show that if the same outrigger copper design is manufactured at two sites, then the PCB warpage is in the same range, validating the hypothesis that manufacturing site variation does not significantly impact the PCB warpage.

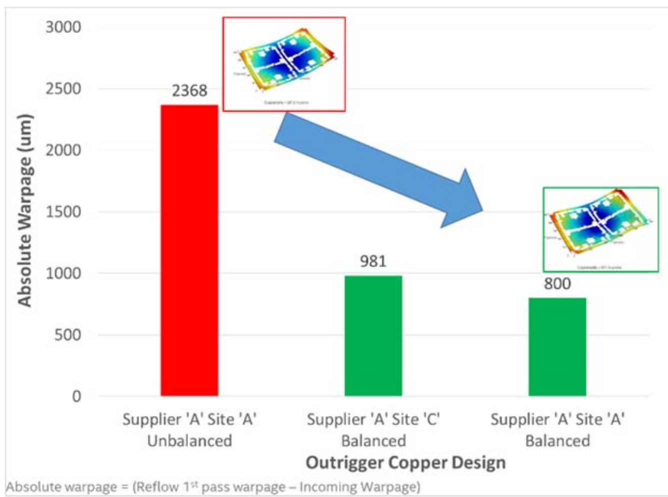


Figure 5. PCB warpage as a function of outrigger cu design and manufacturing sites

Based on the DOE 1 & DOE 2 results, the hypothesis that outrigger copper density plays a significant role in modulating the PCB warpage was validated. In order to define an outrigger copper design recommendation, a DOE with 5 legs was designed on PCB Design A and PCB Design B boards where the outrigger copper density for each layer was matched, increased by 10%, decreased by 10%, 20% and 30% when compared to the PCB copper density. PCBs were manufactured at the same site and a detailed layer by layer comparison was provided by the PCB vendor to validate the design requirements. Table 5 shows the DOE leg with PCB and outrigger copper density for PCB Design A and PCB Design B.

Table 5 (a). DOE leg with PCB and outrigger copper density for PCB Design A

DOE Leg	Board Copper	Outrigger Copper
1:1	67 to 91%	67 to 91%
+10%	67 to 91%	77 to 87%
-10%	67 to 91%	57 to 81%
-20%	67 to 91%	47 to 71%
-30%	67 to 91%	37 to 61%

Table 5 (b). DOE leg with PCB and outrigger copper density for PCB Design B

DOE Leg	Board Copper	Outrigger Copper
1:1	25 to 89%	25 to 89%
+10%	67 to 91%	34 to 94%
-10%	67 to 91%	14 to 79%
-20%	67 to 91%	10 to 69%
-30%	67 to 91%	5 to 59%

PCBs were sent through the reflow oven and warpage was measured using the Shadow Moiré post 1st pass reflow. For each leg, a sample size of 5 PCBs was used. Figure 6 and 7 shows the PCB warpage vs. copper density for PCB Design A and PCB Design B.

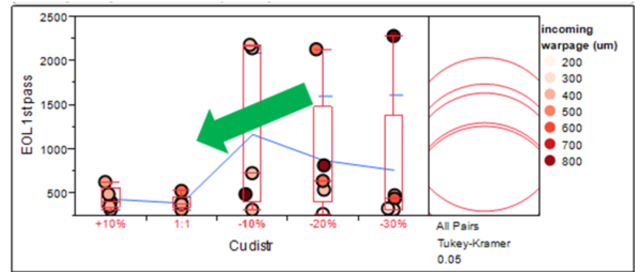


Figure 6. PCB warpage vs. copper density for PCB Design A

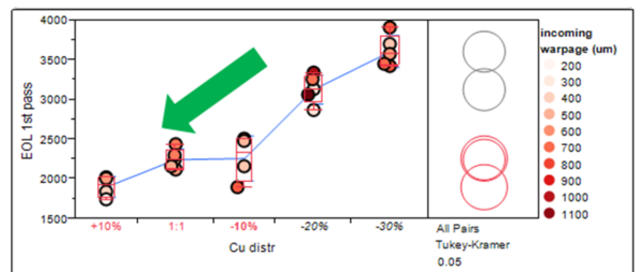


Figure 7. PCB warpage vs. copper density for PCB Design B

Review of the data from the above two figures shows that matching of outrigger copper density to board area copper density reduces end of line (EOL) PCB warpage. A Higher mis-match of copper density between outrigger and board area, leads to a higher PCB warpage. Matching of copper density reduced the thermal expansion mismatch across the board area during the reflow process and thereby helps to minimize PCB warpage.

To minimize panel warpage, outrigger copper area for each layer needs to be 100-120% of the single image copper area for that layer. For example, if a board area copper density is 50% for a layer, then the outrigger copper density for the layer should range from 50 to 60%.

PCB Supplier Pre-Treatment

PCB manufacturing sites use pre-treatment to minimize PCB warpage. In order to understand the impact of these pre-treatments to warpage, a DOE was performed where PCBs were baked at 165° C for 3.5hrs (i.e., pre-treatment before ship to end customers). Pre-treatment temperature of 165° C was chosen based on the Tg of the PCB laminate. For this DOE, PCB glass transition temperature (Tg) was 150C and a 15C delta was added so that it would soften the PCB and minimize the warpage. Figure 8 and 9 shows the room temperature (incoming PCB with no reflow condition) and high temperature warpage for the No pre-treatment (i.e., as manufactured) and Pre-treated condition. As expected, pre-treated PCB showed significant lower warpage at room

temperature when compared to the No pre-treated condition. Baking the PCB above the T_g helps to soften its laminate and minimize its warpage. However, when the PCB is heated, the thermal expansion drives the warpage and no difference in warpage is observed between the pre-treated and non pre-treated condition.

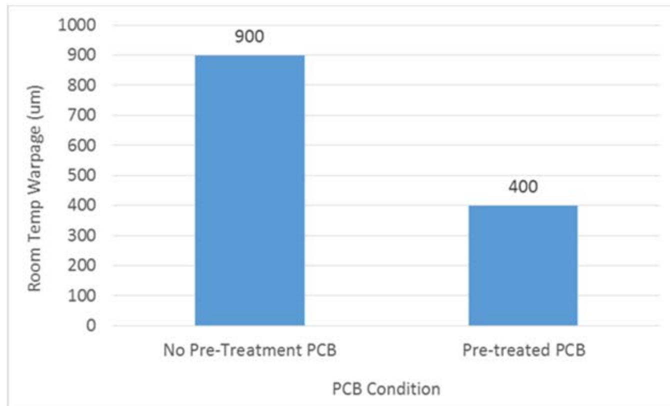


Figure 8. PCB Room Temp warpage for No Pre-treatment vs. Pre-treatment condition

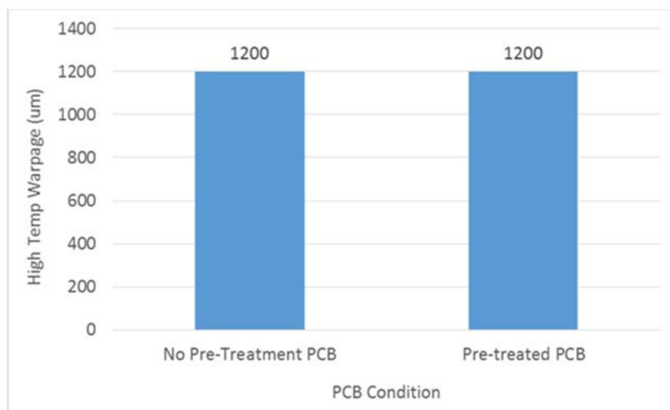


Figure 9. PCB High Temp warpage for No Pre-treatment vs. Pre-treatment condition

To summarize, PCB pre-treatment helps to minimize warpage only at room temperature, no benefit at high temperature.

PCB WARPAGE CONTROL APPROACHES

In this section, we cover approaches that can be utilized to control PCB warpage in the SMT assembly process. Controlling PCB warpage in assembly process is critical to achieve consistently high assembly yield.

Reflow Pallet Design

Reflow pallet design plays a significant role in modulating PCB warpage. To understand the impact, PCB design A was run through the reflow oven with 5 different reflow pallet designs and warpage measurements were taken post 1st pass reflow. The 5 different reflow pallet designs are described below.

- Tensioned + Z constraint. In this design, the PCB was stretched in four corners using a tooling pin with a spring loaded mechanism which puts the PCB in tension laterally. Additionally a magnetic top plate was used to clamp the PCB in the z-axis. In this design, it was expected that putting the PCB in tension and adding a constraint from the top would minimize the PCB warpage.
- Unconstrained + Kapton tape. In this design, the PCB was placed in a supported pallet without any constraints. Kapton tape was used to secure the PCB in the four corners.
- Z constraint pallet. In this design, the PCB was placed in a supported pallet without any constraints and a magnetic top plate was used to constrain the PCB in Z-direction.
- Bare PCB. PCB was reflowed without a reflow pallet.
- Unconstrained. In this design, the PCB was placed in a supported pallet and no constraints were applied to the PCB.

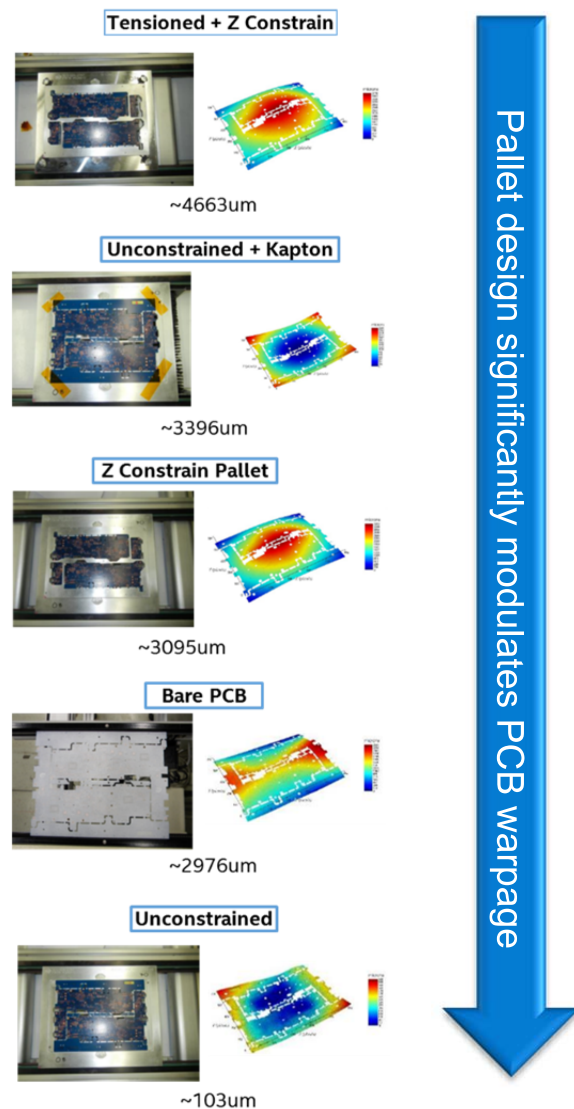


Figure 10. Impact of reflow pallet design to PCB warpage

As shown in Figure 10, reflow pallet design plays a significant role in modulating the PCB warpage for the same PCB design. PCB warpage ranged from ~4500um to ~100um based on the reflow pallet design condition for the PCB with thickness of 32mils. Pallets which used the maximum constraints (tension + Z) showed the maximum warpage, while the pallet with the least constraints (unconstrained) showed the minimum warpage.

Based on our internal DOEs, the following three factors, shown in Figure 11, were identified to be the reflow pallet design factors that are fundamental to a modulating board warpage.

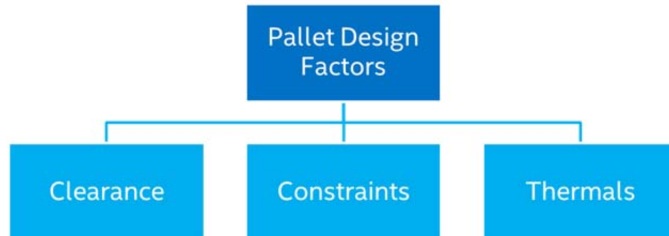


Figure 11. Reflow pallet design factors

Thermals

Maintaining a thermal equilibrium between the pallet and PCB plays a significant role in minimizing the PCB warpage. Differences in temperature allows for different rate of expansion and the higher the temperature difference, the higher the resulting PCB warpage. Thermal mismatch is the paramount reflow pallet design parameter out of the 3 factors identified. To quantify the impact of thermal mismatch (or Delta Temp) to PCB warpage, a DOE was designed with four different pallet designs. These four designs are described below. Each of these reflow pallets were designed with 1.0mm clearance and the least constraints.

- Aluminum Tensioner. Pallet material was Aluminum and the PCB was stretched in all four corners using the tooling pin and spring load puller which puts the PCB in a tension condition (Figure 12 a.)
- Composite Swiss cheese Design. Pallet was made with a composite materials (Durapol) and the PCB was supported by ribs with end clamps. Also holes were added in the outrigger area (Swiss cheese) to provide paths for air flow (Figure 12 b.)
- Aluminum Peg Design. Pallet material was Aluminum and the PCB was supported by pins where possible with end clamps (Figure 12 c.)
- Composite Peg Design. Pallet was made with a composite material (Durapol) and the PCB was supported where possible by pins with end clamps (Figure 12 d.)

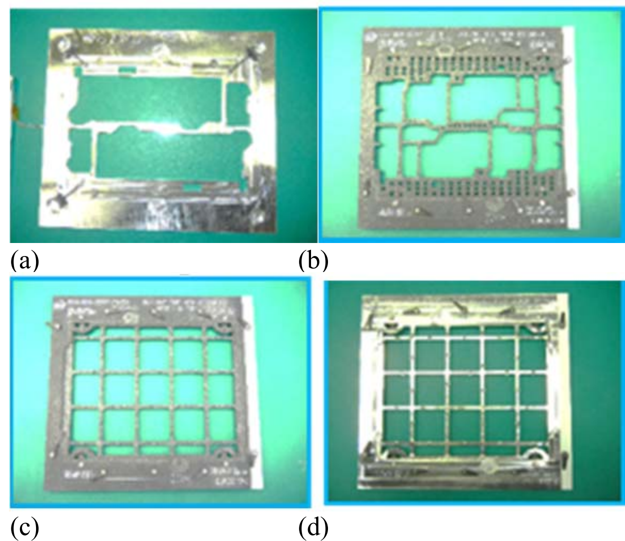


Figure 12. Pallet design for thermal mismatch experiments

Thermocouples were attached to the PCB and pallets to measure their temperature during the reflow process. After 1st pass reflow, PCB warpage was measured using Shadow Moiré metrology. Absolute panel warpage was calculated from the difference between reflow 1st pass warpage and incoming warpage. Figure 13 shows that higher thermal mismatch across the PCB and pallet drives higher PCB warpage post 1st pass reflow. Aluminum tensioner with the higher delta temp showed the higher PCB warpage. The composite material peg design showed the least delta temp and least PCB warpage.

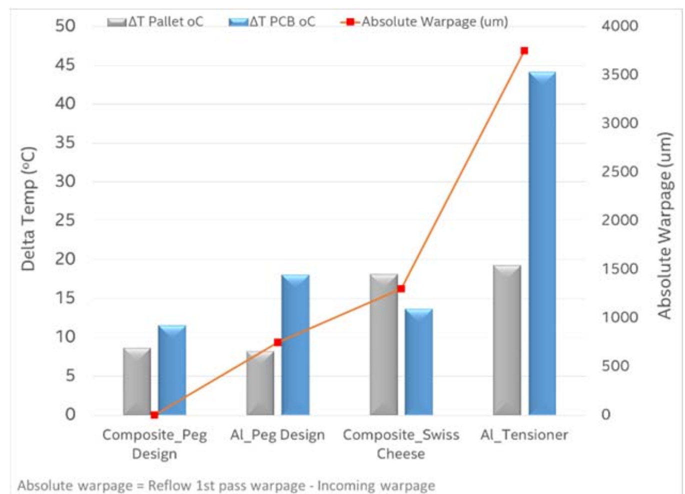


Figure 13. Impact of thermal mismatch to PCB warpage

Additionally, the type of pallet materials used also impacts PCB warpage. A comparison of peg design with the composite and aluminum material showed lower PCB warpage with the composite material due to a lower thermal mismatch driving the rate of thermal expansion.

Clearance

Clearance is required to compensate for PCB & Pallet thermal expansion. The Board and the pallet will expand at

different rates during reflow due to a difference in their thermal mass and a clearance is needed between the PCB and the pallet to prevent interference during SMT reflow. Figure 14 highlights the impact of the thermal expansion and why clearance is required in reflow pallet design.

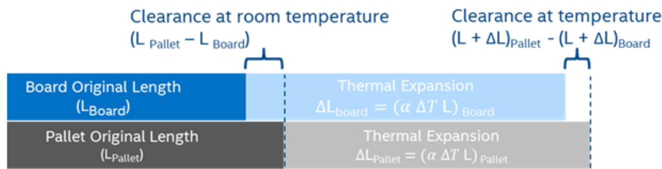


Figure 14. Impact of thermal expansion to reflow pallet clearance requirements

To calculate the clearance required for a reflow pallet, the equation below is used

Clearance = $L_{Pallet} - L_{Board} = L_{Board}\ ((\alpha\ \Delta T)_{Board} - (\alpha\ \Delta T)_{Pallet})$

Below is an example on how to calculate the clearance needed for a PCB length of 500mm. Reflow temperature information is used to calculate the delta temperature in the PCB and pallet. Figure 15 shows a reflow profile with PCB and pallet temperatures.

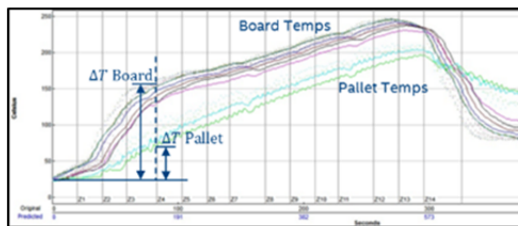


Figure 15. Reflow profile with PCB and pallet temperature

Measured Thermal Profile:

PCB:

Length = 500 mm, CTE = 17 ppm/°C & ΔT = 125°C

Pallet:

CTE = 11 ppm/°C & ΔT = 50°C

Required Clearance:

Clearance = $L_{Pallet} - L_{Board} = L_{Board}\ ((\alpha\ \Delta T)_{Board} - (\alpha\ \Delta T)_{Pallet})$

= 500 mm (2125 ppm – 550 ppm) = 0.7875 mm

Based on the thermal expansion equation, a clearance of 0.40mm is required for each PCB edge to compensate for the difference in thermal expansion between PCB and pallet. Lack of clearance will cause expansion constraints and will induce warpage in the PCB. To highlight the impact of clearance, a DOE was performed using a known high risk warpage PCB with 32mil thick for 0.5mm and 1.0mm reflow pallet clearance. Reflow pallets with 0.5mm clearance constrained the PCB from expansion which led to excessive warpage (~1600um), while the 1.0mm clearance allowed for PCB expansion and minimized PCB warpage (~110um), as highlighted in Figure 16.

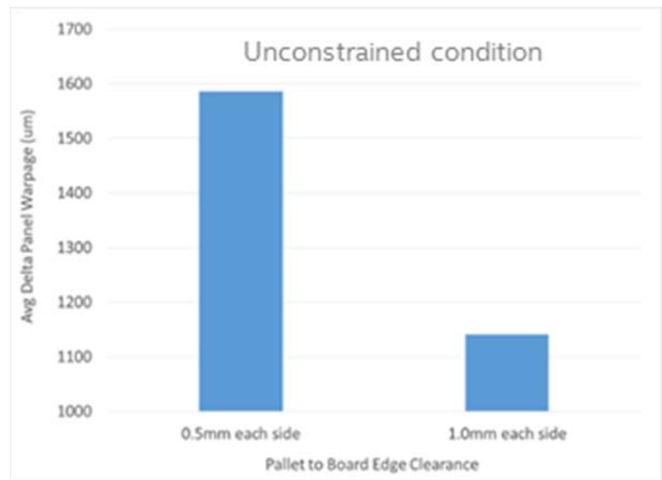


Figure 16. Impact of reflow pallet clearance to PCB warpage

Constraints

Minimizing constraints in reflow pallet design allows the PCB to expand freely which in turn helps to minimize PCB warpage in the reflow process. As highlighted in Figure 10, adding constraints that restrict the PCB movement (i.e., expansion) during reflow process increases PCB warpage. Low spring force end clamps are recommended to prevent the PCB edge lift off during the reflow process (Figure 17).

Figure 17. PCB edge lift off during reflow

If tooling pins are needed for the SMT component Pick-and-Place (PnP) process step, engage the tooling pins prior to PnP and then dis-engage the tooling pins prior to the reflow process step to minimize constraints. In this mechanism (Figure 18), pins will be engaged during the PnP process to provide the needed accuracy for placement machines and before reflow the pins will be retracted by turning the screw. Retracting the pins allows PCB expansion without any constraints and helps to minimize PCB warpage.

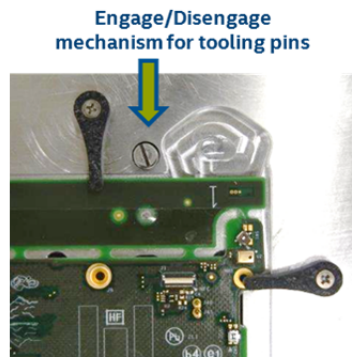


Figure 18. Tooling pin engage/disengage mechanism

Based on reflow pallet findings, the following pallet design recommendations have been found to reduce PCB warpage during SMT reflow:

- Minimize Delta Temp across PCB and Pallet (<20° C)
- Minimum clearance between PCB edge and Pallet edge for each side based on the thermal expansion equation
- If tooling pins are needed for PnP, engage/dis-engage the tooling pins at PnP and Reflow process steps to minimize constraints
- Use low spring force hold downs around the perimeter of the PCB to prevent PCB edge lift-off
- Provide support across the span of the pallet to prevent PCBs from sagging at temperature

The above reflow pallet design rules were used in multiple products and the results from the new pallet designs are summarized in the table below. Table 6 shows that the new pallet design guidelines reduced Room Temp, High Temp Panel, and BGA area warpage. The reduced board warpage resulted in a measurable improvement to the solder paste printing process and/or SMT yield.

Table 6. Case study results with SMT reflow pallet design guidelines

Product	Warpage: As Designed	Warpage: New pallet design rules	Impact to SMT Process
Product 'A' Tablet MB	HT Avg. Panel: 3250um HT Avg. BGA: 100um	HT Avg. Panel: 850um HT Avg. BGA: 50um	SEB
Product 'B' Phone MB	HT Avg. Panel: 3500um HT Avg. BGA: 53um	HT Avg. Panel: 1750um HT Avg. BGA: 41um	Improved SMT yield by 16%
Product 'C' Laptop MB	RT Avg. Panel: 4200um	RT Avg. Panel: 100um	Reduced print process volume variability → Improved SMT Yield
Product 'C' Laptop Daughter MB	RT Avg. Panel: 2100um	RT Avg. Panel: 1000um	Reduced print process volume variability → Improved SMT Yield

Vacuum Fixture

SMT solder paste print process is significantly impacted by PCB warpage. Constant contact between the PCB and stencil is needed to have a consistent print process. PCBs with warpage can create a gap between the PCB and Stencil. This excessive gap (i.e., poor gasketing) leads to wet bridging and excessive/insufficient solder paste release, as shown in Figure 19.

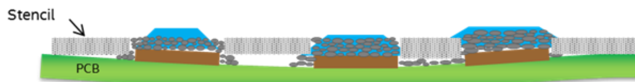


Figure 19. Gap between PCB and Stencil will lead to print defects

PCB support is critical for a consistent solder paste print process. The PCB support system is selected based on the PCB design as well as the warpage & process requirements, as shown in Figure 20.

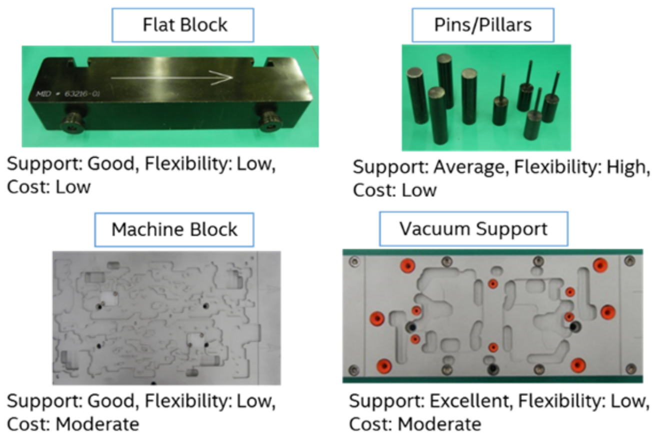


Figure 20. PCB support systems

Adequate board support is especially critical during the 2nd pass solder paste print for a double sided SMT process due to PCB warpage post 1st pass reflow. For PCB with warpage > 1000um, Vacuum fixtures provide custom support underneath the assembled PCB components with vacuum bellows to flatten PCB during the print process. Figure 21 shows that 3D vacuum fixture showed high panel warpage reduction when compared to machine block fixture (sample size of 15). Reduction in PCB warpage during the stencil print process in turn helps to have a consistent print process with minimal variation, as illustrated in Figure 22.

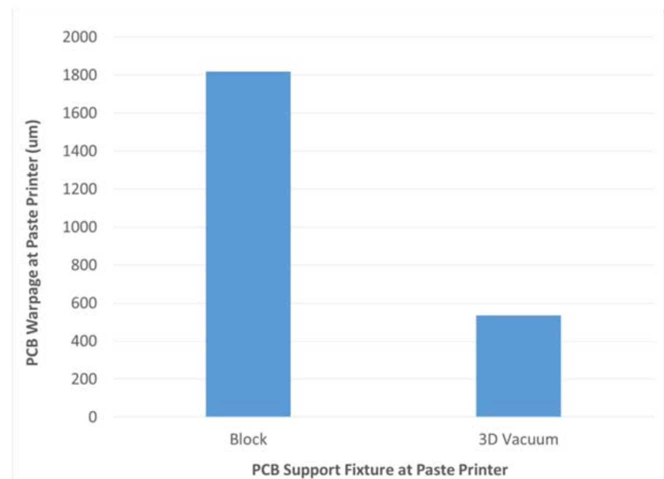


Figure 21. Vacuum Fixture impact to minimize PCB warpage

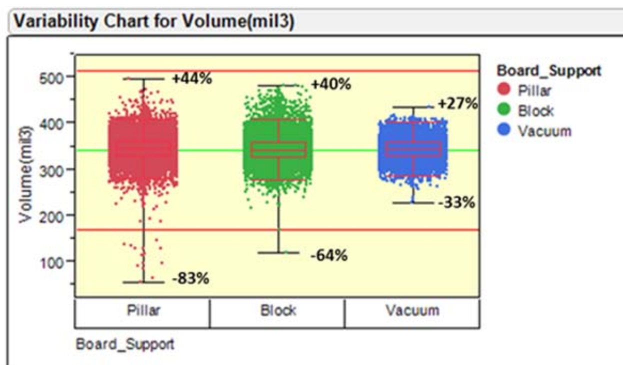


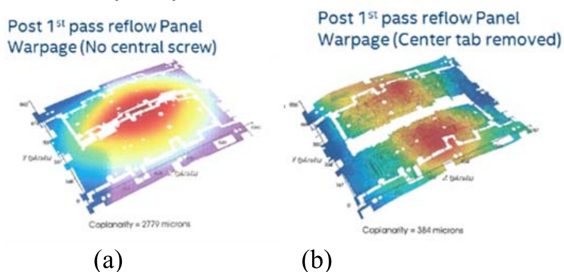
Figure 22. Impact of PCB warpage and PCB support to print process

For PCBs with warpage > 1000um, a vacuum fixture maximizes support for the print process and utilizes vacuum bellows to pull the board flat, improving print consistency.

Selective De-panel after 1st pass reflow

Another approach to address PCB warpage in the SMT assembly process is through the removal of a few selective router tabs post 1st pass reflow. This can remove constraints within the panel design to allow the PCB expand and not warp. This approach is applicable only to PCB designs with an outrigger and where excessive PCB warpage is observed post 1st pass reflow.

Figure 23 below shows the impact of selective de-panelization to PCB warpage. Post 1st pass reflow, the PCB exhibited warpage pf ~2700um (a) and the excessive warpage led to significant issues at the solder paste print process. To address the warpage, selective de-panelization was done through the removal of center tabs and this process reduced the PCB warpage to ~350um and enabled a successful print process.



(a) (b)

Figure 23. Selective de-panelization to address PCB warpage

CONTAINMENT

Another aspect to approach minimizing the PCB warpage in the board assembly process is to have metrologies that can screen and help reduce the opportunity of forming defects or defect escapees from the assembly process.

Solder Paste Volume Inspection with verified limits is an effective way to control paste volume and reduce the opportunity for opens, Head-on-Pillow (HoP), and solder bridge defects.

Non-destructive X-ray inspection will help identify SMT defects and minimize escapes (containment). Figure 24 shows a HoP defect identified using the non-destructive x-ray inspection.

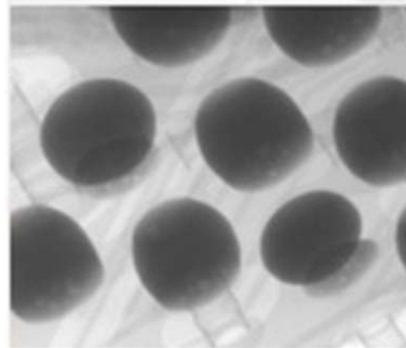


Figure 24. HoP defect identified using non-destructive x-ray inspection

CONCLUSIONS

This paper offers a deep dive into the understanding of PCB warpage and its impact on the assembly process. Implementation of the recommended design guidelines in PCB design/fabrication, reflow pallet design along with process control will help alleviate the issues that occur due to PCB warpage and will provide margin back to the board assembly process.

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