LEADLESS FLIP CHIP PLGA FOR NETWORKING APPLICATIONS

Andrew Mawer, Tara Assi, Steve Safai and Trent Uehling
NXP Semiconductors N.V.
Austin, TX, USA
andrew.mawer@nxp.com

ABSTRACT
Volumetric miniaturization of semiconductors and associated packaging is one of the largest driving forces within the industry. Initially motivated by the demand for smaller, more efficient and feature rich mobile electronics, this design trend has evolved and expanded across numerous applications. One example of a device designed to minimize size and maximize performance is the package that houses what is currently believed to be the world's smallest 64 bit microprocessor [1, 2]. The processor is designed for applications such as Internet of Things (IoT) gateways, portable entertainment platforms, high performance portable storage applications featuring mobile HDD and mobile storage for rechargeable devices. The package chosen for this processor is a molded plastic land grid array (PLGA) because the final mounted height is kept to a minimum while maintaining robustness and reliability requirements. The package itself is only 9.6 mm x 9.6 mm x 0.805 mm. This paper explores the packaging design, SMT assembly process, and board level reliability testing for this package. The results of these evaluations are discussed as well, including warpage versus reflow, board-level thermal cycling, JEDEC drop and IPC bend testing performance. All of the evaluations and testing performed to date indicates that the flip chip PLGA is a robust packaging solution that meets or exceed the requirements of its various intended applications.

Key words: Molded Flip Chip Plastic Land Grid Array, FC PLGA, drop testing, solder joint reliability, warpage at reflow, monotonic bend testing, Internet of Things, IoT

PACKAGE INTRODUCTION
The application focus for package miniaturization has expanded from consumer handheld devices to a variety of industries, including automotive, medical, military, aerospace, industrial communications, and high-volume networking/processing. Package design is shaped by the demand for greater I/O density while simultaneously decreasing IC size and weight. For application spaces like IoT, portable entertainment, and mobile storage, a traditional flip chip plastic ball grid array (FC PBGA) may not be the package of choice. These FC PBGAs, with body sizes typically ranging from 17 to 45+ mm and a relatively coarse pitches of 0.80 to 1.27 mm, may be too large for these applications. However, miniaturization of the FC PBGA can be accomplished by using a molded plastic land grid array (PLGA), where some minimal amount of solder is deposited on the LGA pads. The package itself is 9.6 mm × 9.6 mm × 0.805 mm, the scale of which can be seen in Figure 1.

Figure 1. 211 FC PLGA Topside Image with Thumbtack Shown for Relative Size Comparison.

The bottom of the PLGA package contains SnAgCu solder bumps on the land grid array pads, which can be seen in Figure 2. The overall design of the land grid array consists of two outer rows of rectangular pads at 0.5 mm pitch along each edge, as well as a 9 × 9 inner array and large corner pads at 0.8 mm pitch. The two outer rows were specifically designed to enable routing of all signals on the top layer of the application PCB using non-premium design rules. Also, rotating the inner array of square pads 45° allows for the use of larger diameter interstitial vias. The detailed attributes of the package are listed in Table 1. The die interconnect to the package is flip chip with Pb-free bumps, and can be seen in Figures 3 and 4. For additional robustness, the flip chip die backside is covered with mold compound that also serves as the underfill between the die and substrate. The substrate is a three copper (Cu) layer coreless type with a designed thickness of 0.18 mm.

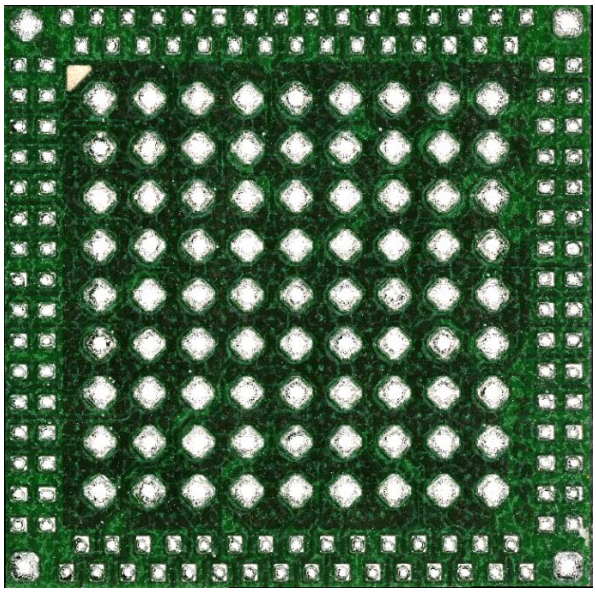

Figure 2. 211 FC PLGA Bottomside Image Showing Two Outer Rows of LGA Pads at 0.5 mm Pitch and 0.8 mm Pitch Inner 9 × 9 Array of LGA Pads.

Table 1. Detailed Listing of FC PLGA Package Attributes.

Item	Value	Comment
Package Body Size	9.6 × 9.6 mm	
Package Thickness	0.805 mm	With Solder
Joint Stand-Off Height after Board Mount	150 – 200 µm	Pad / Paste Dependent
Total LGA Pads	211	
Package LGA Pad Type	Soldermask Defined (SMD)	
LGA Pad Finish	100 +/- 50 µm SnAgCu Solder Bumps	
Total Perim LGA Pads	126	Two Rows
Total Center LGA Pads	81	9 × 9 Array
Total Corner LGA Pads	4	
Perim LGA Pad Pitch	0.5 mm	
Perim LGA Pad Size	0.22 × 0.26 mm	
Center LGA Pitch	0.8 mm	
Center LGA Pad Size	0.45 × 0.45 mm	
Substrate Cu Layers	3	Coreless
Substrate Thickness	0.18 mm	Including Soldermask
Mold Cap Thickness	0.53 mm	
Die Size	6.4×4.9×0.3 mm	Daisy-Chain Die
Product Power	~1 W	Typical

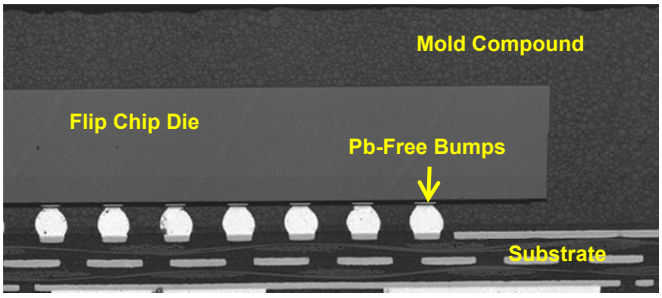

Figure 3. Cross-Section of FC PLGA Showing Mold Compound on Both Top and Bottom of the Die, Pb-Free Die Bumps and Three Copper Layer Laminate Substrate.

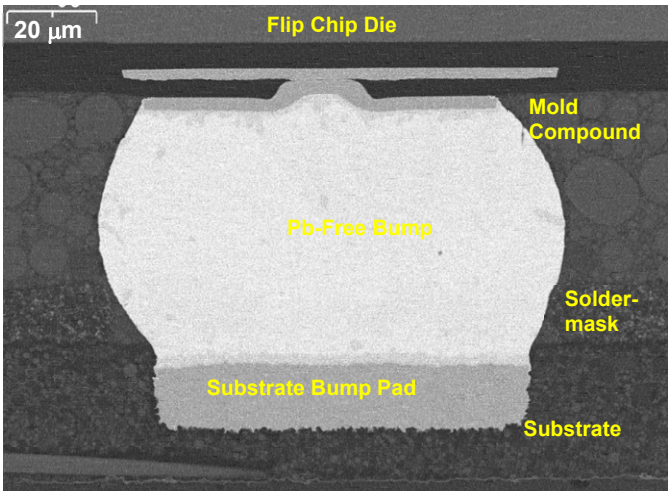

Figure 4. Higher Mag (800X) SEM Image of a Typical Pb-Free Bump on the FC PLGA.

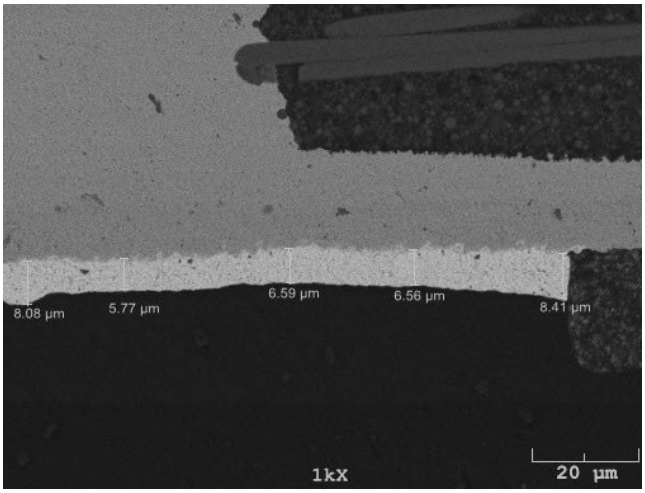

Figure 5. 1kX SEM Image of a Cross-Section of a Portion of LGA Pad with Before Additional Solder Was Applied to Pad.

Package LGA Pad Configuration

The initial configuration that was evaluated was a typical LGA with only minimal solder on the bottomside LGA pads. The purpose of this was to protect the Cu to ensure solderability of the pads, but not to add any appreciable solder volume to the resulting joint following SMT. This can be seen in Figure 5 where the solder thickness on the

LGA pad ranged from only 5.8 to 8.4 µm. As will be discussed later, for added robustness and SMT manufacturability, it was decided to pre-apply a larger volume of solder on the LGA pads through solder paste stencil printing as part of the package assembly process. The resulting LGA pad has an approximately 100 µm thick layer of solder on it. Figures 6 and 7 show this 100 µm thick solder bump optically from the side of the package and in cross-section, respectively. A typical test mark, commonly referred to as a witness mark, can be seen in the bump in Figure 7. Also visible in this cross-section is the fact that the FC PLGA substrate employed Cu filled microvia-in-pad on the LGA pads. This is necessitated by substrate routing density but also adds robustness to the pad in order to resist pad cratering during assembly, cycling, drop and bending. The soldermask defined LGA pads on the package also add to this robustness.

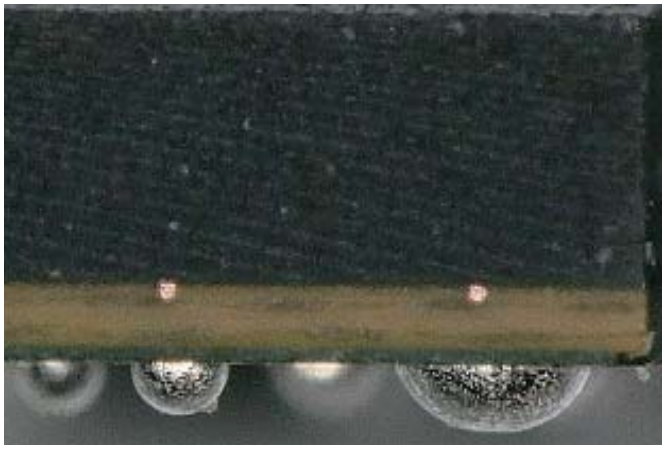

Figure 6. Optical Image Showing FC PLGA Substrate, Mold Compound and the 100 µm of Pre-Applied Solder Bumps on the LGA Pads.

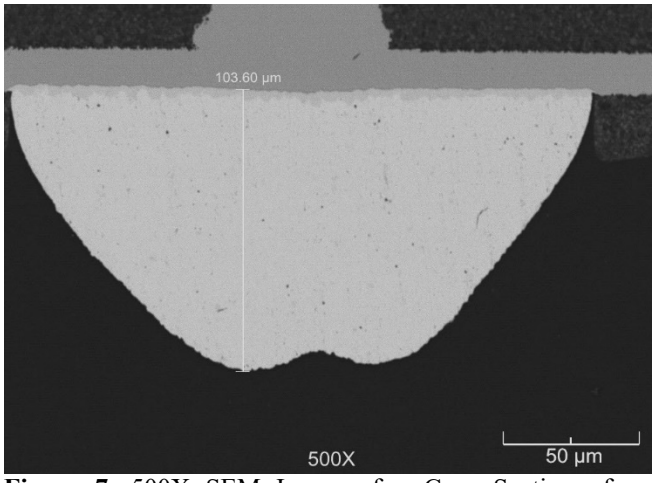

Figure 7. 500X SEM Image of a Cross-Section of an Approximately 100 µm SnAgCu Solder Bump on an Outer LGA Pad. Note the Bump Height Measurement of 103.60 µm and the Test Mark on the Bump.

PACKAGE REFLOW WARPAGE MEASUREMENTS

Since LGA packages have by definition lower solder volume then BGAs, they do not collapse as much during SMT assembly. Therefore, besides the stencil printing process ensuring consistent printed solder paste volumes at every site and controlled localized PCB warpage at the LGA footprint, a package with minimal warpage during reflow is critical. Using the TherMoiré technique, the bottomside warpage of five FC PLGAs with the solder removed from the LGA pads was characterized through a typical reflow profile. Warpage was measured at 15 points during the reflow cycle. Figures 8 and 9 show typical 3D plots of the bottomside warpage at both room temperature and 260°C peak reflow, respectively. The data on the five units is plotted in Figure 10 and tabulated in Table 2. No part had warpage over 40 µm at any time during the reflow cycle with the maximum warpage occurring at room temperature. Most importantly, warpage during the portion of the Pb-free profile where solder would be molten (>217°C) was <30 µm. The warpages measured meet industry standards and would indicate that there would not be any issues with joining during a typical reflow process with consistent solder paste volumes applied [3 - 5].

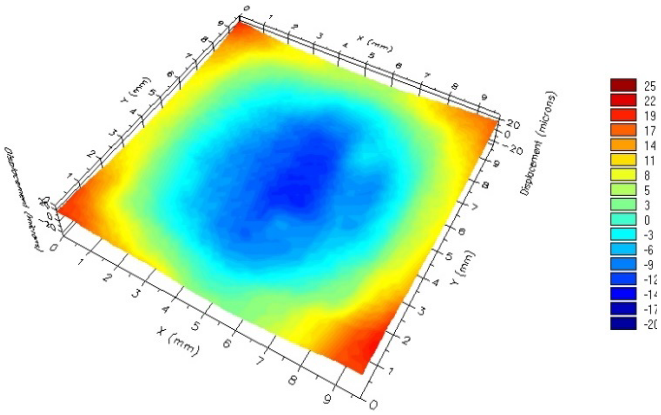

Figure 8. Typical 3D TherMoiré Plot of Bottomside FC PLGA Warpage of 34 µm at Room Temperature of 25°C.

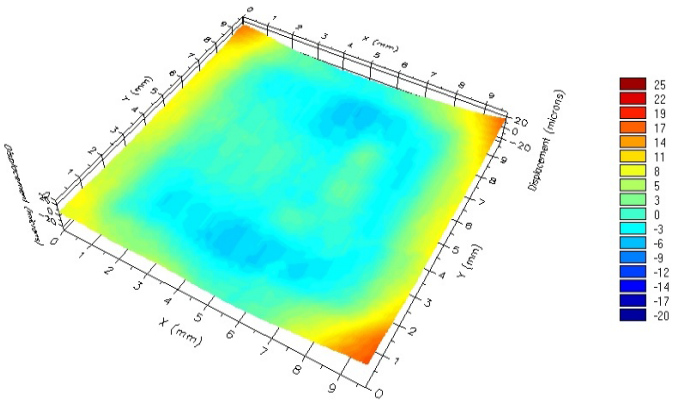

Figure 9. Typical 3D TherMoiré Plot of Bottomside FC PLGA Warpage of 23 µm at Peak 260°C Reflow.

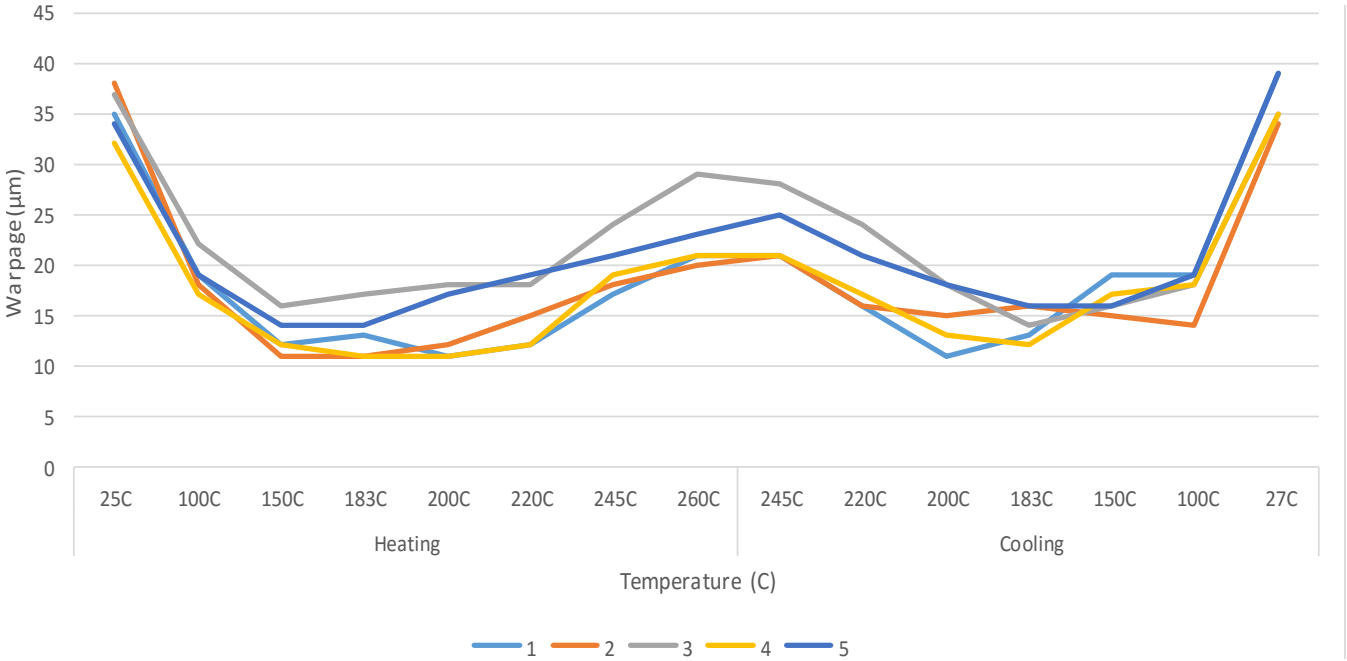

Figure 10. TherMoiré Warpage Plot on Five 211 FC PLGAs at 15 Temperatures During a 260°C Peak Reflow Profile.

Table 2. TherMoiré Warpage Data on Five 211 FC PLGAs at 15 Temperatures During a 260°C Peak Reflow Profile.

	TherMoire Read Points (microns)														
	Heating								Cooling						
Unit	25C	100C	150C	183C	200C	220C	245C	260C	245C	220C	200C	183C	150C	100C	27C
1	35	19	12	13	11	12	17	21	21	16	11	13	19	19	39
2	38	18	11	11	12	15	18	20	21	16	15	16	15	14	34
3	37	22	16	17	18	18	24	29	28	24	18	14	16	18	35
4	32	17	12	11	11	12	19	21	21	17	13	12	17	18	35
5	34	19	14	14	17	19	21	23	25	21	18	16	16	19	39

PCB AND SMT ASSEMBLY PROCESS

Daisy-Chain Design

A daisy-chain test vehicle version of the product package was designed for SMT assembly and board-level reliability studies. The daisy-chain substrate started with the product substrate routing in order to replicate the copper density as much as possible. A special daisy-chain flip chip die was also designed so that both the LGA joints and die to substrate bumps could be assessed. The associated daisy-chain PCB was designed such that there were a total of four nets monitored on each part: 1) two perimeter LGA rows, 2) 9 × 9 center LGA array, 3) 225 µm pitch die bumps and 4) 250 µm pitch die bumps. A schematic of the package daisy-chain routing is shown overlaid with the PCB routing in Figure 11.

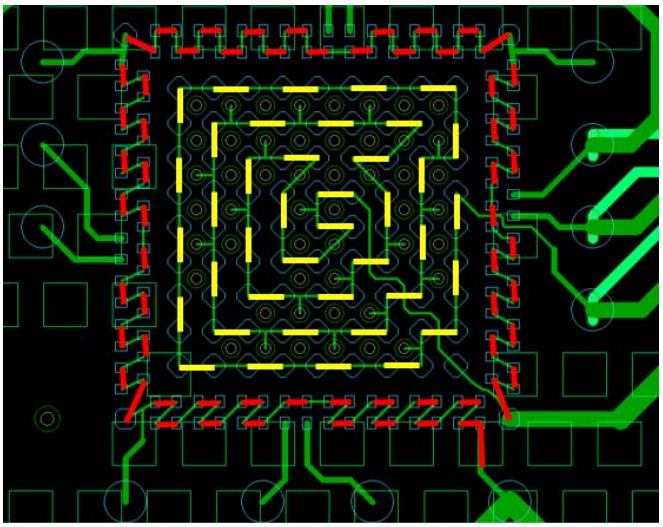

Figure 11. Top Down View of 211 FC PLGA Daisy-Chain Routing with the PCB (Green) and Package (Red and Yellow) Nets Both Shown. I/O's Not Included in the LGA Daisy-Chain Were Assigned to Monitor the Bump Connections.

PCB Construction

Two PCBs were designed, one for thermal cycling per IPC-9701A and one for drop testing per JEDEC JESD22-B111

[6, 7]. Since it could accommodate the dimensional and constructional requirements, the thermal cycling PCB was also able to be used for bend testing per IPC-9702 [8]. These PCBs, which are pictured in Figures 12 (thermal cycling/bend) and 13 (drop), were both 1.57 mm thick, eight layers and constructed of a high Tg FR4 material. Note that even though the JEDEC standard for drop allows up to 15 parts to be populated on the PCB, the drop test PCB was designed with only five footprints per side in an "X" pattern in the middle. Those five locations are thought to give the most consistent results. For both PCB types, layers one and eight were used for daisy-chain routing, layers two and seven had 1.0 x 1.0 mm copper squares at 1.60 mm pitch for 40% copper coverage and layers three through six had 1.0 mm copper squares at 1.20 mm pitch for 70% copper coverage. The surface finish for both PCBs was an Organic Solderability Protectant (OSP). Dummy thru-hole vias were placed interstitially in the center 9 × 9 array to mechanically mimic an actual application PCB. These vias were epoxy filled and plated over in order to prevent any solder from wetting down them during assembly.

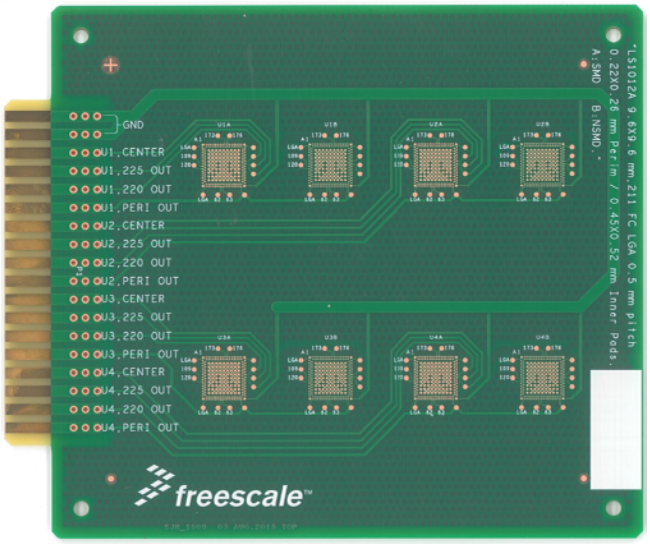

Figure 12. Unpopulated Thermal Cycling Test Board. Note the Hard Gold Plated Edge Fingers on the Left Side Are for Continuous, In-Situ Monitoring in the Chamber. This PCB Was Also Used for Bend Testing.

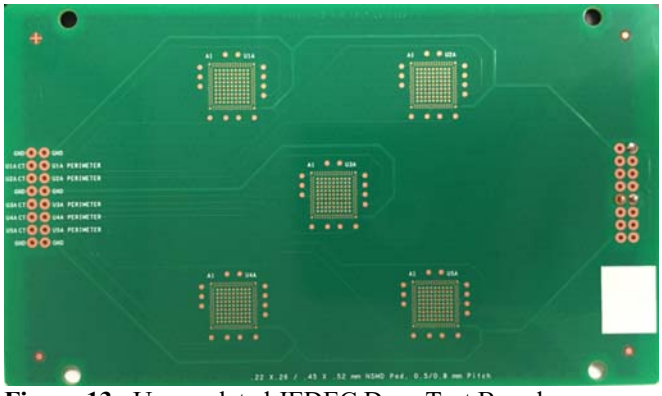

Figure 13. Unpopulated JEDEC Drop Test Board.

PCB Pad Types

The daisy-chain test board was designed with both soldermask defined (SMD) and copper defined or non-soldermask defined (NSMD) pads. The different pad types were put on opposite sides of the PCB so that either could be used. The pads were all designed to be 1:1 with the package LGA pads. Refer back to Table 1 for those package LGA dimensions. The NSMD and SMD pads are shown in Figures 13 and 14, respectively. NSMD PCB pads are generally recommended for most applications [9]. They can provide the best solderability including solder typically completely wetting down the sides of the pad for additional strength. However, NSMD pads may result in lower performance in drop and bend testing in cases where NSMD pads ripping out of the PCB or cratering is the limiting factor. SMD pads have greater strength in this regard, but have been shown to be a higher stress pad in thermal cycling due to the stress concentration point at the edge of the solder joint.

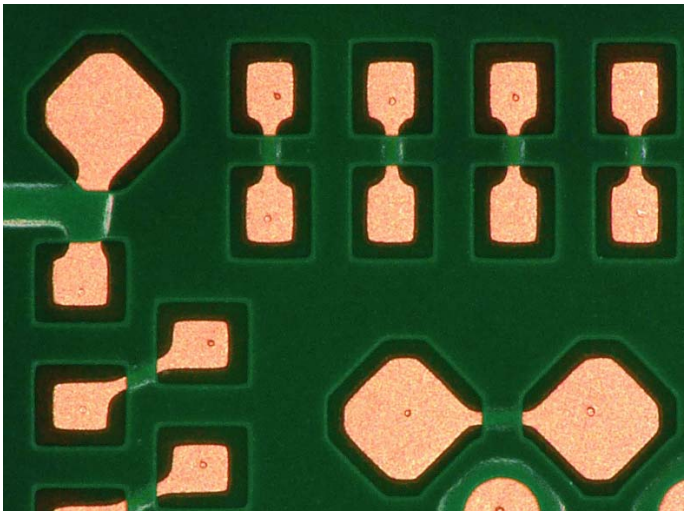

Figure 14. A Portion of the Daisy-Chain Footprint that Uses NSMD Pads with a 50 µm Soldermask Clearance Around the Copper Pads. Marks Visible on Pads are from PCB Test.

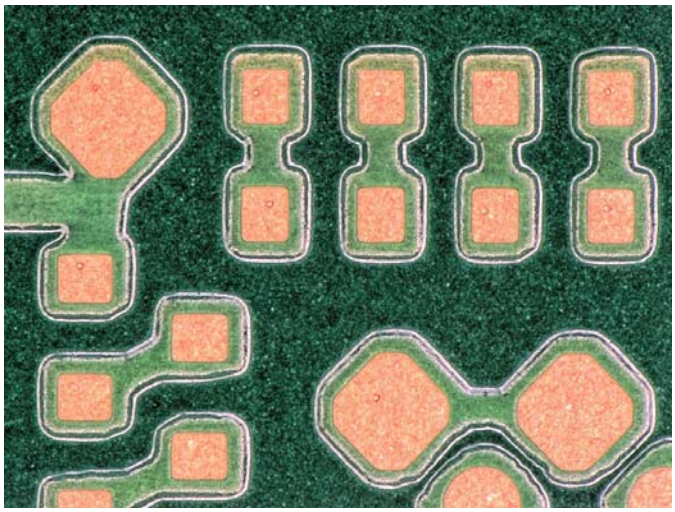

Figure 15. A Portion of the Daisy-Chain Footprint that Uses SMD Pads with a 50 µm Soldermask Overlap of the Copper Pads.

Reflow, Solder Paste and Stencil Configuration

Fresh jars of no-clean, halide free, SAC305 ROL0 solder paste with Type IV (28 – 40 µm diameter) solder powder were used for all SMT assembly. Reflow was done in a ten heating/three cooling zone belt convection reflow oven with an air atmosphere and a peak reflow temperature of 240°C. Laser cut, nickel plated, electropolished and nanocoated 100 µm thick stencils were used for SMT assembly of the LGA [10, 11]. Initially, a stencil with apertures that were 1:1 with all the PCBs pads was used. With these 1:1 ratio apertures, some stencil printing inconsistency issues were observed on the 0.5 mm pitch perimeter pads. This in combination with the initial LGA units that contained minimal solder on the LGA package pads (refer back to Figure 5), resulted in relatively low solder joint stand-off and some instances of time zero opens (See Figure 16 for example). Therefore, it was decided to make two improvements to increase SMT assembly robustness. The first one was to make the stencil aperture openings for the 0.5 mm pitch perimeter pads have a 1.61:1 ratio to the solderable pad. This is pictured in Figure 17 and a typical resulting solder print is shown in Figure 18. The second improvement was to increase the pre-applied solder volume on all the LGA pads to approximate 100 µm thickness as was shown previously in Figure 7.

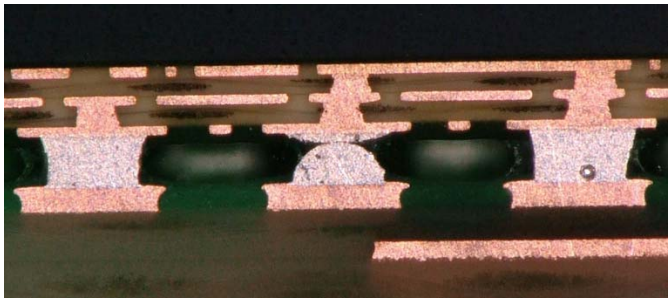

Figure 16. Low Solder Paste Volume Induced Open on the Perimeter Row of LGA Joints Encountered When Using Stencil Apertures that Were 1:1 with the Pads and a Package with Minimal Solder Pre-Applied to the LGA Pads.

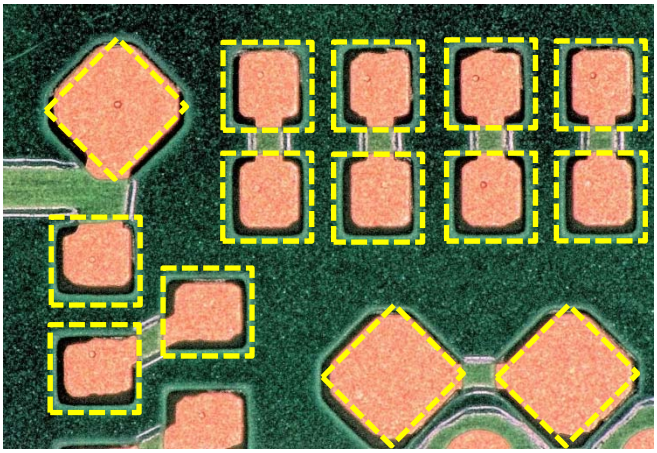

Figure 17. The SMD PCB Footprint Shown Overlaid with an Improved Stencil Design in Dashed Yellow Lines Where the Perimeter Pads had Aperture Openings with a 1.61:1 Ratio to the Pads. This Allowed for a Theoretical 60% Overprint on Those Pads.

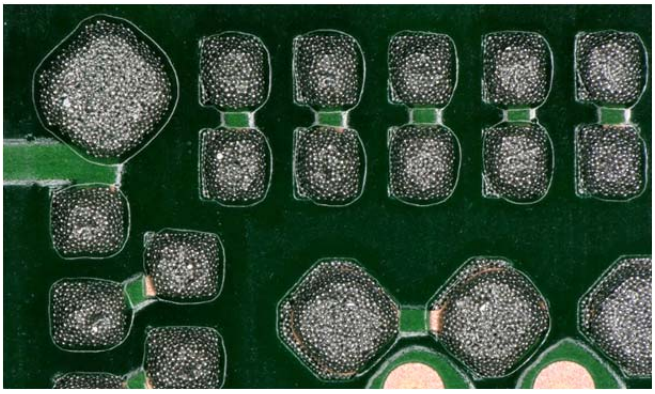

Figure 18. Solder Paste from a Typical Stencil Print Using Improved Stencil with Openings with a 1.61:1 Ratio on the 0.5 mm Pitch Perimeter Pads Only.

Using the new 1.61:1 ratio stencil and components with the 100 µm thickness of pre-applied solder, a total of 105 FC PLGAs were assembled to test boards for various board-level stressing with 100% assembly yield. The quantities assembled for each test are listed in Table 3. All the PCBs were 100% X-rayed for solder joint shorts. A typical X-ray image is shown in Figure 19.

Table 3. Quantities of 100 µm Thick Pre-Applied Solder FC PLGAs Assembled for Various Board-Level Tests.

Board-Level Test Type	NSMD Pads	SMD Pads
IPC Thermal Cycling	12 and 32*	12
IPC Monotonic Bend**	14	15
JEDEC 1500 Gs Drop	10	10

*Notes: *Quantity of 32 was a follow-on, confirmation build. **Thermal cycling test board was also adapted for bend testing.*

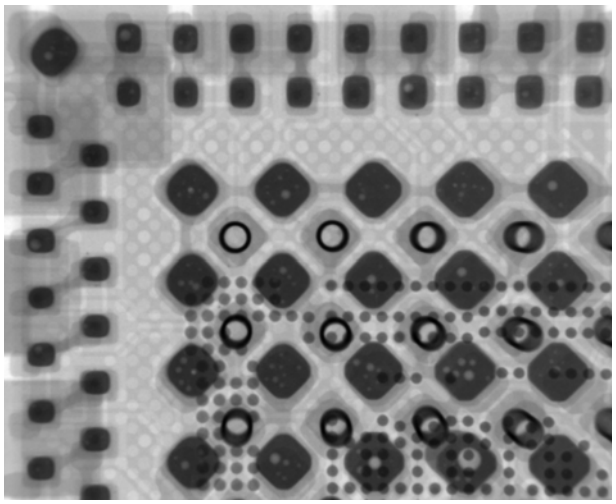

Figure 19. Typical X-ray Image Following SMT Assembly Showing Consistent LGA Solder Joints from the 1.61:1 Area Ratio Stencil Apertures. Note the Typical Solder Joint Voiding and the Flip Chip Die Bumps.

BOARD LEVEL RELIABILITY TESTING

Single Chamber Thermal Cycling

Initially, twelve components each were assembled to SMD and NSMD PCB pads on the thermal cycling test boards. The boards were placed into –40 to 125°C single chamber cycling with 15 min controlled linear ramps and 15 min dwells. The resulting ramp rate was 11°C/min. Continuity was continuously monitored using Anatech STD256 event detectors. The event detectors were set to record failures at 300Ω resistance and can detect events that are as short as 200 nanoseconds. Each part was monitored in-situ using four separate nets: 1) perimeter LGA joints including corners, 2) center LGA joints, 3) 225 µm pitch die bumps and 4) 250 µm pitch die bumps. Cycling continued until 100% of the parts had failed. At the conclusion of the test, no center LGA or bump net fails had been recorded, only perimeter net fails. Failure analysis was carried out on both SMD and NSMD PCBs pad types. The SMD pad parts were seen to exhibit solder fracturing predominately at the PCB pads (Figure 20) while the NSMD pad pads had fracturing predominately at the package (Figure 21). Even though the SMD pads resulted in greater solder joint stand-off, the NSMD pads had almost 2× greater cycles to first failure and 30% longer Weibull characteristic life (eta). A confirmation assembly build with a larger sample size of 32 parts was carried out using the NSMD PCB pads only. The failure data from this build, the results of which replicated the initial NSMD data, is plotted in Figure 22 along with data from the initial build.

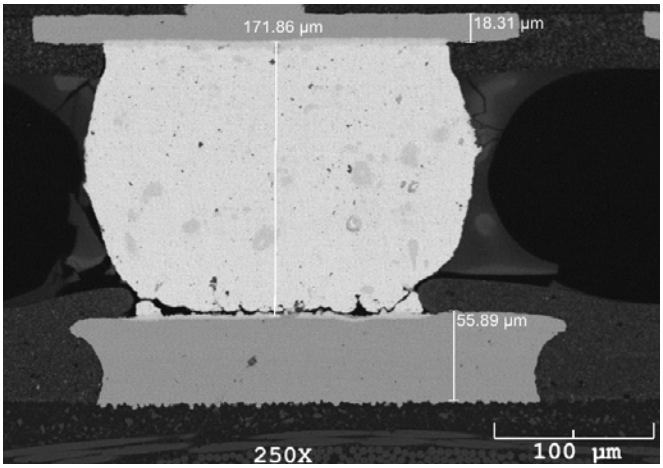

Figure 20. Cross-Section of a Typical Failing SMD PCB Joint. Note Fracturing Predominantly Near PCB Pad.

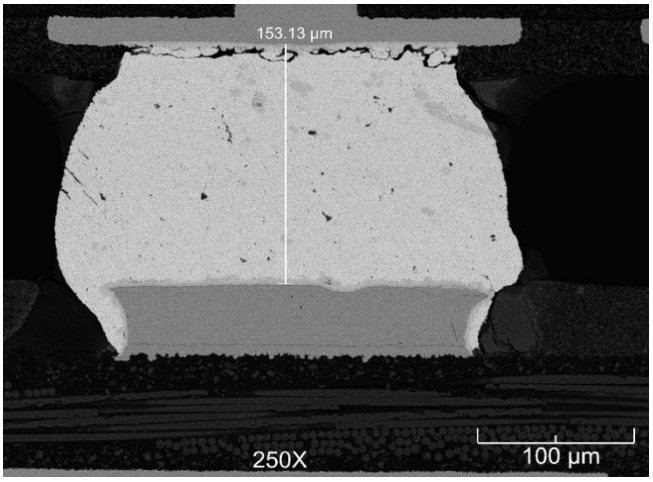

Figure 21. Cross-Section of a Typical Failing NSMD PCB Joint. Note Fracturing Predominantly at Package Interface.

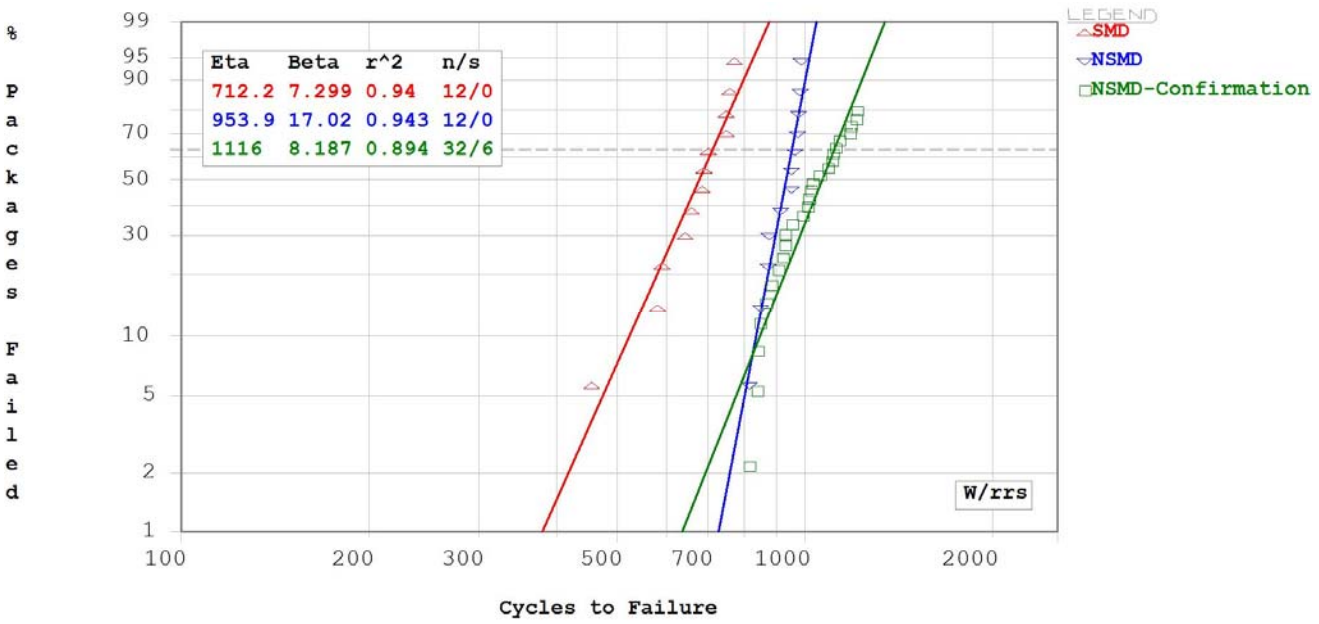

Figure 22. Two Parameter Weibull Plot of the -40 to 125°C Thermal Cycling Failures for SMD and NSMD PCB Pads.

Monotonic Bend Testing

Fourteen and 15 parts mounted to NSMD and SMD PCB footprints, respectively, were subjected to four point monotonic bend testing per IPC/JEDEC-9702. The testing employed a minor or load span of 44 mm and a major or support span of 76 mm. The set-up is shown in Figure 23. Continuous electrical monitoring was performed with an applied strain rate of 5,000 µstrain/sec on a uniaxial strain gauge adhered to the PCB approximately halfway between the package edge and the nearest load roller. Testing continued up to a -1,332 N load which resulted in a maximum strain of 13,000 µstrain with no electrical failures recorded on any of the 29 samples at that point. A plot of all the relevant variables during a typical test is shown in Figure 24.

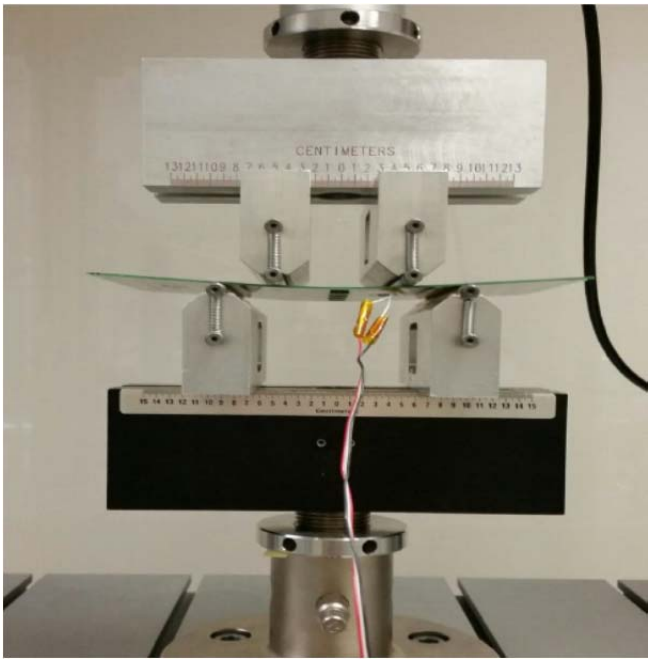

Figure 23. Four Point Monotonic Bend Test Configuration.

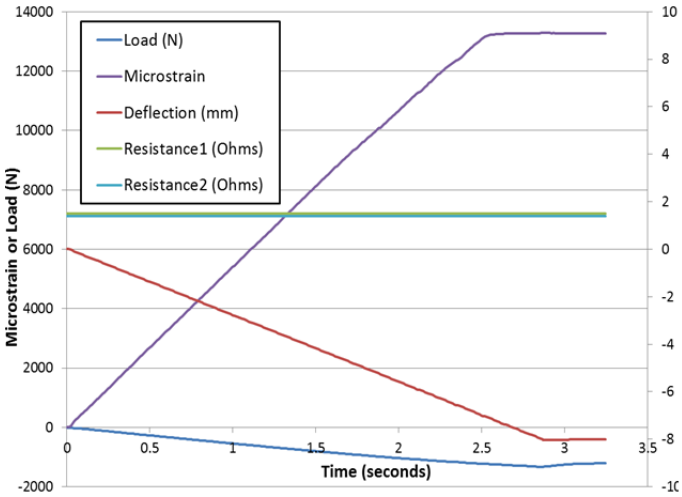

Figure 24. Plot of Microstrain, Load, Deflection and Electrical Resistance Versus Time During Bend Testing. The Load, and Therefore Deflection and Microstrain, Maxed Out Around 13,000 µstrain with No Failures Recorded.

Drop Testing

Even though a five-up board with the footprints in an "X" pattern was designed for JEDEC drop testing, for better consistency only the center position was populated on each PCB which is allowed in the standard. Ten boards of each footprint type (SMD and NSMD) were subjected to JEDEC Condition B of 1,500g drop with a 0.5 ms duration, half-sine pulse. Drop test was always performed with the LGA component under test on the bottomside of the PCB. Dropping from an average height of 52 cm was required to attain the 1500 Gs. The shock tower set-up is shown in Figure 25. No electrical failures were recorded within the JEDEC required 30 drops and testing was halted at that point. Using a rectangular rosette strain gauge, PCB strain was characterized during drop testing set-up and found to be up to approximately 1,300 µstrain max during the 1500 Gs drop.

Figure 25. Shock Tower with Two Attached PCBs Used for Electrically Monitored JEDEC Drop Testing to 1500 Gs.

CONCLUSIONS

During the various aspects of package and surface mount process development and associated board-level reliability testing for a novel, miniaturized 211 pin FC PLGA for high performance networking and IoT applications, the following conclusions were drawn:

- Excellent SMT assembly yields were achieved with the combination of overprinting (1.61:1 aperture to pad ratio) solder paste on the 0.5 mm pitch perimeter LGA pads only and the addition of approximately 100 µm of pre-applied solder to all the LGA package pads. The resulting joint was a compromise between traditional BGAs and LGAs.
- The component displays <40 µm bottomside flatness both at room temperature and throughout the entire reflow which is more than 2× better performance than any current, known industry standards.
- Board-level thermal cycling performance met the projected requirements for intended applications with first failure in –40 to 125°C cycling at greater than 800 cycles with NSMD and greater than 400 cycles with SMD PCB pads. Solder joint fatigue fractures with the SMD PCB

pads were predominantly at the PCB pad interface. The opposite was true for the recommended NSMD PCB pads.

- The fact that the die shadow was completely over the coarser pitch (0.8 mm) center array of LGA joints possibly helps to explain the good thermal cycling performance.
- The small body size along with the larger corner pads were believed to be part of the reason for the excellent performance in 1500 Gs JEDEC drop and 13,000 μstrain IPC monotonic bend with no failures recorded in either test with either SMD or NSMD PCB pads.
- Nets for monitoring the integrity of the die to substrate interconnect were included in the daisy-chain test vehicle. Vias and traces in the substrate were also included in this net. No failures were recorded on these nets in any of the testing performed indicating a very robust connection within the component.

ACKNOWLEDGEMENTS

The authors would like to thank Paul Galles for performing SMT assembly, TherMoiré and carrying out thermal cycling, drop and bend testing. Also, thanks to Alvin Youngblood for assistance with the test board design and for performing failure analysis. Special thanks to Michael Zimin and George Leal for the original concept and design of the package configuration. Lastly, thanks to Kevin Hussey, Kelly Folts and Franklin Utama for ongoing management support of these development activities.

REFERENCES

1) J. Lipsky, “NXP Processor Powers IoT, Networks”, www.eetimes.com, Feb. 22, 2016.

2) LS1012A Announcement on www.nxp.com, http://media.nxp.com/phoenix.zhtml?c=254228&p=irol-newsArticle&ID=2141376.

3) JEITA ED-7306, “Measurement Methods of Package Warpage at Elevated Temperature and the Maximum Permissible Warpage”, Standard of Japan Electronics and Information Technology Industries Association, March 2007.

4) IEC 60191-6-19, “Mechanical standardization of semiconductor devices – Part 6-19: Measurement methods of the package warpage at elevated temperature and the maximum permissible warpage, Edition 1.0, Feb., 2010.5)

5) JEDEC SPP-024A, “Standard Practices and Procedures - Reflow Flatness Requirements for Ball Grid Array Packages”, March 2009.

6) IPC-9701A, “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments”, Feb. 2006.

7) JEDEC JESD22-B111, “Board Level Drop Test Method of Components for Handheld Electronic Products”, July 2003.

8) IPC/JEDEC-9702, “Monotonic Bend Characterization of Board-Level Interconnects”, June 2004.

9) AN2265, “Assembly Guidelines for Land Grid Array (LGA) Package”, Rev. 1.0, July 2015.

11) M. Rösch et al, “Characteristics and Potentials of Nanocoated Stencils for Stencil Printing Optimization”, 2010 SMTA International.

12) E. Moen, “Nano Coated Stencils for Optimized Solder Paste Printing”, Proceedings of Toronto SMTA Expo and Technical Forum, May 2012.