INFLUENCE OF PCB SURFACE FEATURES ON BGA ASSEMBLY YIELD

Satyajit Walwadkar, Todd Harris, Bite Zhou, Aditya Vaidya, Juan Landeros, Alan McAllister
Intel Corporation
Hillsboro, OR, USA
satyajit.s.walwadkar@intel.com

ABSTRACT
Demand for higher performance products in thinner and lighter form factors has driven a trend towards thinner ball grid array (BGA) packages with higher pin counts at a reduced pitch. As solder ball density increases and solder ball dimensions decrease, manufacturing yield during surface mount assembly has become increasingly sensitive to the surface topography of the printed circuit board (PCB). Irregularities in the local surface topography are introduced by the uneven distribution of copper on the outer layers of the PCB due to copper plane layout, trace routing, via placement and BGA pad definitions. The conformal solder mask coating used to insulate these copper features and define pad dimensions can result in significant variation in board thickness and surface feature dimensions. This paper provides insight into the impact of these irregularities on BGA package surface mount yield, and provide guidance on design and manufacturing practices to limit their impact.

Key words: SMT, FCBGA, PCB, DIC, Copper plane, Laser confocal Microscopy

INTRODUCTION
Semiconductor chips have to be packaged and assembled onto a system level printed circuit board (PCB) to form a complete electronic product. With Moore's law playing a significant role, advanced packaging with increased I/O counts has become a necessity [1]-[3]. In order to cope with the increase in performance requirements, tighter pitches are required on PCBs in the component region posing both design and manufacturability challenges.

The PCB designer is faced with complex challenges to design a platform for lowest total cost while meeting aggressive performance requirements. The overall design process must take into account critical functional and signal timing requirements as well as complex power delivery schemes, all the while working within PCB technology boundaries. Key PCB features that drive cost include, but not limited to, PCB technology type, layer count, PCB dimensions, minimum PCB design rules, and materials specifications.

A PCB is a composite of organic and inorganic materials with external and internal wiring allowing electronic components to be electrically interconnected and mechanically supported. In addition, a PCB provides power to the components and conducts heat when necessary [1]. PCBs are largely made of epoxy glass based composite materials, constructed on multiple plies of epoxy –resin impregnated onto a woven glass cloth. They typically vary in thickness from less than 0.1mm to several millimeters depending on the application.

Fabrication of a typical multi-layer PCB involves following major process sequence: First the panels with inner conductive layers are produced by simple double sided etching from the copper clad prepreg laminates; then these etched panels, adhesive pre-pregs and un-etched outer panels are laminated pressed and cured to get a rigid PCB. Finally, the PCB is subjected a sequence of process steps corresponding to pattern or panel plating of double sided PCB [4].

With requirements of finer and finer PCB assembly interconnection geometries, a solder resist mask or solder mask is required to be deposited over all the parts of the PCB except where the solder joints are to be made. A solder resist is a heat-resisting coating material applied to selected areas of the PCB to prevent the deposition of solder upon those areas during subsequent soldering and in particular to prevent solder bridging between the conductive tracks. The functions of the solder mask also include the control of outer layer impedance, minimizing handling damage during assembly and increasing corrosion and flammability resistance besides providing aesthetic look to the PCB [5].

Solder mask comes in different media depending on the application demands. The lowest-cost solder mask is an epoxy liquid that is pattern printed through the screen onto the PCB. Other types are the liquid photo-imageable solder mask (LPSM) inks and dry film photo-imageable solder mask (DPSM). Screen printing application process provides a ~25-50um thick solder mask over most of the PCB with thickness between the tracks reaching up to 80-100um. LPSM can be either screen printed or sprayed on the PCB. Spray coating process provides ~50-75um over most of the PCB with a much better control of thickness between the tracks than the screen printing process as shown in Figure.1. Post application, the solder mask is exposed to the pattern and developed to provide openings in the pattern for parts to be soldered to the copper pads. All three application processes go through a thermal cure of some type to drive off the solvent after the pattern is defined [5]-[7].

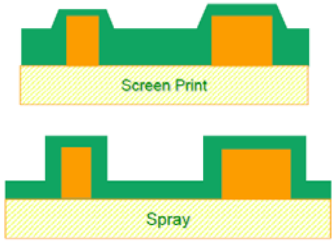


Figure 1. Screen print vs Spray coating track coverage on copper features

The impact of some of the PCB surface features discussed in this paper originates from the fact that solder mask coverage is inconsistent between a copper clad vs non-copper clad area. This non-uniformity in solder mask coating typically arises during solder mask application process and could potentially impact the BGA assembly yield as the BGA pitches become finer. This paper introduces some of the PCB surface features typically observed on PCBs for cavity and full grid array Flip Chip BGA (FCBGA) footprints. This is followed by SMT yield data, failure analysis observations, and a detailed discussion on how these surface features could potentially interfere during SMT through simple lab experiments. Finally, summary of findings are provided based on observations towards the end. Recommendations provided in this paper will help to better design PCBs by taking into account PCB surface features to avoid product SMT yield margin loss.

TYPICAL PRODUCT PCB SURFACE FEATURES

PCB designers are driven to reduce layer counts. Addition of layers drives cost in material use, increases lamination cycle processes, as well as reduces overall yield. Reduced design times and aggressive time to market schedules require designers to implement best known practices to reduce design risk. This drives effective and efficient use of all useable layers. Large planes are integrated to optimize power delivery while routing layers are used to provide optimized signal integrity.

The circuit connection and integration of a typical BGA package typically considers system connectivity, power delivery, voltage drop, noise, impedance, cross-talk, skew, and shielding. Connections can be categorized into signals, ground, and power. Signals tend to be isolated from adjacent pads and follow a direct and controlled path to its intended destination. Power and ground typically are networked within the BGA package to improve overall power delivery as shown in Figure 2.

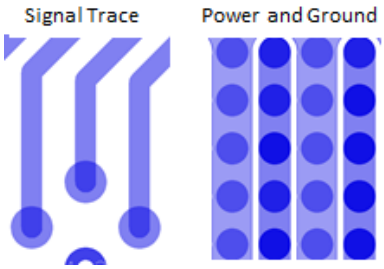
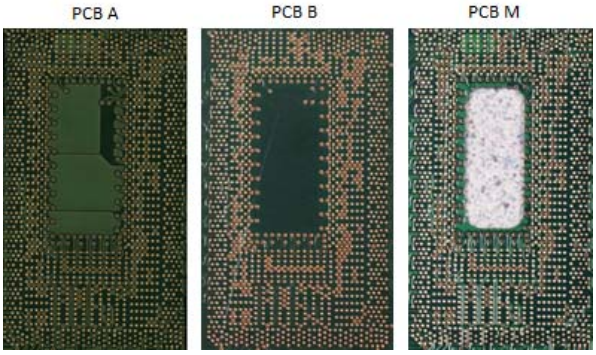


Figure 2. Schematic showing signal trace vs power and ground connection

The integration of a BGA into a board design is typically managed through pads, traces, shapes, and multi-layer interconnect vias. The electrical connections are covered by solder mask to prevent assembly shorting. Several connections supported by layer transition vias are routed on internal or backside layers, thus masking their presence within the internals of the PCB design. However, those features present on the same layer that the device is placed may have an influence on SMT assembly. Component BGA packages may have depopulated land arrays near their centers to support component placements. Board manufacturers are requested in those areas to ensure features at the board level will not interfere or potentially short to those components. Plated through hole plugging and capping is often implemented in those areas to prevent component BGA shorting to board features. The additional processing steps often result in an increased thickness locally to the plated through hole locations.

Two basic type of land patterns are typically used on surface mount devices. NSMD (non-solder mask defined) where solder mask opening is larger than the metal pads and SMD (solder mask defined) where the solder mask opening is smaller than the metal pads. Improved manufacturing process control and reliability favors NSMD over SMD [8], however in reality component layout has a combination of both NSMD and SMD pads to balance out power delivery and I/O requirements. In addition, some of the high performance computing applications require a cavity BGA type of layout in PCB where a copper plane is present in the cavity region to reduce the current loop inductance. Having a mix pad layout pattern along with presence of copper features in the BGA footprint creates further challenges in terms of achieving solder mask print uniformity during PCB manufacturing step. In order to gain understanding of impact from these solder mask topographic non-uniformities, few product PCB configurations with cavity array FCBGA and full array FCBGA footprints as shown in Figure 3 along with description in Table 1 were selected for the study.

a)



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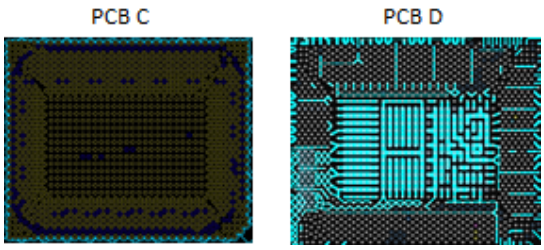


Figure 3. a) Product cavity array FCBGA PCB layout with presence and absence of copper plane in the center b) Product full array FCBGA PCB layout with symmetric and a-symmetric land pattern design.

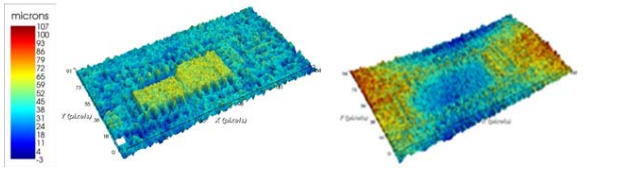
Table 1. PCBs used for surface feature impact study

S/N	PCB	BGA Pattern - Pitch	Comments
1	PCB A 32mil thick	Cavity Array – 0.65 mm	With Cu plane in center cavity
2	PCB B 32mil thick	Cavity Array – 0.65 mm	Without Cu plane in center cavity
3	* PCB M 32mil thick	Full Array – 0.65 mm	Center Cu plane cavity routed out
4	PCB C 28mil thick	Full Array – 0. 4/0.5 mm	SMD pads on single flood plane
5	PCB D 28mil thick	Full Array – 0. 4/0.5mm	SMD pads connected with traces

* PCB M with routed center cavity was extreme variant of PCB A design and was used for study purposes in limited cases only

PCBs under different categories were measured and Figure 4a. shows room temperature topography for a cavity array FCBGA pattern on PCB A and PCB B. With presence of copper, the center cavity region is raised up whereas in absence of copper, the cavity region sits below the surrounding BGA pad region. To decouple the PCB warpage aspect, accurate center cavity region height measurements were made with respect to the copper pads using a confocal laser microscope as shown in Figure 4b. Center cavity region profile showed a step-up height of ~35-40 microns for PCB A whereas PCB B cavity measurements showed step-down height of ~7 microns. Cross section measurements through the center cavity region on PCB A confirmed that the printed solder mask was thicker in the center cavity region than surrounding BGA region with the copper plane remaining at the same height as surrounding BGA pads as shown in Figure 4c.

a)



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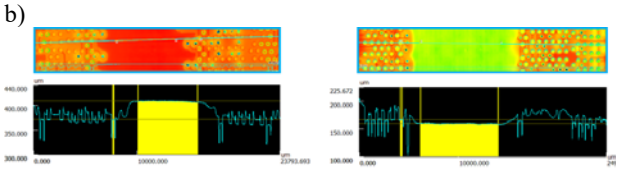

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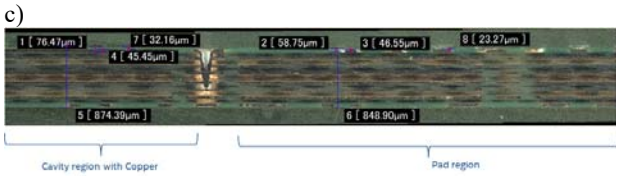
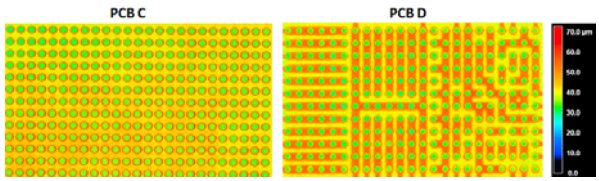


Figure 4. a) Contours for PCB A with copper plane in center cavity and PCB B without cavity copper plane b) Laser confocal microscope height profile measurements on PCB A and PCB B c) Center cavity copper plane cross-section of PCB A

Similar height profile measurements were also done on full array FCBGA footprints in the center die shadow region on a symmetric layout due to SMD pads on single copper flood plane on PCB C and asymmetric layout due to SMD pads connected to each other by copper traces on PCB D. This is shown in Figure 5a. PCB C showed a stepped-up and more uniform solder resist between the pads whereas PCB D showed stepped-up with a cavity in between the solder resist orthogonal to the copper traces. The solder resist along the copper traces was flat and more uniform. The difference in solder resist heights parallel and perpendicular to the copper traces on PCB D was estimated to be in the range of ~15-20 microns as shown in Figure 5b.

The impact of the surface mount process of these PCB surface topology differences between cavity and full array BGA footprints is discussed in next section.

a)



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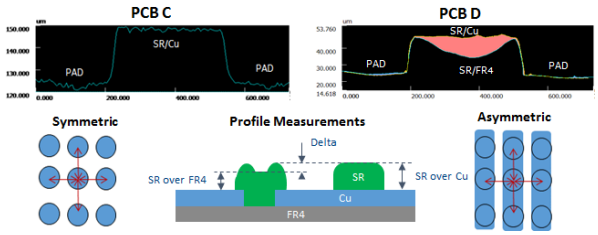


Figure 5. a) Profile measurements across the SMD pads showing solder resist profile differences b) Schematic showing differences in symmetric and asymmetric pad layout pattern

SMT YIELDS ON PRODUCT PCB

Increased ball density of the packages and thinner package substrates made it challenging to arrive at stable and capable SMT process for both types of FCBGA packages used in this study. SMT processes for all the legs of the experiment were carried out in air environment using a ramp reflow profile. Table 2 shows some of the key reflow process parameters used in this study.

Table 2. Reflow process parameters used for SMT builds

Process Parameters	Values
Max Ramp Slope	1 to 3 °C/sec
Peak Reflow Temperature	240 ± 5 °C
TAL (>220 °C)	60 ± 10 sec

SMT yield loss was observed during early development stages on both the cavity and the full array FCBGA used in this study. In order to overcome the SMT challenges and to improve yields, there was a need to characterize the SMT process to understand the key parameters modulating the yield. Printed paste volume characterization was done by modifying the stencil designs on both the product types to define a safe printing envelop. For the cavity array FCBGA package, a 4mil thick stencil was originally used and the packages were

reflowed on PCB A design that represented actual product configuration using a SAC305 lead-free solder paste. Actual product packages were used for SMT yield assessment. Initial yield assessment was based on visual inspection and X-ray. The average SMT yield obtained was lower than expected and failures were observed at package warpage levels much lower than the cliff derived for similar stencil as shown in Figure 6. The cliff is a maximum reference warpage used in this study.

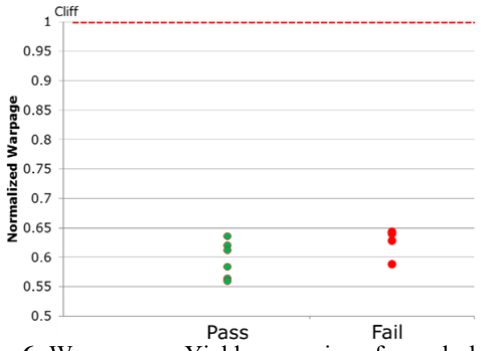


Figure 6. Warpage vs. Yield comparison for early builds on PCB A

Within the failed units, varying levels of second level interconnect (SLI) open defects were observed at solder ball level inspection. Majority of the open failures were observed near the shorter edge of the package as shown in Figure 7. Stretched joints were also observed at non-failing locations near the shorter edge of the package. Failure analysis on failed units through cross section confirmed that the open defects showed a mix of non-wet open (NWO), non-contact open (NCO), and head-on-pillow (HnP).

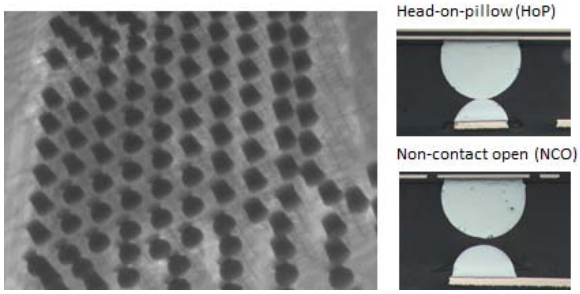


Figure 7. Tilted 2D X-ray image showing stretched solder joints and massive HnP/NCO open failures

In order to improve the SMT yield, a new stencil design was implemented by changing the stencil aperture from 12 mil-round opening to 13 mil-square opening for the package-body pads shown in Figure 8 with details in Table 3. This lead to a 49% increase in paste volume target on the body pads. SMT builds using an optimized stencil resulted in an increase in SMT yield. Hwever failures were still observed at lower package warpage levels with same defect modes. Cross sections confirmed similar solder joint quality marginality in terms of stretched joints at shorter edges even after stencil modification.

Based on the above findings, the PCB was redesigned to PCB B where the Cu plane in the cavity area was removed. SMT builds on PCB B using an optimized stencil showed no fails for units around and below the cliff (Set 2) whereas PCB A continued to show marginality. Testing PCB B type design, with packages slightly above the warpage cliff (Set 1), also resulted in no solder joint failures thereby showing some margin as shown in Figure 9.

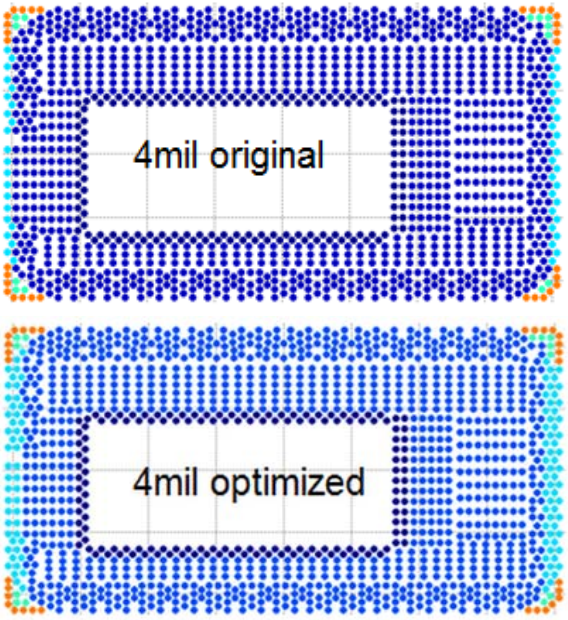


Figure 8. Original and optimized stencil design used on Product cavity array FCBGA package

Table 3. The original and optimized stencil designs

Stencil design	Location	Aperture
4mil original	Corner 1st row	15 × 25
	Corner 2nd row	16 × 16
	Short edge	15 × 15
	Body	**12 round**
	Cavity edge	11 round
4mil optimized	Corner 1st row	15 × 25
	Corner 2nd row	16 × 16
	Short edge	15 × 15
	Body	**13 × 13**
	Cavity edge	11 round

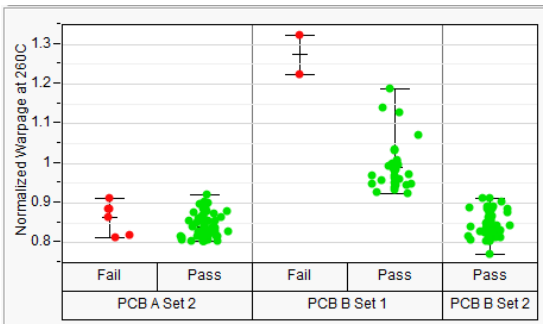


Figure 9. SMT results on PCB B with PCB A control

The full gird array FCBGA package assembled on PCB C and PCB D designs also showed sensitivity to the PCB surface features during SMT process development. With same stencil design, PCB D showed significantly lower yield as compared to PCB C with solder bridging defect under the die-shadow as a dominant failure mode as shown in Figure 10. Stencil design was further optimized to print less paste in the die shadow region for both the PCB designs. The stencil change with reduced paste volume in the die shadow region was partially able to modulate the SMT yield on PCB D design but there was still some marginality and abnormal solder joint flow behavior in comparison to PCB C design.

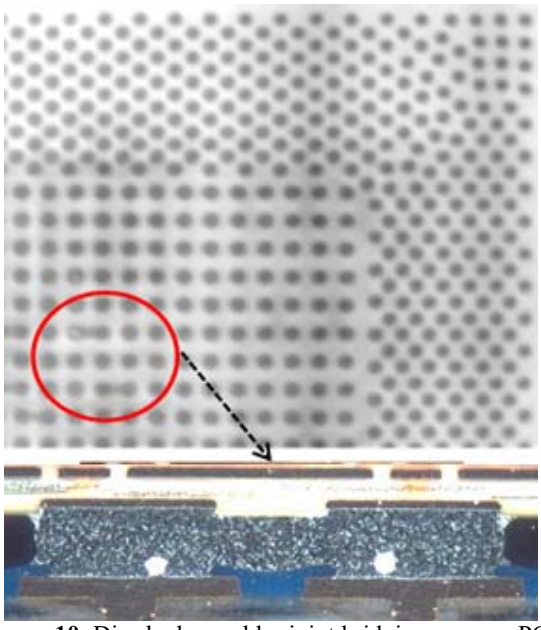


Figure 10. Die shadow solder joint bridging seen on PCB D

SMT yield analysis indicated that the surface topography created by the PCB designs had an influence on the solder collapse and also the molten solder flow behavior during SMT leading to solder joint defects. Understanding this required further investigation through fundamental experimental studies as discussed in the next section.

DISCUSSION ON THE FAIL MODES

The dominant failure mode observed on cavity array FCBGA packages on PCB A was solder joint open defect. Physical FA was conducted by cross-sectioning along the package edge and center-row solder joints and measuring the solder joints (SJ) standoff heights (SOH) on pass and failed units. SJ SOH trends reflect the relative package and board warpage shape upon solidification.

SJ SOHs measured on passing units each from different PCB designs (PCB A, B, and M, as described in Table 1) showed that average SJ SOH was lower on PCB B and PCB M than PCB A as highlighted by red lines on the graph in Figure 11. Lower SJ SOH indicated that solder collapse was more on PCB designs B and M than on PCB A. Cavity array FCBGA packages have land side capacitors (LSC) in the center cavity region on the bottom side of the package substrate to optimize power delivery requirements in package. It was hypothesized that PCB A which had a step-up height of 35-40µm in the cavity region caused the LSCs on the cavity array FCBGA package to bottom out much earlier as compared to PCB B which allowed more collapse before LSCs bottom out.

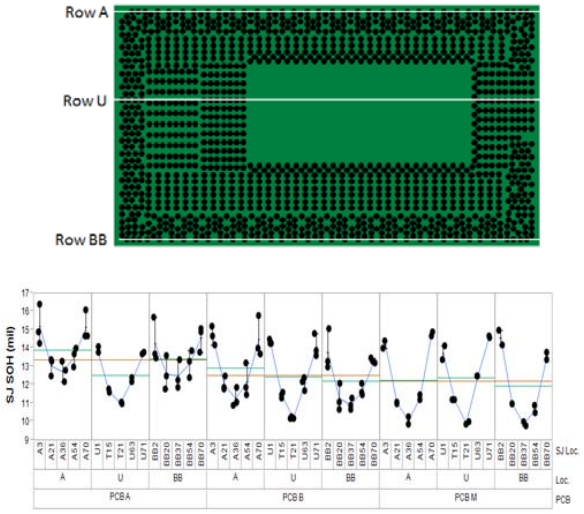
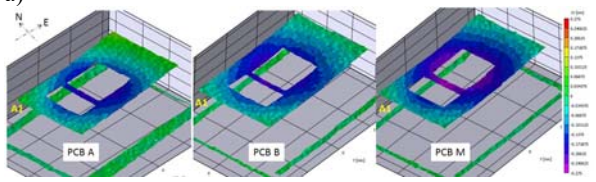


Figure 11. Measured SJ SOHs from three PCB designs

To verify the collapse differences between the PCB types, an experimental in-situ lab-based SMT technique was employed to characterize solder joint collapse, and to study BGA package and PCB warpage interactions during reflow. Studies were conducted with identical conditions as seen during the SMT assembly process using an experimental setup consisting of a simulated SMT reflow oven and digital image correlation (DIC). Digital image correlation (DIC) is a non-contact, full-field optical measurement technique used for quantifying displacements on a sample of interest in the *x*, *y*, and *z* directions with the help of stochastic speckle pattern. The DIC technique employed is capable of measuring the relative change in shape between two configurations, such as package and PCB displacement, to resolution of 11 µm [9]. Identical cavity array FCBGA packages in terms of their warpage magnitude and shape were placed on PCB A, B and M and were run through a simulated SMT profile. Collapse in the center rib region of the cavity array FCBGA package was monitored by tracking the z displacement of the rib with respect to the PCB for all the above 3 cases. Figure 12a, shows comparison of cavity array FCBGA warpage contour at reflow temperature for PCB A, B and M. The color bar scale represents contours

of constant height, with red and purple indicating the high and low points, respectively. Due to absence of any center cavity region constraints in PCB M, the cavity array FCBGA package collapses more on PCB M than on PCB A. Collapse on PCB B falls in between PCB A and M. The magnitude of the collapse on PCB M was about twice the collapse achieved on PCB A. The collapse margin reduction due to presence of these surface features was estimated to be around 22% as highlighted in the Figure 12b.

a)



b)

Figure 12. a) in-situ package warpage shape difference on PCB A and PCB M at peak reflow temperature b) Collapse magnitudes on PCB A, PCB B and PCB M during in-situ SMT reflow

The loss in SMT margin on PCB A was also quantified using a SMT collapse model based on minimization of surface energy of solder joints. The SMT model used here is able to predict the FCBGA package collapse based on the stencil design, PCB land pattern and FCBGA package warpage as the input. PCB surface features observed on PCB design A were simulated by effectively increasing the height of the LSCs from the substrate over that assumed for PCB design B. Figure 13 shows the results from the model normalized with respect to the PCB B condition across PCB warpages. It is evident that the taller LSCs used to simulate PCB A would cause loss in NCO margin at even lower PCB warpage levels and yield losses will increase further with increase in PCB warpage.

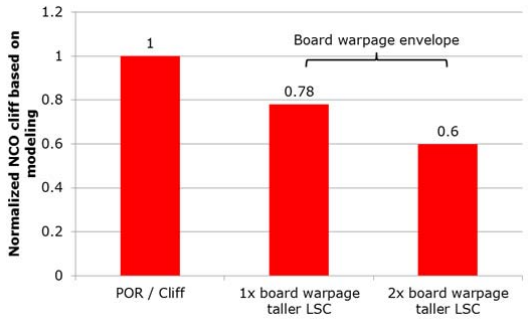
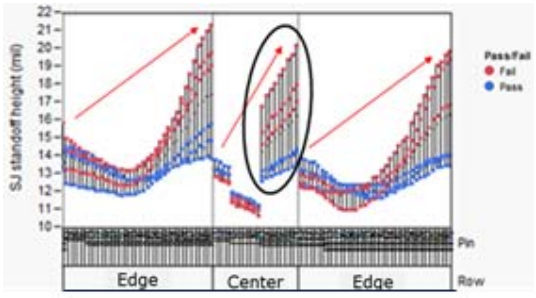


Figure 13. Modeling results showing loss of NCO margin

On the failing units, apart from the extra standoff due to LSCs, an abnormal SJ SOH trend was observed as shown in Figure 14a. The SJ SOH on the east side of the package was significantly higher than on the west side for both the outer rows and center row SJs. Comparing the center-row SJ SOH trends between the passing and the failing units, it was apparent that passing and failed units have similar SOH values on the west side of the cavity, but there are distinct differences on the east side of the cavity (data points highlighted in the ellipse in Figure 14a). The reason for this abnormal behavior was attributed to cavity array FCBGA package tilting before solder melting when the LSCs bottom out on the PCB, as shown in the schematic in Figure 14b. LSCs bottoming out during SMT was confirmed through a quick in-situ SMT lab experiment by using a see through glass PCB taped in the center cavity region to create PCB surface feature effect similar to PCB design A. Flattening of the LSC solder terminations was observed during SMT with help of cameras mounted to the reflow simulator oven along with remnants of the footprints of the capacitor solder terminations that bottomed out on the tape after SMT as shown in Figure 14c.

a)



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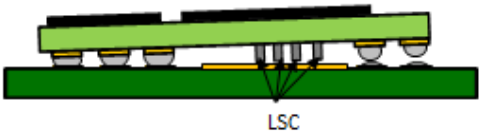

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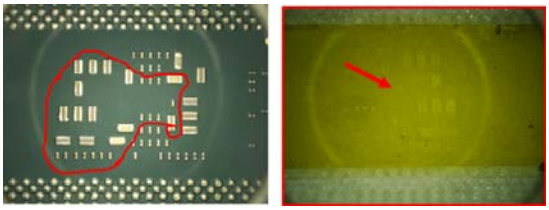
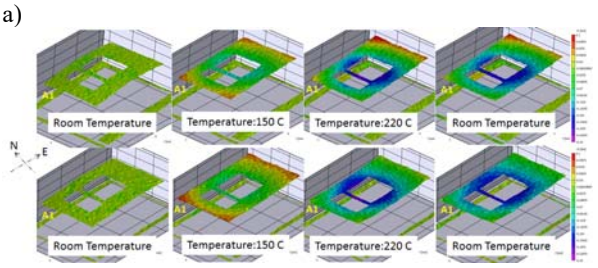


Figure 14. a) Measured SJ SOH trends indicate package tilting in failed units b) schematic showing interaction between the LSC and the cavity Cu plane causing tilting during reflow c) Set of capacitors that touched PCB during in-situ SMT experiment causing NCO type failures

The in-situ SMT DIC approach was used to further understand tilting observed on cavity array FCBGA packages. Identical cavity array FCBGA packages were reflowed on PCB A, B. PCB M with a cut out center cavity was excluded since no LSCs bottoming was expected with this design. Cavity array FCBGA package warpage behavior with respect to the PCB was monitored as the assembly was reflowed. The progression in the

FCBGA package warpage contours of the FCBGA package as it undergoes a simulated SMT temperature reflow profile are shown in Figure 15a. Again, red and purple colors in contour represents high and low points. The initial room temperature condition shows that the FCBGA package on both the PCBs is flat to slightly convex, but symmetric about the center of the package. This symmetric warpage condition prevails until about 150C. However, as the FCBGA package-PCB assembly is heated to the reflow temperature, the warpage increases and the component tilts upwards in the east direction on the top side of PCB A whereas PCB B showed no such tilt behavior. The out of plane displacements measurements at the corners of the FCBGA package as shown in Figure 15b also show that package corners freely collapse on PCB B case whereas for PCB A the corner keeps getting away from the PCB due to early bottoming out of the LSCs creating tilt.

a)



b)

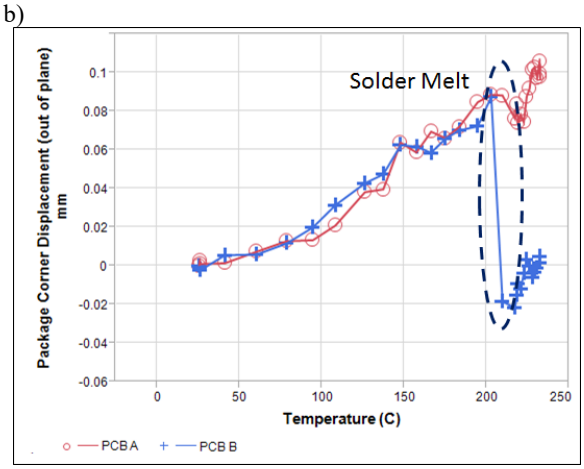
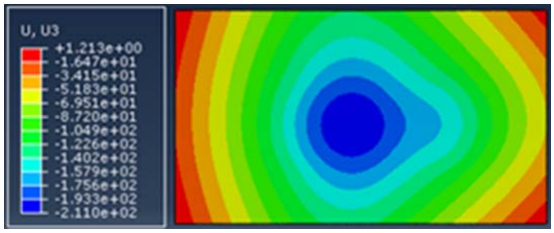


Figure 15. a) in-situ package warpage behavior on PCB A and PCB B during SMT b) Out of plane displacements at corner of the package for PCB design A and B.

Finite element modeling of cavity array FCBGA package was completed to demonstrate that the asymmetric nature of cavity array FCBGA package design does not cause the FCBGA package to tilt. Figure 16a and 16b shows the modeled warpage contours for cases without and with solder balls or LSC. The former warpage profile is more symmetric while the later shows tilt and increased warpage magnitude consistent with the solder joint cross section observations and DIC measurements.

On full grid array FCBGA packages that were built on PCB C and D designs, the dominant failure mode was solder bridging in the die-shadow region. In order to better understand the failure mechanism and sensitivity to the PCB surface features, an in-situ SMT X-ray technique was used. Both PCB C and D were cut to expose the BGA component region. Solder paste was printed using a mini-rework stencil. Full grid array FCBGA packages similar in terms of warpage magnitude and shape were placed on both PCBs using a placement tool. The coupons were then reflowed in the X-ray system equipped with conduction heating capability. In-situ X-ray images (2D) were captured as the entire assembly was reflowed. Solder flow and solder joint collapse behavior were studied.

a)



b)

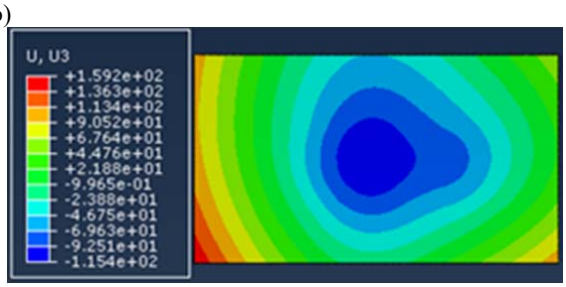


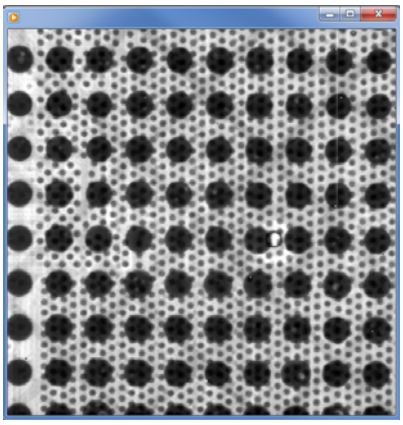
Figure 16. Modeled warpage contour for package (a) without BGA and LSCs and (b) with BGAs and LSCs

In-situ X-ray images showed different solder flow pattern for PCB C and D. The PCB designs differ in terms of SMD pad layout in the center die shadow region as described in Table 1. For PCB C, where SMD pads exists on an underlying flood plane, uniform flow of molten solder around the pads was observed post collapse as shown in Figure 17a. The solder joints were more circular in shape in the area of interest at peak reflow temperature of 240C. On the other hand, for PCB D, where SMD pads use defined connected traces, the direction of solder flow was in a form of an oval shape around the pads. Solder appeared to flow directionally towards each other creating a near-bridging type of scenario, as highlighted in Figure 17b. Near-bridging was noticed mostly in the horizontal direction with tighter pitch (~0.5mm) than in the vertical direction where the pitch was slightly larger (~0.55mm). Solder bridging failure locations and pattern from the in-situ SMT X-ray experiment matched with actual SMT results.

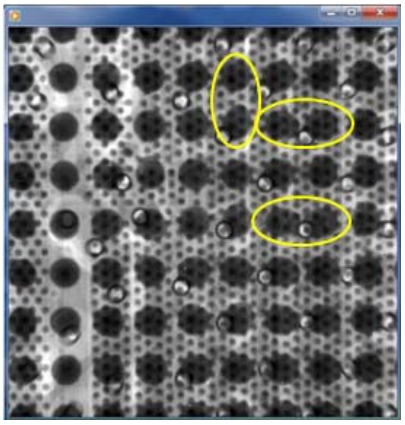
The solder flow pattern on PCB D design was then mapped with actual PCB pad layout to explore if there was any commonality that would help explain the directional solder flow. Figure 17c highlights some of the nearby pad locations that nearly bridged during the in-situ reflow experiment. Comparing these locations with the PCB design file showed that the highlighted near bridge pairs were connected to different power rails. It was suggested that the flow of molten solder between the near bridge pads could possibly be facilitated by presence of any solder mask undulation created during PCB

manufacturing as a result of asymmetric pad layout during PCB manufacturing as explained in section 2. In contrast, the pad locations that were connected by same power rail traces showed no such solder mask undulations between the pads and as a result no directional molten solder flow was observed between them.

(a)



(b)



(c)

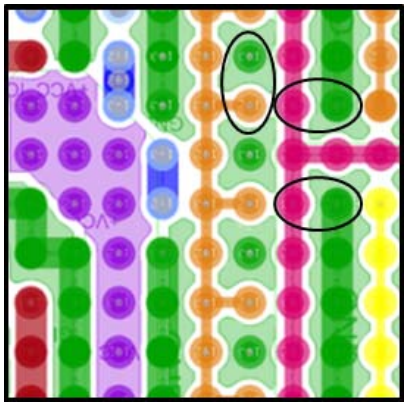
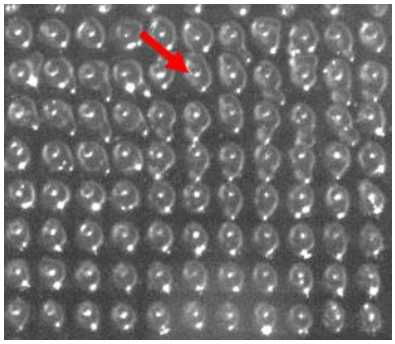


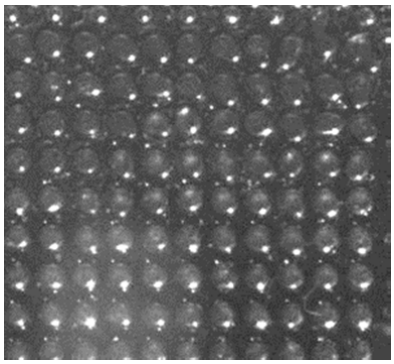
Figure 17. a) and b) Top-view X-ray image collected at ~240°C for the SMD pads on a single CU plane and SMD design connected with traces, respectively; (c) corresponding PCB top-layer design showing directional solder flow across the traces

The observation of directional solder flow on SMD pads defined on power rails was further explored by running an in-situ SMT experiment using static weights. A glass package with similar BGA foot print was prepared and placed on both the PCBs. Use of glass package makes it possible to capture in-situ solder flow behavior. The assembly was run through SMT oven with a static weight on top of the glass package to simulate worst case loading condition. After reaching reflow temperature, the package collapsed under the influence of the weight and solder spread into the areas surrounding the pads. It was observed that the spread of solder aligned with the PCB surface features on PCB D whereas in PCB C the spread was more random, as shown in Figures 18a and 18b. To understand this directional solder flow behavior further especially on PCB D design, a flux only experiment was done by applying dyed flux on PCB D and heating it through a simulated SMT profile. It was observed that with increase in temperature, the flux was able to freely flow into the channels created by the surface features between the pads as shown in Figure 18c. With puddle of flux in the channels it was easy for the solder to spread into these areas thus providing for the directionality of solder bridging as observed on PCB D during SMT.

a)



b)



c)

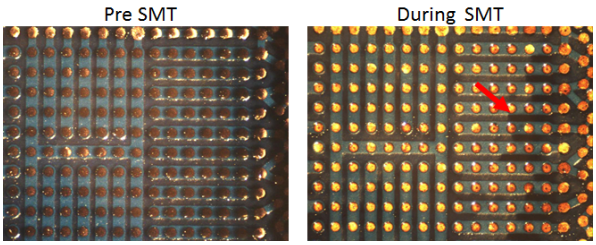


Figure 18. a) Solder flow behavior during SMT on PCB D b) Solder flow behavior during SMT on PCB C c) Flux (dyed) deposited on the pad pre SMT and flux flow behavior observed during SMT on PCB D design.

SMT collapse model SJ width findings by reverse fitting the SJ SOH data obtained on PCB D design post SMT also showed disagreement for the center die shadow

region of the package where the solder joints showed abnormal flow behavior. The model SJ width predictions matched well with the measured values where the SJ width was symmetric as shown in Figure 19a and 19b.

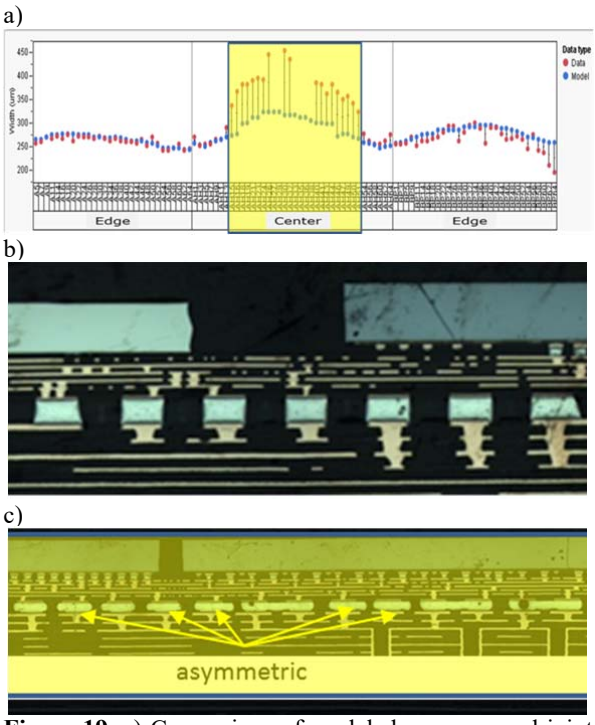


Figure 19. a) Comparison of modeled vs. measured joint widths b) Cross-section image of edge joints showing normal behavior c) Cross-section image of center joints showing asymmetric behavior

SUMMARY AND RECOMMENDATION

This paper demonstrated the influence of PCB design features on the resulting SMT quality. PCB design features in the center of cavity grid array FCBGA package, in form of raised PCB surface topography, was shown to interfere with package collapse, alter solder joint formation and create open defects. Uneven PCB surface features created as a result of dense trace routing, impacts the solder joint creation during the reflow soldering process and may result in increased risk of solder joint shorts as demonstrated in this paper. Traditional SMT process optimizations did improve quality in some cases. However, increased density and pitch reductions may drive demands for improved PCB features design for manufacturing measures.

PCB designers are challenged to deal with a diverse set of requirements and driven to design with complex interactions. As detailed, the ongoing densification of platform designs increases sensitivities and drives the need to improve design margins. It is important that platform designers be aware of possible interference of PCB surface features and impacts to SMT assembly. Some of the PCB design recommendation based on the SMT impact from two PCB surface feature cases studied here, would be to try and possibly shift any isolated copper planes at the PCB surface in the BGA region to internal PCB layers.

Additionally, focus should be to try and minimize any surface profile and pad type variations. For example, copper thickness of outer layers can impact adjacent solder mask surface profiles as shown in Figure 20.

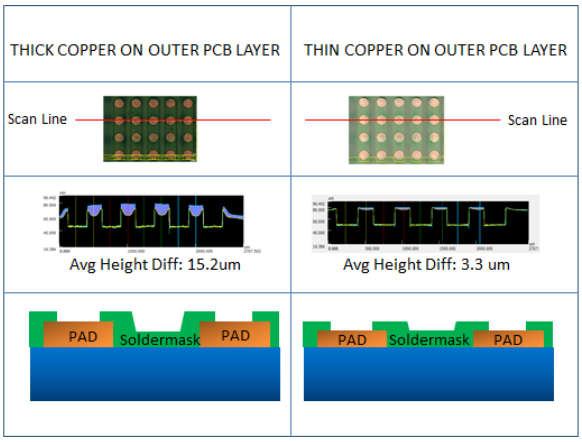


Figure 20. Surface profile measurements of thick and thin outer layer copper foil thickness coupons. Cross sections illustration of copper thickness impact to solder mask surface profile variation.

Dense trace routing networks in the BGA region at the PCB surface may drive pad type variations. If PCB thickness is not a constraint, then similar approach of having only pads at the PCB surface by routing the entire trace network through internal PCB layers should be considered as shown in Figure 21.

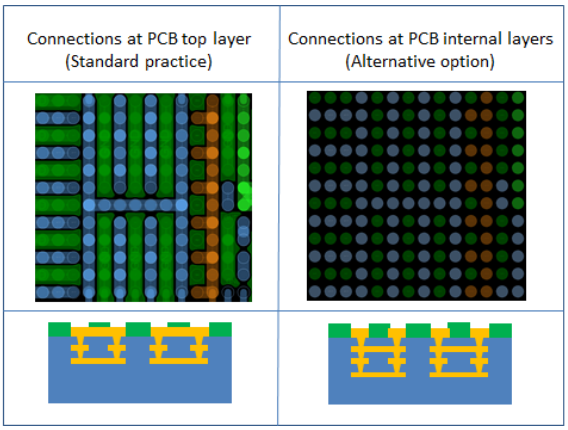


Figure 21. Planar and cross section demonstrate of stackup variations that may benefit outer layer solder mask profile variation

ACKNOWLEDGEMENTS

The authors would like to acknowledge the help of Steve Klein, Amit Abraham, Michelle Phen, Eric Brigham, Jamie Gillespie, Li-Sheng Weng, Joe Van Nausdle and Prasanna Raghavan for their invaluable contribution towards understanding the issues seen above.

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