EXTRA FINE PITCH FLIP CHIP ASSEMBLY PROCESS, UNDERFILL EVALUATION AND RELIABILITY

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ABSTRACT

Interest in using fine pitch SMT components has increased greatly in recent years due to the growth of portable, hand held electronics and due to miniaturization trends in consumer and industrial electronics markets. The reliability of those fine-pitch portable electronics products is a great concern particularly in the areas of impact and shock performance. For very fine pitch SMT components such as WLCSPs and BTCs without ground planes (0.5mm pitch or lower), underfills can be used to improve the impact and thermal cycle reliability. Historically, the target properties of underfills can be generally summarized as high glass transition temperature (Tg), high modulus (E) and matched coefficient of thermal expansion (CTE) to solder. However, the underfill selection and evaluation process has become increasingly complex, time consuming and cost prohibitive due to increasing product design constraints, introduction of new package materials, and ever changing from factor of semiconductor packages. With every new generation of package technology, one must factor into the underfill selection process, new solder alloys and soldermasks, thinner substrate core materials, finer pitches, and increasing package dimensions.

This paper focused on the extra fine pitch Flip Chip assembly process, Flip Chip underfill dispensing process, evaluation and reliability issues. A 0.2mm pitch Flip Chip PB8 was used for this study. Four types of flux, seven types of Flip Chip commercial underfills from various venders were applied. The details of the assembly process, underfill dispensing issues are discussed in this paper. The air-to-air thermal cycle and thermal-humidity reliability testing data are included. The comparison and evaluation of these fluxes and underfills for Flip Chip application are presented as well. The best flux and underfill combination in reliability performance was selected and applied to the production process.

Key words: Flip Chip, Assembly Process, Dispensing Process, Underfill Evaluation

INTRODUCTION

Due to the demand growth for portable, hand held electronics products with a lighter weight, smaller size, higher performance in consumer and industrial electronics markets, the interest in using fine pitch SMT components, such as BGA, 0.4/0.3 mm pitch WLCSPs, Flip Chips, 0201, 01005 components, and smaller components, has increased greatly in recent years. The usage of these fine-pitch and high-density packages and devices have had a tremendous impact on board-level reliability and assembly process. Against mechanical drop/shock and temperature cycling, solder joint reliability deteriorates as the result of smaller solder joint size with pitch reduction. Board level underfill (BLUF) has been known as a solution for handheld devices in providing solder joint with an additional mechanical protection against drop/shock.

Flip-chip interconnect technology is an advanced electrical interconnection approach where the silicon die or chip is electrically connected face down to the substrate by reflowing solder bumps on area-array metallized terminals on the die to match footprints of solder-wettable pads on the chosen substrate. This advanced flip-chip interconnect technology will significantly improve the performance of high-speed systems, the productivity enhancement over manual wire bonding, self-alignment during die joining, low lead inductances, and reduced need for precious attachment of metals. The disadvantages of flip chip include high assembly accuracy is needed, the short connections are very stiff and may cause low reliability issue, etc.

Underfill is a polymeric material used to fill the gap between the IC chip and the organic board, encapsulating the solder joints. It enhances device reliability by distributing thermo-mechanical stresses caused by the coefficient of thermal expansion (CTE) mismatch between chip and board evenly over the whole package. Underfill absorbs the CTE mismatch and therefore reduces significantly stress to a more uniform distribution on solder joints. Conventional underfills are not reworkable after post cure. As a result, faulty packages are often disposed of if

failure occurs. Reworkable underfill on the other hand, enables packages to be repaired, replaced, recovered or recycled. These materials can be thermally decomposed at a lower temperature and the decomposition residues can then be removed using commonly available solvents, without damaging the underlying electronic components. They have also evolved to be very easily used in board assembly line with fast flow, low temperature and instant cure [1, 2].

Historically, the target properties of underfills can be generally summarized as high glass transition temperature (Tg), high modulus (E) and matched coefficient of thermal expansion (CTE) to solder. In the past of decades, a lot of studies have been commissioned to evaluate the selection, application, assembly process and reliability of the commercial underfills at that time [3-13]. In the recent of years, however, as the increased product design constraints, updated new package materials, and changed new generation of package technology, the underfill selection and evaluation process has become increasingly complex, and many factors need to be considered and investigated usually.

This paper focused on the extra fine pitch Flip Chip assembly process, Flip Chip underfill dispensing process, evaluation and reliability issues. A 0.2mm pitch Flip Chip PB8 was used for this study. Four types of flux, seven types of Flip Chip commercial underfills from various venders were applied. The details of the assembly process, underfill dispensing issues are discussed in this paper. The air-to-air thermal cycle and thermal-humidity reliability testing data are included. The comparison and evaluation of these fluxes and underfills for Flip Chip application are presented as well. The best flux and underfill combination in reliability performance was selected and applied to the production process.

TEST VEHICLE AND DEVICES

New designed PCBs were used as the test vehicle for this Flip Chip application, shown in Figure 1. The dimension of these boards is 145mm x 94mm x 1mm. There were 12 devices on the board design. On each device site, four local fiducials were designed to make the placement more accurate. Many probing pads were also designed surrounding the device to monitor the daisy chain failure location. NSMD pads were used for all pads and ENIG was used as the surface finish. The devices used in this application were Flip Chip PB8, as shown in Figure 2. This PB8 device has a 0.2mm pitch with perimeter 88 solder balls giving 44 daisy chain pairs. The body dimension is 5mm x 5mm x 0.6mm. The solder bumps use SAC305 alloy and their diameters are 0.115 ± 0.03mm.

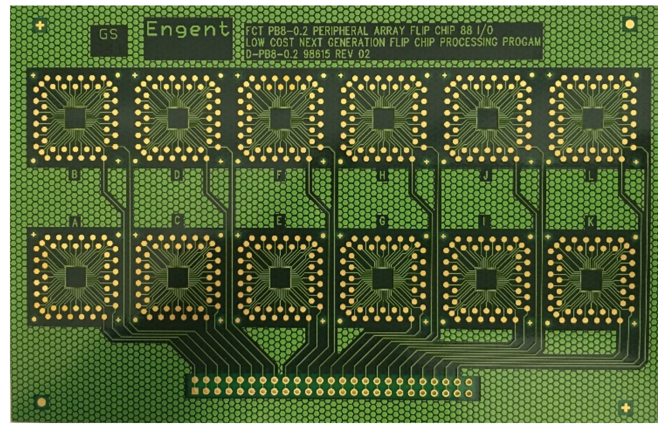

Figure 1. Flip Chip PB8 test vehicle

Figure 2. Flip Chip PB8 device used in the application

ASSEMBLY PROCESS

The assembly process development and assembly work were conducted at Engent Inc., Norcross, GA. For the 0.2mm pitch pads, only dip flux was used, no solder paste printing. The dip flux and placement machine used Siemens Siplace F5, and the reflow oven used Rehm VXS634. The test plan included using Flux S1, Flux S2 and Flux I1 to build the test vehicles, and then applying 6 types of underfills on the boards to compare their compatibility and reliability. These 6 materials are all Flip Chip underfills from varied vendors, named as UF-A, B, C, D, E, F.

Dipping flux was applied at the same time as the device Pick and Placement process. Normally the dip flux thickness is required to be at least 50% of the solder ball diameter. Because Flux S1 will be burned off much faster compared with other flux, more dip thickness were used to leave more flux dipped on the device solder balls to make sure the flux will not be burned off during reflow process. The actual dip thickness used for this assembly was around 80 um. The image for the dip flux S1 was shown in Figure 3 below.

Figure 3. Dip flux S1

For the placement, local fiducials has to be applied as the reference of the single component placement. In the beginning of the placemen process development, the global fiducials were used to place all components. An accumulating error had occurred and some component were found to have offset in the placement. And such offset could not be avoided due to the accuracy of the placement machine based on the global fiducials. No matter how accurate in the pick & place programming, offsets for some components were always happened. After using the local fiducials, each component in every site could be placed very accurate.

For the reflow process, a Ramp-To-Peak profile was found to be much better for flux S2, which were burnt off much faster than other flux. Nitrogen reflow environment is required for this application. The key reflow parameters are: Ramp time 50ºC-220ºC 116 second, Reflow time (TAL) 41 second, Peak temperature 242ºC. A longer-time or slow profile will cause the flux burnt off problem and then cause the solder wetting issue, and the reliability will be deteriorated as well. The reflow profile used for Flux S2 is shown in Figure 4.

Figure 4. Ramp-To-Peak profile for flux S2

A similar Ramp-to-Peak reflow profile was developed for flux I1. This profile was designed to have a longer ramp and Temperature above Liquidius (TAL) because Indium flux was not as easy to burn off as flux S2, and it can stand for more time to activate. The key reflow parameters are: Ramp time 50ºC-220ºC 142 second, Reflow time (TAL) 52 second, Peak temperature 245ºC. The reflow profile used for Flux I1 is shown in Figure 5.

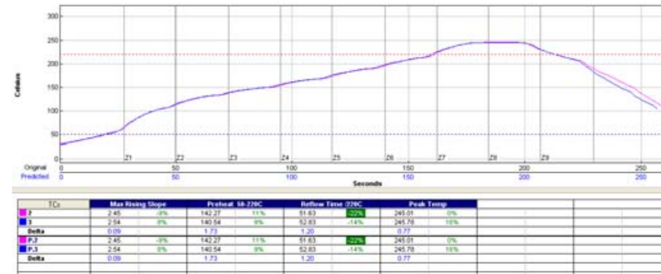

Figure 5. Ramp-To-Peak profile for flux I1

After the first article was built, cross section was conducted to analyze the build quality and check the reflow profile. Figure 6 shows the SEM image for the first row of solder joints after reflowed. All the solder joints look to have good shape and good wetting. Figure 7 shows a single joint with the height. Again, it shows the good shape and wetting. The solder joint height was about 70 um after device collapsed. Figure 8 shows the imtermetallic layer on the board pad side and it shows there is a good bonding between the solder and the board pad.

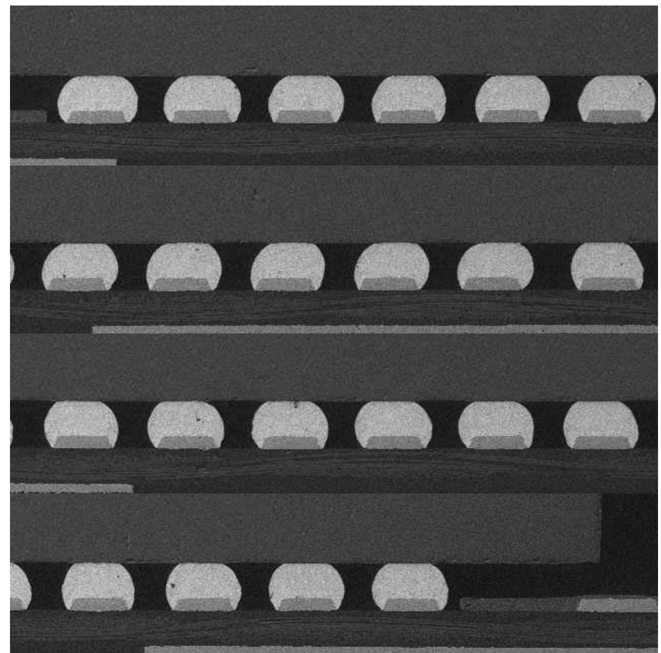

Figure 6. SEM image of cross section for the 1st article

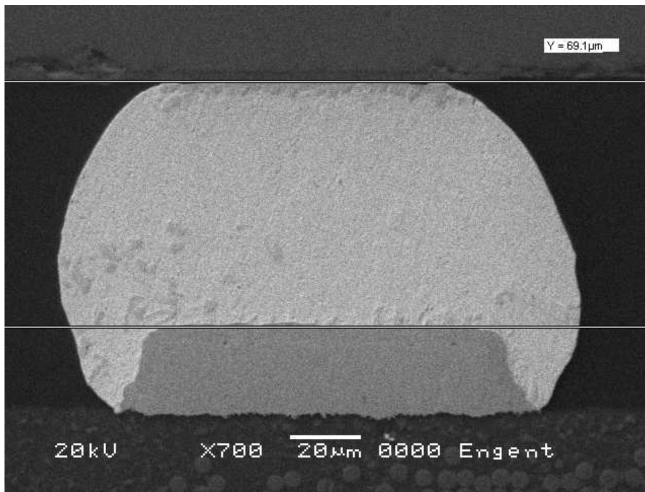

Figure 7. Single joint height – about 70um

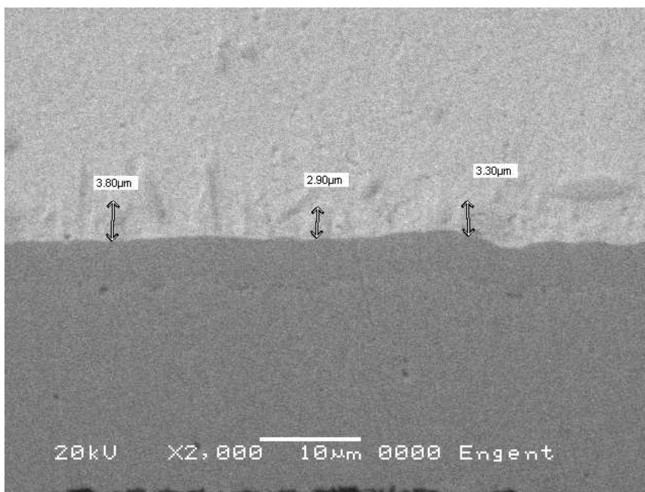

Figure 8. Intermetallic layer on the board side

Besides the cross section, shear test was conducted as well, the results also indicate very strong bonding on the pad side. All shear failure modes showed to be the bulk solder failure at the chip side. Figure 19 & 10 show the failure mode after the PB8 was sheared off. In addition, the X-ray image after reflow also showed that no voiding is found on the solder joints. All these analysis and test indicate that the assembly process was very robust and developed very well.

After all the boards were assemblied, 6 types of underfill materials were applied to improve the component and board reliability. Underfill dispensing process used Asymtek S-820 dispensing machine. Underifll A, B, C were provided from varied vendors, and the underfill material D, E, F were provided by H. B. Fuller Co. Jetting process was applied for this device application. The key jetting parameters are: needle tip temperature 80ºC, Hot plate temperature 100ºC to keep the underfill flow, fluid pressure 25 psi. Jetting used weight control and the material weight was 9.0 mg for each device. The underfilled device and the underfilled detail are shown in Figure 11 & 12 respectively. A C-SAM inspection was performed to check the underfill voiding and quality. Figure 13 shows this image and there is no voiding. All these test and analysis results indicated that the assembly and underfill process were robust.

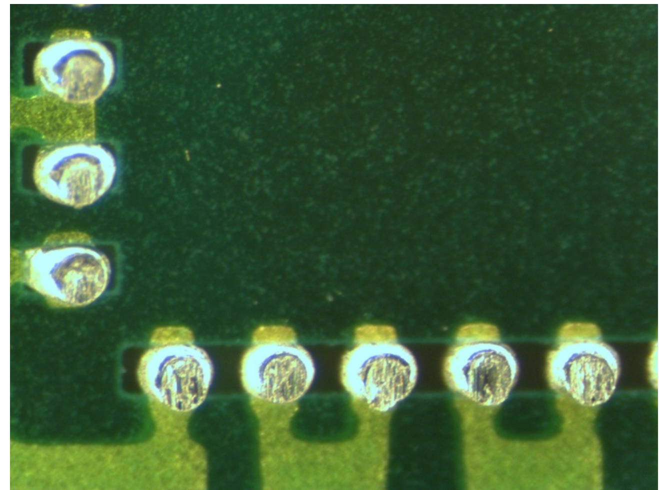

Figure 9. Shear test failure mode - board side

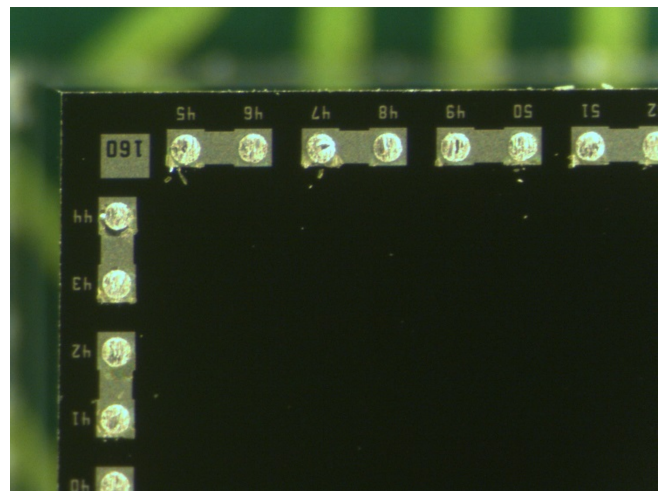

Figure 10. Shear test failure mode - chip side

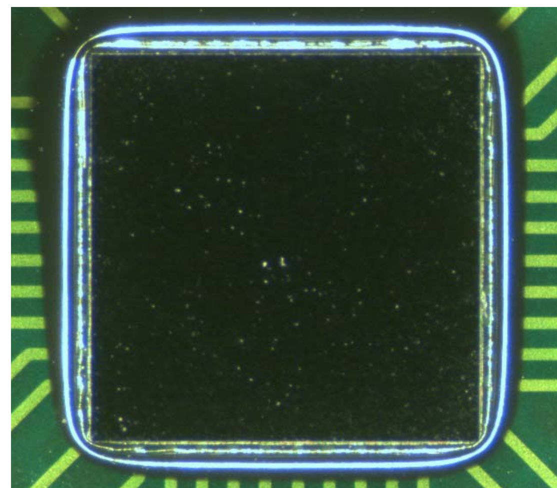

Figure 11. Underfilled device

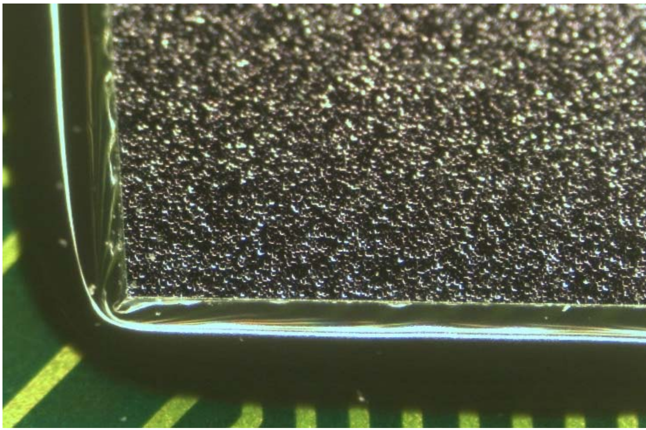

Figure 12. Underfilled device - detail

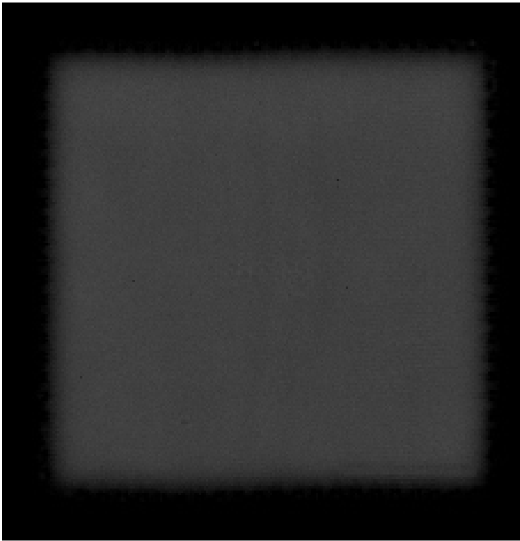

Figure 13. C-SAM image for undefiled device

RELIABILITY TEST – THERMAL CYCLE

Thermal cycling test was conducted for these underfilled daisy chain Flip Chip PB8 components. A two-zone ESPEC thermal cycle chamber was used for this test. Three boards for each batches were tested. The test conditions were: -40°C to 125°C, 15 minutes dwell time. Figure 14 shows the boards in the chamber. In order to monitor the actual thermal profile on boards, a thermal couple was attached on the back side of a test board, and this thermal couple was connected to a Fluke thermal humidity meter to monitor the actual temperature profile. A software program then record the data. Figure 15 shows the actual thermal profile on boards. The ramp time was 8 minutes, and the dwell time is 15 minutes.

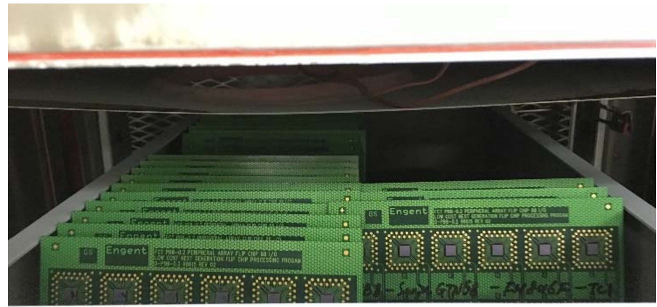

Figure 14. Thermal cycle test boards in chamber

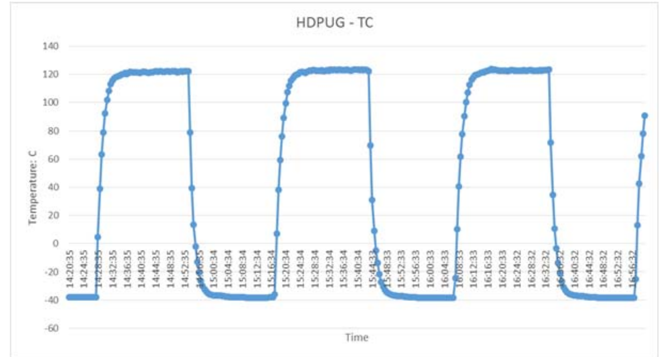

Figure 15. Actual thermal cycle profile on boards

All underfilled boards were probed every 200 cycles through 1200 cycles. The tests were extended till all daisy chains failed. The criteria for the potential failure or reliability issue was the daisy chain resistance increased 30%. Table 1 shows the reliability data and compares all the underfilled components. From the results, Underfill C with flux I1 flux had the best reliability. This test has not finished yet, so the Weibull plot cannot be figured out by now. The test will keep going till all daisy chains fail. The final results will be posted in the future.

Table 1. Flip Chip PB8 thermal cycle reliability data

Cycles & UFs	200	400	600	800	1000	1200
UF A Flux I1	0/28	0/28	2/28	3/28	3/28	3/28
UF B Flux K1	0/32	1/32	20/32	32/32	32/32	32/32
UF C Flux I1	0/33	0/33	0/33	0/33	0/33	0/33
UF D Flux S1	0/33	0/33	0/33	0/33	0/33	1/33
UF D Flux I1	0/29	0/29	0/29	0/29	0/29	6/29
UF F Flux S1	0/22	0/22	0/22	0/22	0/22	0/22
UF F Flux S2	0/32	0/32	0/32	0/32	7/32	9/32

RELIABILITY TEST – THERMAL HUMIDITY TEST

At the same time, a thermal humidity test was performed as well for the other batch of underfilled devices. The test condition was 85C with 85% humidity. The samples were taken out to probe and have C-SAM every 168 hours. The probed result was shown in Table 2.

Table 2. Thermal humidity test results

Hours & UFs	168	336	504	672	840	1008
UF A Flux I1	0/23	0/23	0/23	0/23	0/23	0/23
UF B Flux I1	0/33	0/33	0/33	0/33	0/33	0/33
UF C Flux I1	0/31	0/31	0/31	0/31	0/31	1/31
UF D Flux S1	0/22	0/22	0/22	0/22	0/22	0/22
UF D Flux I1	0/30	0/30	0/30	0/30	0/30	0/30
UF E Flux S1	0/22	0/22	0/22	0/22	0/22	0/22
UF E Flux S2	0/33	0/33	0/33	0/33	0/33	0/33
UF F Flux S1	0/21	0/21	0/21	0/21	0/21	0/22
UF F Flux S2	0/32	0/32	0/32	0/32	0/32	0/32

So far, there was only one failure found for this thermal humidity test. The probing and test will continue. The C-SAM images will be reported in the future as well.

SUMMARY AND CONCLUSIONS

A very fine pitch Flip Chip PB8 application on the test vehicle was conducted. The assembly process was developed and material reliability was evaluated. The devices used in this application was 0.2mm pitch daisy chain PB8. Four flux and 6 underfill materials were used for the assembly and reliability in this study. The details of the assembly process including dip flux, component placement, reflow and underfill dispensing have been discussed in this paper. JEDEC standard air-to-air thermal cycling and thermal humidity tests are performed for the reliability evaluation purpose.

All the cross section analysis and shear test results show that the assembly process with the Senju and indium flux was very robust. And the underfill material dramatically improved the reliability performance of the assembled devices. For the thermal cycle test, underfill C had the best performance, and underfill D & F are followed.

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