

ELECTRONIC PACKAGES AND MODULES BASED ON EMBEDDED DIE TECHNOLOGIES

Lars Boettcher¹, Stefan Karaszkiwicz¹, Dionysios Manassis² and Andreas Ostmann¹

¹ Fraunhofer Institute for Reliability and Microintegration (IZM),

² Technical University of Berlin

Berlin, Germany

lars.boettcher@izm.fraunhofer.de

ABSTRACT

This paper will describe the use of embedded die technologies for various application fields. The main focus of the development work in the presented European funded project EmPower [1] is on power electronic applications.

Here, three different power levels are of interest:

- 50W single die packages with fast rectifier diodes
- 500W power modules for electric bicycle application
- 50kW power modules for HEV and EV application

All three application fields are based on a similar concept, which is called embedded power core. For the higher power modules additionally thermal management is required. Here a construction of IMS substrates and the power core is chosen. This construction enables a double sided cooling and also the electrical isolation of the module to the cooler. The connection between power core and IMS substrates is made by low temperature and low pressure Ag sintering.

All three applications fields will be described in detail. Besides the power core manufacturing, the paper will elaborate on the sintering process for Power Core/IMS interconnections, the microscopically features of the sintered interfaces, and the lateral filling of the sintering gap with epoxy prepreps.

For 500W power modules, which were manufactured using this approach, solder reflow testing and active power cycling results will be discussed in detail.

Additionally the development work toward the realization of the 50kW module will be described.

Key words: Power semiconductor packaging, embedded components, embedded actives and passives, PCB technology, System in Package, power electronics, silver sintering

INTRODUCTION

A significant increase in commercial products, which use embedded die technologies, can be observed over the last years. By embedding active power semiconductors into PCB like structures, the length of the signal lines and the thermal path can be reduced. In addition, by eliminating the wire bonded interconnections and replacing them by direct copper connections, parasitic impedance can be reduced

remarkably which yields in an improved switching behavior and reduced switching losses [2].

The so called power core provides the base for the package/module. This power core contains the embedded semiconductor(s) and is manufactured using printed circuit board processing on a large panel format of 18 by 24 inches. Electrical contacts to the embedded dies are made by laser drilled micro vias and copper filling. Additionally, the use of this panel format offers the possibility of parallel processing during the manufacturing of the packages/modules.

Three different power classes be addressed in the EmPower project.

A 50W fast Schottky rectifier diode will be the simplest package, demonstrating the capability in thickness and form factor reduction. The realized version will be comparable to the conventionally used D²Pak, realizing the same footprint. The conventional package will be used as benchmark.

The 500W module is a MOSFET B6 bridge, for an electric bicycle (PEDELEC) application. By embedding the MOSFET, about 50% of space reduction for the switching elements can be achieved and in addition a double sided cooling of the semiconductors is possible.

The 50kW module represents a 3-phase automotive power inverter. This module consists of 8 IGBT and freewheeling diodes per phase, embedded into a power core structure and sandwiched between to IMS substrates. In total 48 semiconductor dies will be embedded for this application example.

THE EMPOWER PROJECT

With the funded European Project “EmPower” in the frame of CATRENE (Cluster for Application and Technology Research in Europe on Nanoelectronics) academic and industrial players formed a consortium with the goal to develop the next generation of embedded power packages and power modules.

The structure the EmPower consortium forms the complete supply chain starting from wafer supply, wafer plating, wafer back end, die embedding and module assembly to

realize power packages, and power modules with embedded components, specified by the participating end users (Figure 1). The EmPower project is a follow-up project of the highly successful HERMES Framework 7 funded European Union project.

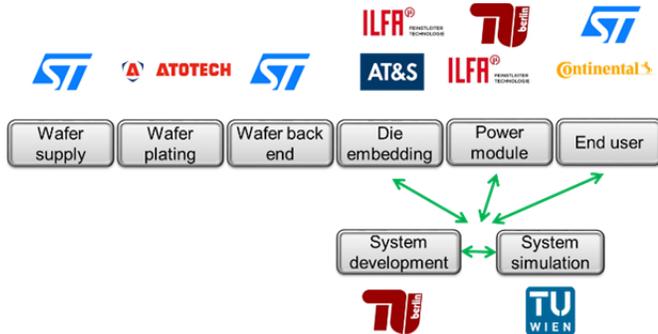


Figure 1: EmPower project consortium

50W SCHOTTKY DIODE PACKAGE

Concept and process flow

In order to compare the power core based approach package with an existing package, the D²PAK package from STM (ST Microelectronics) was chosen (Figure 2).

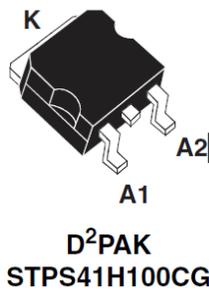


Figure 2: Schematic of the D²PAK package (Source: STM datasheet)

To use the same test environment, the embedded package was designed to realize the same footprint. As a result of that, the x and y dimension was not reduced, but the package height was shrunk significantly to around 625µm compared to the D²PAK with around 4.5mm. If an x and y optimization would be applied, an additional approximately 50% area reduction would be possible.

The manufacturing process flow is based on bare dies, which have a double sided copper metallization of their contact pads. This copper metallization is required in order to create the contact areas by laser drilled micro via and copper metallization.

The process sequence (Figure 3) is based on a prelaminated substrate. This substrate consists of a structured FR4 core, containing the openings for the Schottky diode dies, a thin prepreg and a copper foil.

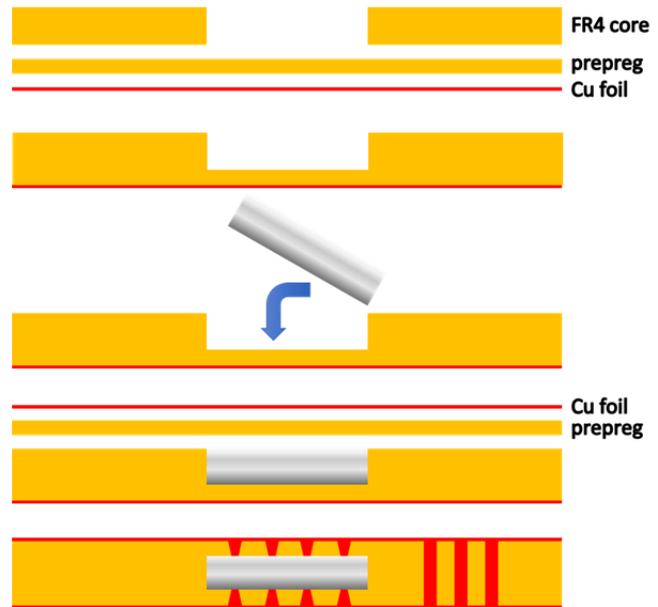


Figure 3: Process flow for double sided Cu micro via connection

This stack will be prelaminated to a substrate. During the lamination, the prepreg layer only acts a “glue” layer and will not be fully cured. Into this substrate the silicon dies will be assembled. The created cavities in the FR4 core determine the position of the die, and are required to be as accurate as possible.

After die assembly, additional layer of structured and full area prepreg and copper foil is laid up. The embedding is done by lamination in a standard multi-layer press.

Using this layout, a fully symmetric build up realized, having the dies centered in the middle of the core.

In order to create the electrical contacts to anode and cathode of the embedded die, micro vias are drilled with a UV laser drilling process. Additionally the routing of the anodes from the front to the backside of the substrate requires mechanical drilling of through holes. Followed by that, copper metallization of the vias is done. Finally the routing and footprint is structured by lithography and etching.

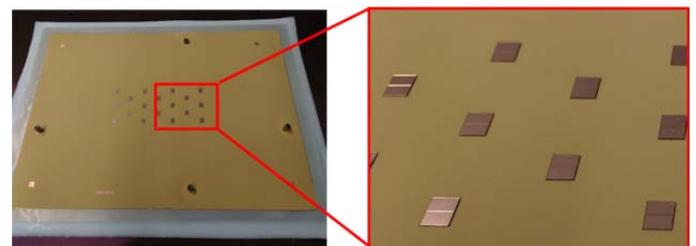


Figure 4: Placement of dies

Figure 4 shows the placement of the dies into the prelaminated substrate prior to the final layout of the prepreg and copper foil.

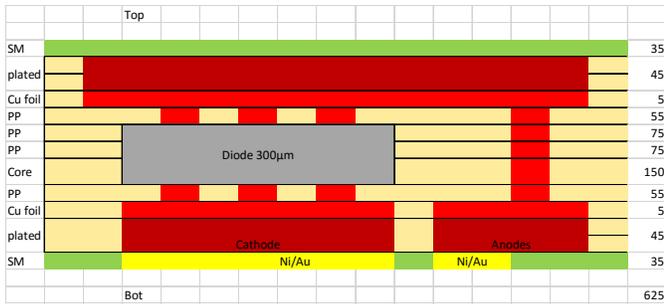
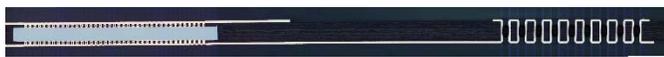
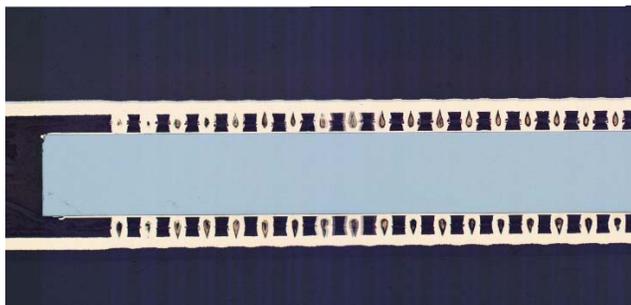


Figure 5: Build up of Schottky diode package

In Figure 5 the schematic build up is illustrated. As visible in the sketch, the structure is design to create a fully symmetric build up, yielding in ideal thermo-mechanical properties.



Overview



Double-sided micro via to embedded die



Through hole contacts

Figure 6: Cross section 50W package

Figure 6 shows the cross section of the 50W package. It is visible, that an excellent symmetry was achieved using the designed build up. The double sided copper connections are equally formed on both sided of the die. Some voiding in the filled micro via appears, which is a result of a slightly too high aspect ratio of the micro via, causing these plating appearance, which can be easily adapted.

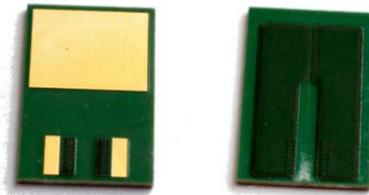


Figure 7: 50W Schottky diode package

Figure 7 illustrates the ready package, front and backside. In total around 220 packages were manufactured in a first run. A part of these are currently used for electrical characterization at STM.

Another part of the packages has started reliability testing right now. First step is the reflow soldering test followed by high temperature storage, temperature humidity storage and passive thermal cycling.

MSL3 Reflow test

Reflow soldering test is done according to JESD22-A113-E and moisture sensitivity level (MSL) 3. Of main interest here is the behavior of the interfaces within the package.

The test is done like described in the following

Preconditioning:

Temperature cycling: 5 cycles -40°C/60°C
 Dry bake: 24h, 125°C
 Moisture soak for MSL 3: 192h, 30°C/60%RH

Reflow test:

3 times Pb-free reflowing (peak 260°C), between 15 minutes and 4 hours after removal from the humidity chamber.

Results:

No outside delamination of the package is visible after the reflow test.

The cross sectioning of the packages after reflow show the following results: No delamination between the epoxy material and the die can be detected. There is also no evidence of any other interface problems. Micro via to the embedded die, copper metallization of vias and the routing does not show any delamination from the epoxy material (Figure 8 and Figure 9).



Figure 8: 50W package after MSL3 testing / through holes

embedded approach) and connectors will be assembled to the surface.

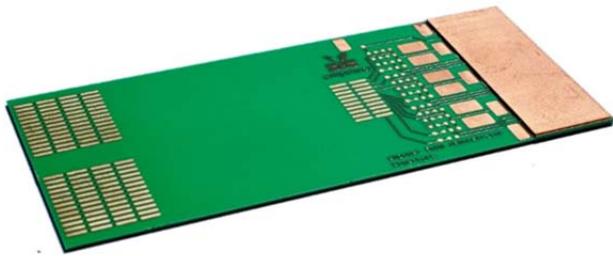


Figure 13: 500W PEDELEC module

Reflow soldering test

In order to test the reflow behavior of the complete module, consisting of top and bottom IMS, Ag sintered to the power core with the embedded MOSFETs, again reflow soldering tests have been performed according to JESD22-A113-E and moisture sensitivity level (MSL) 3 was applied.

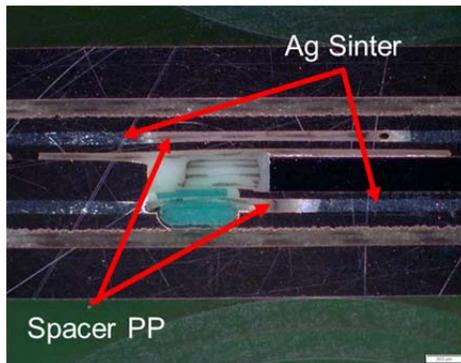


Figure 14: Cross section after MSL3 test

TOP IMS

Power Core

BOT IMS

observed between the solder mask material of the power core and the IMS to the filling prepreg and the solder mask material within the IMS. Additionally, delamination of the spacer prepreg from the copper of power core and IMS to the spacer prepreg is visible. In order to eliminate these failures, a complex DOE of in total 8 different process variations was created and performed. Remark: The visible delamination MOSFET die/embedding prepreg is addressed at component preparation level and will not be discussed in this paper.

Adhesion improvement DOE

The DOE incorporated the methods of Cu surface preparation of power core and IMS, the filling material to level the surfaces of power core and IMS as well as the build up materials itself. Also the method to prepare the module for removal of the not needed part of the top IMS was investigated.

As a result the following statements can be made:

- Sufficient adhesion promotion of the involved copper surfaces is of paramount importance. The different tested chemical treatments yielded in similar results.
- The elimination of solder mask material in the laminated areas does yield in an excellent adhesion of the spacer prepreg to the new leveling material
- No influence of the build up materials was found

In Figure 16 the cross section of an example from the DOE after reflow testing is shown. All interfaces, which were identified critical in the first MSL3 testing, remain defect free. No delamination of the spacer prepreg or the leveling material was detected. Also the filling of the gaps by the resin of the prepreg appears without any voiding.

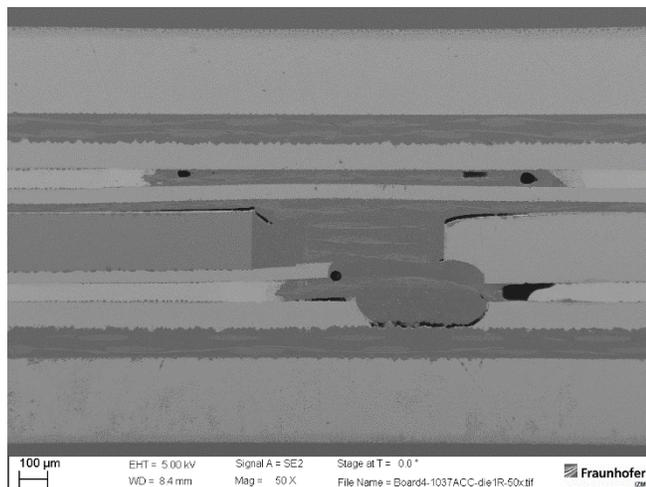


Figure 15: SEM of cross section after MSL3 test

The analysis of the cross sections of the tested modules (Figure 14 and Figure 15) gives a detailed impression. Both pictures do not show any evidence of delamination within the Ag sinter interconnection structure between IMS and power core. Ag sinter layer, and its interfaces remain intact after the test. On the other side, a delamination can be

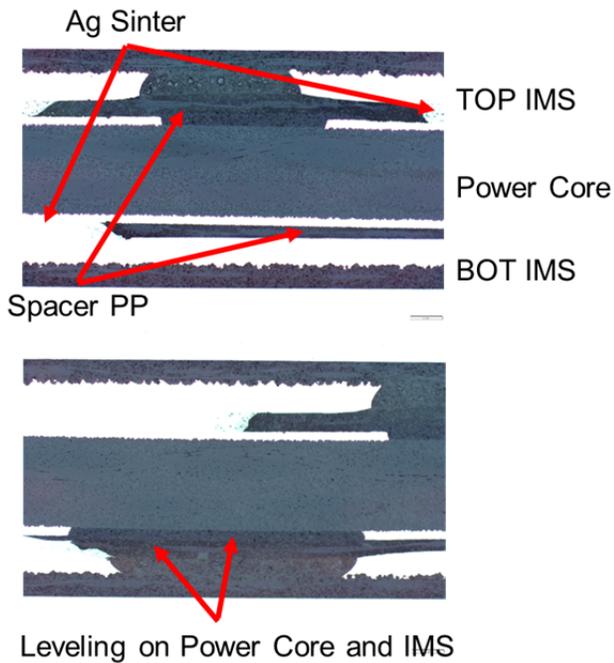


Figure 16: Cross section of MSL3 tested 500W module, adhesion improved

As the result of the DOE, a process sequence and parameters were determined, which a guarantee a reliable module manufacturing

Active Power cycling of power module – B6 bridge

Active power cycling is an important test for power electronic components and modules.

First power cycling tests were performed on module level. The test setup is illustrated in Figure 17 and Figure 18. The high current connection is made to the common drain connection of the high and low side FETs and the short-circuited phase connection of the module. By that, the high and low side FET will operate in parallel mode during the test.

A double sided cooling in the area of the embedded semi-conductors is attached to the module. The temperature of the cooler is set to 18.5°C resulting in a $T_{j,min}$ of 20°C.



Figure 17: Power cycling tester

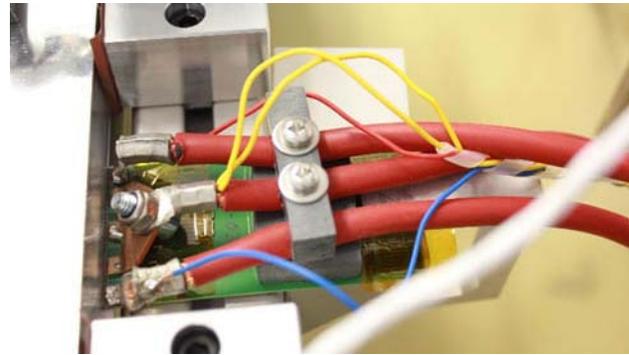


Figure 18: Power cycling test setup

For monitoring the junction temperature during the active power cycling, the internal reverse diode is calibrated at different temperatures prior to starting the test. Followed by that, the test parameters are setup. The goal is to realize a temperature swing of 100 K with each active cycle. For this purpose a current flow of 32 A for a duration of 3 sec is required. Cooling down to 20°C is realized by switching off the current for 6 sec. It needs to be mentioned, that due to the configuration of the module, the high side dies do only realize a temperature swing of 60 K whereas the low side dies reach 100 K. This effect is caused by the configuration of the FETs in the module and the resulting different thermal paths.

The test criteria is, that an increase of the forward voltage of 20% is defined as a module failure. The test was terminated at around 310.000 active power cycles passed, without any noticeable increase of the forward voltage. Compared to a wire-bonded module, which typically reaches around 100.000 cycles to failure, this test provides an excellent result and a significant improvement in active power cycling reliability.

50kW DC/AC inverter

The concept of the 50kW module is similar to the 500W module. The main difference is different configuration of the IMS substrates, with higher copper thickness in order to achieve a good heat spreading of the thermal losses of the IGBT and diodes.

Therefore, a configuration for the IMS of 1mm copper / 100µm thermal prepreg / 300µm copper was chosen. Between the top and bottom IMS the power core, containing the embedded IGBT and diodes, is placed again (Figure 19). The manufacturing of the module is similar to the 500W module:

- Application of immersion Ag layer
- Stencil printing of Ag sinter paste
- Layup of spacer prepreg
- Sintering in multi-layer press

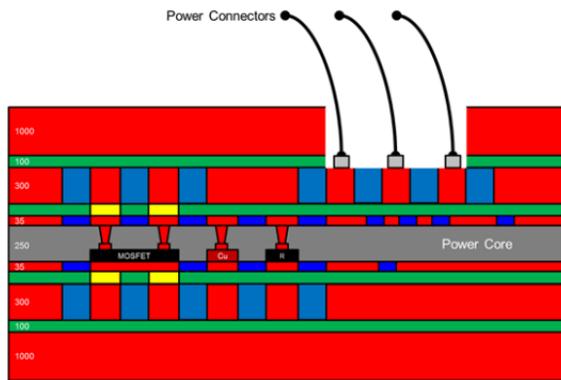


Figure 19: Schematic of 50kW module

In contrast to the 500W module, for the 50kW module the complete top IMS will remain on top of the module. Therefore the high current connectors must be exposed to access them after sinter lamination. This will be done by a depth milling into the 1mm thick copper of the top IMS. The remaining thermal prepreg material will be selectively removed at the high current connectors only.

Currently the first test vehicles are manufactured, and are used to setup and optimize the process sequence. In Figure 20 a first result of this manufacturing run is shown. The total thickness of the module is about 3.3mm and the high current connectors are visible in the middle opening.



Figure 20: Example of 50kW inverter module

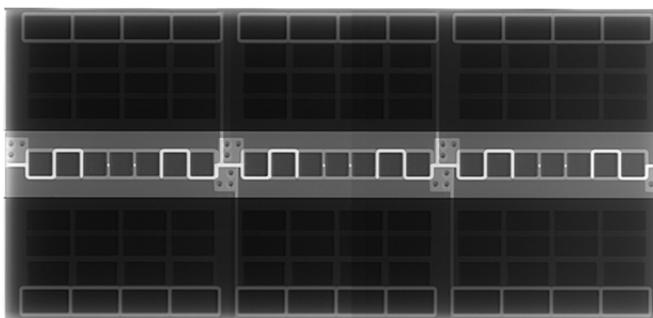


Figure 21: x-ray of 50kW module

Figure 21 shows a first x-ray analysis of the module. The first manufactured modules show promising results, demonstrating, that the method for finalizing the modules can be transferred from the 500W demonstrator. Currently a detailed analysis, in order to detect potential areas for

improvement in the processing, is done. Furthermore, MSL3 reflow testing is currently under way.

CONCLUSION

The presented work within the EmPower project, demonstrates continues development of a new concept in the embedded die technology for power electronic packages and modules. The development work of all three different addressed power classes is described in detail.

For the 50W Schottky diode package a new process flow was developed and successfully applied to create fully symmetric, single die packages. First reliability testing proves the robustness of the developed technology.

For the 500W and 50kW modules the focus of work lies on the sinter lamination technology, which is applied for module finalization, enabling improved thermal management, by providing the option of double sided cooling, and realizing the high current connections to the module.

For all three application areas functional test vehicles were realized or are currently underway. A full reliability assessment will be applied to all of the demonstrators, to demonstrate the robustness of the developed technologies.

ACKNOWLEDGEMENTS

The authors would like to thank the German “Federal Ministry of Education and Research” for their financial support the “EmPower” project (FKZ 16EK0016), which is also supported in the European “Catrene” program (CT315 – EmPower).

Additionally they would also like to thank the partners within the “EmPower” project:

Johannes Blum from ILFA GmbH, who provided the input on the IMS manufacturing to this paper. ILFA provides all required IMS substrates for the development work and demonstrator manufacturing in the project.

Mike Morianz and Hannes Stahr from AT&S for their input on the power core manufacturing for the 500W and 50kW demonstrator.

ATS provides all required power core substrates for the development work and demonstrator manufacturing in the project.

REFERENCES

- [1] <http://catrene-empower.ats.net/>
- [2] Eckart Hoene, Andreas Ostmann, Binh The Lai, Christoph Marczok, Andreas Müsing, Johann Walter Kolar, "Ultra-Low-Inductance Power Module for Fast Switching Semiconductors", PCIM Conference 2013, Nuremberg, Germany.
- [3] Lars Böttcher, Stefan Karaszkievicz, Dionysios Manassis, Andreas Ostmann, “Development of

Advanced Embedded Die Modules for Power
Electronics Applications”, SMTA International
Conference, Rosemont/USA, Sept 27 – Oct 01, 2015