

THE COMBINED EFFECT OF ASSEMBLY PITCH AND DISTANCE TO NEUTRAL POINT ON SOLDER JOINT THERMAL CYCLING LIFE

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ABSTRACT

Cycles-to-failure versus Distance to Neutral Point (DNP) data for SnPb and lead-free assemblies under Accelerated Thermal Cycling (ATC) conditions are observed to follow three main trends: 1) no DNP dependence; 2) a power-law dependence with an exponent near -1; 3) a power-law dependence with an exponent close to -2. The first two trends are at a significant departure from standard Coffin-Manson types of models for SnPb and lead-free assemblies (e.g., IPC 9701). Deviations of DNP test data from the standard models can be significant and have serious implications for board designers: a) solder joint life based on Coffin-Manson type of models may be under-estimated by a large factor - and packages rejected - for new designs using a larger die or package; b) moving to smaller die or packages, the existing models may over-estimate the reliability gains associated with smaller size components. This leaves board designers with significant uncertainties and reliability risks. This paper resolves the above differences by means of a simple strength-of-materials model that provides physical and quantitative insight into the combined effect of assembly pitch and DNP on thermal cycling life. The pitch, which affects the stiffness of the assembly, is a significant factor that is not accounted for in standard models. The proposed "pitch and DNP" life model accounts for the pitch stiffness effect and is validated against numerous ATC datasets.

INTRODUCTION: CYCLIC LIFE VS. DNP TRENDS

Chip or component sizes are widely recognized as solder joint life limiting factors under thermal cycling conditions. Standard life models (e.g., Goldmann, 1969; Engelmaier, 1984, 2008; IPC9701) give cycles to failure, N_f , as a function of the maximum DNP at critical corner joints in the form of an inverse power-law:

$$N_f \propto 1/DNP^m \quad (1)$$

where m is referred to as the Coffin-Manson exponent.

In Goldmann, 1969 - the companion paper of the Norris-Landzberg, 1969 paper where the DNP effect was not laboratory tested¹ - m is quoted at 1.9 for high Pb solders. In Engelmaier, 1983, 2008 and IPC9701, the exponent m is a function of the mean cyclic temperature and the dwell

time at the temperature extremes. The exponent m goes from about 2 to 2.8 for near-eutectic SnPb and from 2.2 to 3.2 for lead-free Sn-Ag-Cu (SAC) alloys and dwell times greater than 5 minutes. Graphs of the m exponent as a function of dwell time and mean cyclic temperature are plotted in Figure A.1 in Appendix, for mean temperatures in the range -25°C to 75°C and dwell times greater than 5 minutes. To this author's knowledge, the life vs. DNP equation (1) with the m exponent of Engelmaier's models was not tested against devices of variable sizes. The SnPb version of the model was fitted to isothermal mechanical fatigue data where the control variable was the cyclic shear strain range in lap-shear experiments by Wild, 1971. Isothermal lap-shear specimens do not have a DNP dimension per se since the concept of DNP relates to the thermal expansion of parts, chips and components. While the standard models give the exponent m in the approximate range 1.9 to 3.2 for different solder compositions and test conditions, ATC test results from throughout the literature tell a different story. The data shows three main patterns of cycles-to-failure vs. DNP:

- Little to no DNP effect, as shown in Figure 1 for maximum DNP's that are less than 21.5 mm.
 - The SnPb data from Amick et al. (1993) is average cycles to failure for 50 mil pitch, 20 to 84 I/O ceramic chip carriers on "CTE-matched", kevlar boards, i.e. for test vehicles with a very small in-plane (global) CTE mismatch between board and components.
 - The SAC305 data from Gatza et al. (2012) is characteristic lives from a large, 1 mm pitch BGA assembly with eight independent daisy chains per device. The in-plane CTEs of the BGA and of the test board were 12.3 ppm/°C and 13-14 ppm/°C, respectively. The global CTE mismatch was small (0.7 to 1.7 ppm/°C). For daisy-chained solder joints with a maximum DNP less than 21.5 mm, cycles to failure are DNP independent. The DNP effect picks up and cycles to failure drop off as the DNP increases past 21.5 mm.

In the region of little to no DNP effect, solder joint failures are driven by local CTE mismatches (Clech et al., 1990), that is, CTE mismatches between the solder alloy and the board and components across the soldered pad areas. Strain energy models (e.g. Clech, 1996, 2005) that give cyclic strain energies due to global and local CTE mismatches allow for an upfront assessment

¹ "All of the experiments to verify the solder fatigue model were performed using a 112-mil chip with 23 controlled collapse interconnections", Norris-Landzberg, 1969.

of the relative damage due to either type of “stress”. In the rest of the paper, the analysis of reliability data focuses on test vehicles where global CTE mismatch is the dominant driver of solder creep / fatigue failures.

- For the four datasets in the left half of Figure 2, cyclic life decreases when the maximum DNP increases, with power-law exponents m in the range 0.77 to 1.11. Standard deviations on these median values of the exponent m are as large as 0.45. The median values are close to 1, and are quite different from what would be expected from standard models. The test devices were of Wafer Level Chip Scale Package (WLCSP) assemblies and failures were confirmed as solder fatigue failures.
- For the two datasets (Meilunas et al., 2011) in the right half of Figure 2, cyclic life decreases when the maximum DNP increases, but much faster than in the previous case, with power-law exponents m in the range 2.29 to 2.39. These values are in the range of Engelmaier’s m exponent. In Meilunas et al.’s experiment, the components are silicon die sandwiched in between two organic substrates. The components have an area array format with 64 I/Os (8 x 8) and the maximum DNP increases with the assembly pitch (1, 1.4 and 1.8 mm).

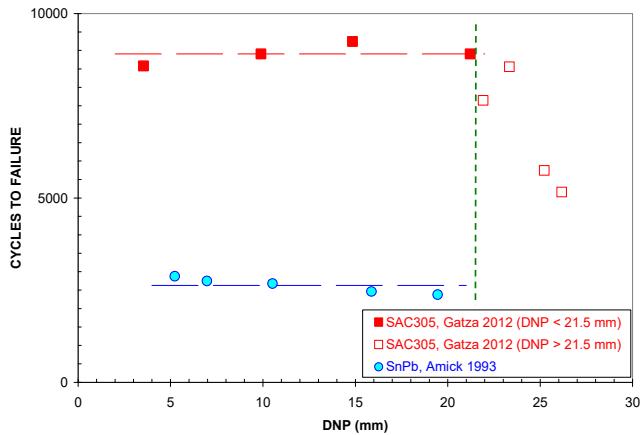


Figure 1: Log-linear plot of cycles to failure vs. DNP for datasets showing little to no DNP effect for DNPs less than 21.5 mm.

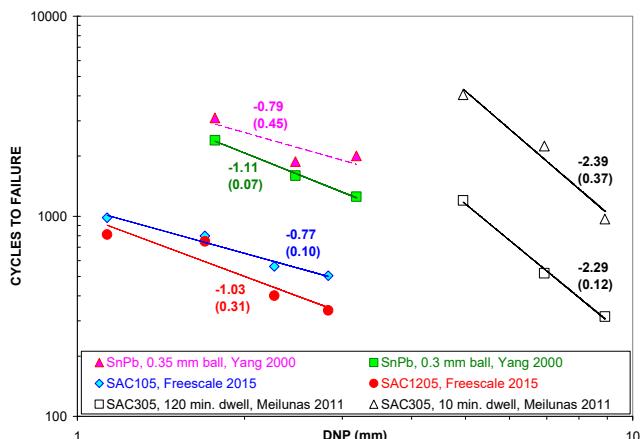


Figure 2: Log-log plot of cycles to failure vs. DNP where cycles to failure decrease when the DNP increases.

Numbers next to fitted lines are exponents of power-law trendlines, followed by standard deviations in parenthesis.

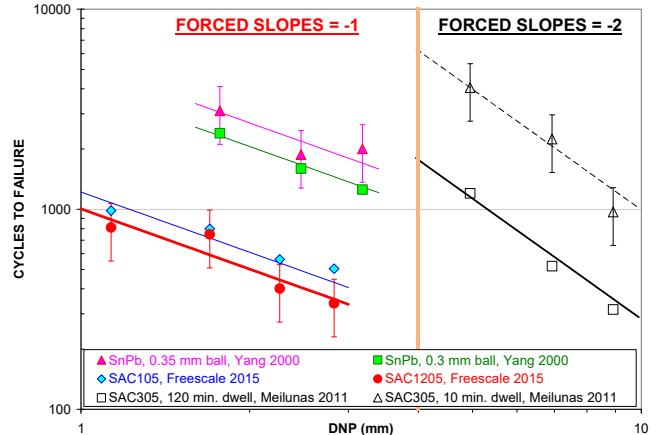


Figure 3: Log-log plot of cycles to failure vs. DNP for the same datasets as in Figure 2 but with trendlines having forced slopes of -1 for datasets on the left side of the graph, and slopes of -2 for those on the right side of the graph.

Figure 3 is a log-log plot of the same datasets as in Figure 2 but with trendlines having forced slopes of -1 (datasets to the left) or -2 (datasets to the right). Error bands have been added in for datasets showing the most scatter around the trendlines. The error bars on cycles to failure are +/- 32%, based on lower and upper bound values of characteristic lives at the 90% confidence level (see Figure A.2 in Appendix). The point is that trendlines with forced slopes of -1 or -2 capture the life cycle vs. DNP data within the lower and upper bound margins of error that are typical of solder joint characteristic lives under ATC conditions.

Other experiments confirm the seemingly unexpected trends of Figures 2 and 3, some of which will be discussed later on in this paper. The main objective of this study is to provide insight as to why the slopes of life vs. DNP trendlines deviate so much from standard model predictions. The proposed physical model, based on a simple strain energy approach, is presented next. The model predicts the exact same slopes (-1 or -2) of the power-law trendlines that are forced through the datasets in Figure 3. A key ingredient of the model is the assembly pitch, a parameter that is not accounted for in standard models. The proposed model is validated against independent test results in the latter part of the paper.

PITCH AND DNP LIFE MODEL

Geometric Parameters

Consider an $n \times n$ area-array of pads of pitch P as illustrated in Figure 4. The cross-diagonal length from one outermost corner pad to the opposite corner pad is:

$$2 \cdot DNP = (n-1) \cdot P \cdot \sqrt{2} \quad (2)$$

An area array land-pattern is usually specified by the pitch and the number of I/Os on the side of the array. For modeling purposes, and because the three parameters n , P and DNP are related by equation (2), we select the pitch P and the maximum DNP as independent variables of the

model. The life model is thus formulated in terms of physical parameters that enter the formulation of solder joint stresses, strains and strain energy density per cycle.

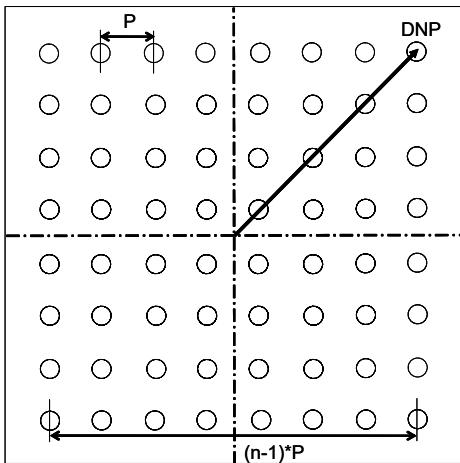


Figure 4: Area-array parameters: $n \times n$ pads ($n = 8$ in the shown example), P = pitch, DNP = maximum distance to neutral point at critical corner joint.

Rough First Order Approach²

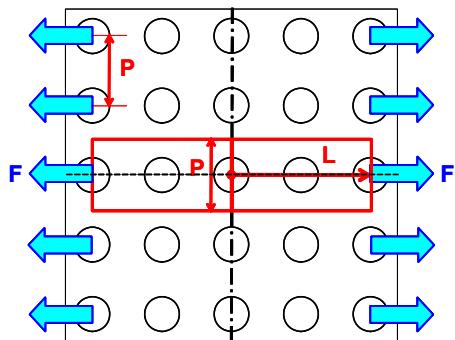


Figure 5: Area-array component with solder joint shear forces F acting on half-strips of width the pitch, P . The length L represents the critical “DNP” in the “rough” model.

To simplify the derivation of the life model, consider the thermal expansion of the component in one direction only, the horizontal direction of Figure 5. Solder joints on the left and right hand sides of the array are subject to the same shear forces F . These shear forces act as in-plane tensile forces that are exerted on component strips of width the pitch P and length L (the dimension that is equivalent to the DNP). The half-strips, from the symmetry axis to the outermost pads have a tensile stiffness $K = E * A / L$, where $A = \text{Pitch } (P) \times \text{Component Thickness } (t)$ is the cross-section of the half-strip perpendicular to the plane of Figure 5. Poisson ratio effects are neglected in this first order formulation. From classical mechanics, the stiffness of a tensile bar of length L and cross-section $A = P \cdot t$ is:

$$K = E \cdot (P \cdot t) / L \quad (3)$$

Since the component pad moves by an amount $L \cdot \Delta \alpha \cdot \Delta T$ relative to the board ($\Delta \alpha$ = global CTE mismatch, ΔT = temperature swing), the tensile force exerted on the strip of width P is:

$$\begin{aligned} F &= K \cdot (L \cdot \Delta \alpha \cdot \Delta T) \\ &= [E \cdot (P \cdot t) / L] \cdot (L \cdot \Delta \alpha \cdot \Delta T) \\ &= E \cdot (P \cdot t) \cdot \Delta \alpha \cdot \Delta T \end{aligned} \quad (4)$$

Note that the DNP or length L drops out in the second line of equation (4). That is, the DNP contribution due to the thermal expansion differential disappears because of the elasticity of the component, with the stiffness of the half-strip going as the inverse of its length.

Next, since the shear force F displaces the top side of the joint by the amount $L \cdot \Delta \alpha \cdot \Delta T$ relative to the board, the amount of work produced by that force is force times displacement:

$$\begin{aligned} \Delta W &= F \cdot (L \cdot \Delta \alpha \cdot \Delta T) \\ &= [E \cdot (P \cdot t) \cdot \Delta \alpha \cdot \Delta T] \cdot (L \cdot \Delta \alpha \cdot \Delta T) \\ &= (E \cdot t) \cdot (P \cdot L) \cdot (\Delta \alpha \cdot \Delta T)^2 \end{aligned} \quad (5)$$

The cyclic strain energy imparted to solder joints thus goes as:

$$\Delta W \propto (P \cdot L) \cdot (\Delta \alpha \cdot \Delta T)^2 \quad (6)$$

Since the cyclic life of soft solder joints goes as the inverse of the strain energy density per cycle (e.g., Clech, 1996, 2005), cycles to failure go as:

$$N_f \propto \frac{1}{(P \cdot L) \cdot (\Delta \alpha \cdot \Delta T)^2} \quad (7)$$

This life model differs from standard models in three ways:

- Cyclic life is inversely proportional to the maximum DNP, L . The DNP effect is not squared because of the elasticity of the component, whereby the stiffness of the half-strip in Figure 5 goes as $1/L$.

² Readers who are only interested in the results can skip the model derivation and go directly to the life model equation (14). The step-by-step derivation of the model will be of interest to those who wish to understand why the pitch matters and what the *pitch stiffness effect* is.

- Cyclic life goes as the inverse of the pitch, P . The pitch appears in the model because of the elasticity of the component, as seen in equation (3) for the stiffness of the half-strip of width the assembly pitch. In other words, everything else being equal, a smaller pitch leads to a longer life because narrower component strips of width P (Figure 5) are more compliant than wider strips. However, the pitch effect alone has to be pondered by pad and joint size effects since smaller pitch assemblies may call for smaller pad sizes. The pad size effect is not covered in this paper.
- The CTE mismatch, $\Delta\alpha$, and temperature swing, ΔT , effects are exactly squared.

The above properties of the model are validated against the data of Figures 2 and 3, and additional, independent test results in the “Model Validation” section of the paper. This includes validation of the CTE mismatch and temperature swing effects being exactly squared. The analytical derivation of the model in the following sub-section leads to the same form of the model as given by equation (7) with the effect of solder joint height added in for thin joints.

Analytical Approach

From equation (3) in Clech et al., 2009, the maximum possible strain energy density per cycle is:

$$\Delta W_{\max} = \kappa \cdot g_0^2 \cdot \Delta T^2 \quad (8)$$

where:

- g_0 is the shear strain per degree of temperature rise:

$$g_0 = \frac{L}{h_s} \cdot \Delta\alpha \quad (9)$$

L is the DNP of interest, $\Delta\alpha$ is the global CTE mismatch, h_s is the solder joint thickness or component stand-off height.

- κ is the slope of isothermal stress reduction lines in the shear stress / shear strain plane where hysteresis loops are drawn (see Figure 1 in Clech et al., 2009). From equation (4) in Clech, 1996:

$$\kappa = \frac{K \cdot h_s}{A_p} \quad (10)$$

where:

- K is the assembly stiffness on a pitch basis. It accounts for elastic deformations (board and component stretching and bending) of a slice of the assembly of width the assembly pitch. K is a function of board and component properties and thickness, the pitch and the maximum DNP of interest, L . From the stiffness equations - (3a-d) for single-sided boards and (4) for double-sided assemblies in Clech, 2015 - and leaving the properties and thickness of the board and component out, K goes as:

$$K \propto \frac{P}{L} \quad (11)$$

- A_p is the minimum solder joint load bearing area in shear, that is, the minimum solder joint cross-section

parallel to the board. In most cases, A_p is also the solder joint crack area, or fracture surface area, for an electrically open, fully cracked solder joint. When failures occur on the component side of solder joints, A_p can be approximated by the component pad area.

By combining equations (8) to (11), and leaving out: 1) the crack area A – the effect of which will be addressed in a future publication, and 2) the board / component properties and thickness whose effects were addressed in Clech, 2015, the maximum strain energy density per cycle goes as:

$$\Delta W_{\max} \propto \left(\frac{P}{L} \cdot h_s \right) \cdot \left(\frac{L}{h_s} \cdot \Delta\alpha \right)^2 \cdot \Delta T^2 \quad (12)$$

$$\text{or: } \Delta W_{\max} \propto P \cdot \frac{L}{h_s} \cdot (\Delta\alpha \cdot \Delta T)^2 \quad (13)$$

Thus, cycles to failure go as:

$$N_f \propto \frac{1}{\left(P \cdot \frac{L}{h_s} \right) \cdot (\Delta\alpha \cdot \Delta T)^2} \quad (14)$$

The pitch, P , as it appears in the above life model, originates in the formulation of the assembly stiffness, K (equation (11)). We thus refer to its effect on life as the *pitch stiffness effect*, separate from its effect on the maximum, critical DNP, L , as in equation (2).

For single-sided boards, equation (14) assumes thin joints with the joint thickness being much smaller than half of the board thickness plus half of the component thickness. The reason for this is that the joint thickness appears within a parameter $H = h_B/2 + h_s + h_C/2$ in the bending stiffness equation (3d) in Clech, 2015, where h_B is the board thickness and h_C is the component thickness. H represents the distance between the board and component’s neutral planes. The thin joint approximation is easily lifted off by combining the present “pitch and DNP” model with the “board thickness” model in Clech, 2015. The above approximation is not an issue for double-sided boards (i. e. mirrored assemblies) since their bending stiffness is infinite and the above parameter H does not appear in the formulation of their assembly stiffness, K .

Equation (14) is similar to equation (7) from the rough, first order approach, with the effect of solder joint height added in. Everything else being equal, equation (14) predicts that cycles to failure are linear with the solder joint thickness. Supporting data is presented later on in the “Model Validation” section. The height effect as predicted by equation (14) is at a departure from the Engelmaier / IPC9701 model which predicts that cycles to failure go as h_s^m with an exponent m larger than 2. To the best of our knowledge, the height effect per se was not laboratory-tested in Engelmaier, 1984, 2005.

MODEL VALIDATION

Constant Pitch Scenario

The two modeling approaches above lead to the same relationship between cycles to failure, pitch and DNP:

$$N_f \propto 1/(P \cdot L) \quad (15)$$

Everything else being equal (including CTE mismatch, pad sizes, solder joint height and thermal cycling conditions), when the component or array size increases and the pitch is kept constant, equation (15) simplifies to an inverse relationship between cycles to failure and the DNP of interest, L: $N_f \propto 1/L$ (16)

This is the situation – constant pitch - with the test vehicles, components or daisy-chains, and the corresponding test results (cycles to failure vs. DNP) on the left-hand side of the graph in Figures 2. For these four datasets, it is thus legitimate to force the slopes of power-law fitting lines to a value of -1 as shown on the left-hand side of Figure 3.

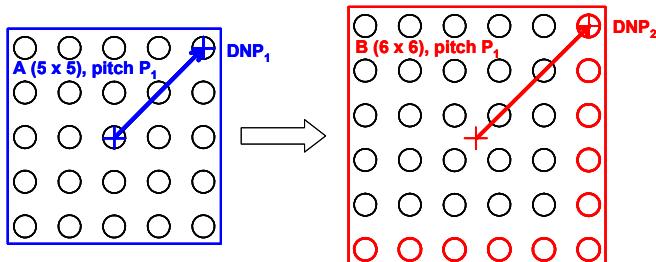


Figure 6: Constant pitch scenario: the pitch, P_1 , is fixed as well as pad sizes. Component or array size increases by adding rows and columns of pads (shown in red). In the shown example, the array size increases from 5 x 5 (component A) to 6 x 6 (component B) and the corner joint DNP increases from DNP_1 to DNP_2 .

Equation (16) applies, in general, to fixed pitch scenarios as depicted in Figure 6. The size of the array increases by adding rows and columns of pads, while keeping the pitch P_1 constant. In the example of Figure 6, the device on the left (A) has $n_1 = 5$ I/Os on each side for a 5 x 5 array. The device on the right (B) has $n_2 = 6$ I/Os on each side for a 6 x 6 array³. According to (16), the ratio of solder joint cyclic lives for the two devices (“A” over “B”) is:

$$\frac{N_{f1}}{N_{f2}} = \frac{DNP_2}{DNP_1} \quad (17)$$

or, by combining equations (2) and (17):

$$\frac{N_{f1}}{N_{f2}} = \frac{n_2 - 1}{n_1 - 1} \quad (18)$$

³ Figures 6 and 7 show three different pad layouts for components labeled A, B and C. In the text of the paper, component parameters, pitch, maximum DNP, number of I/Os on the side and cycles to failure are labeled with subscripts 1, 2 and 3 for components A, B and C, respectively.

In the example of Figure 6, equation (18) gives:

$$\frac{N_{f1}}{N_{f2}} = \frac{6 - 1}{5 - 1} = 1.25 \quad (19)$$

That is, when going from a 5 x 5 to a 6 x 6 array, solder joint life decreases by 25%.

Wafer Level Package Example # 1

Kaysar Rahim et al., 2009, thermally cycled two sizes of wafer level packages (“WLP-C”) with fixed pitch, constant pad diameters and two array sizes: 10 by 10 and 12 by 12. The temperature cycle was from -40°C to 125°C. The ratio of test characteristic lives for the two package sizes was reported as 1.2 (Table 2 in Kaysar Rahim et al., 2009). The model equation (18) predicts a life ratio:

$$\frac{N_{f1}}{N_{f2}} = \frac{12 - 1}{10 - 1} = 1.22 \quad (20)$$

in agreement with the test results of Kaysar Rahim et al.

CBGA Example

In Clech, 2015, we gave a preview of the “pitch and DNP” model, combined with the “board and package thickness” model (see equations 10a-b and Figures 16-17 in section: “BOARD, SUBSTRATE THICKNESS & DNP EFFECT”). The application / validation example was the case of 1 mm pitch, SAC CBGA test vehicles with component sizes 32.5 x 32.5 mm (31 x 31 I/O area-array format) and 42.5 x 42.5 mm (41 x 41 area-array format), and various combinations of board and package substrate thickness after Farooq et al., 2003. The 42.5 mm square CBGAs had a substrate thickness of 1.5, 2.55 or 3.70 mm and were mounted on 1.52 mm thick FR-4 boards. The 32.5 mm square CBGAs had a substrate thickness of 1.50 or 2.40 mm and were mounted on 1.78 mm thick FR-4 boards.

The five cells of ATC (0/100°C) test data by Farooq et al. were found to follow the “1/DNP” cyclic life dependence of equation (16) with a correlation coefficient $R^2 = 0.94$ for two board thickness and three package substrate thickness. This goodness of fit indicates that the combination of the “pitch and DNP” and “board and package thickness” models looks promising. In a fixed pitch scenario, the “1/DNP” cyclic life dependence works for both small (e.g. wafer-level chip scale packages) and large packages (e.g. 42 mm CBGAs).

Fixed I/O Count, Variable Pitch Scenario

Consider two devices, A and C in Figure 7, both with the same number of I/Os (5 x 5 in the shown example), but with different pitches, P_1 and P_3 , respectively. From equation (15), the ratio of solder joint cyclic lives for the two devices (“A” over “C”) is:

$$\frac{N_{f1}}{N_{f3}} = \frac{P_3 \cdot DNP_3}{P_1 \cdot DNP_1} \quad (21)$$

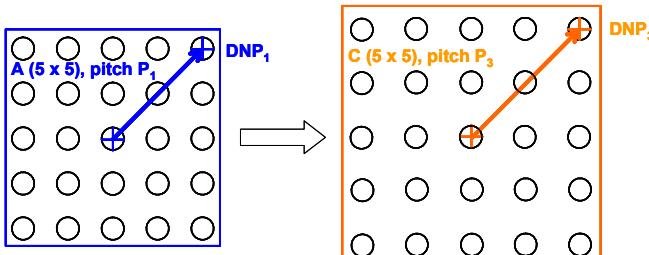


Figure 7: Fixed I/O count, variable pitch scenario: the number of I/Os is constant ($n_1 = n_3 = 5$ for a 5 by 5 array in the shown example). Going from component A to component C, the pitch increases from P_1 to P_3 .

From equation (2), and since the number of I/Os does not change ($n_3 = n_1$ for components A and C), the ratio of DNPs is equal to the ratio of pitches P_3 and P_1 . Equation (21) thus becomes:

$$\frac{N_{f1}}{N_{f3}} = \left(\frac{P_3}{P_1} \right)^2 = \left(\frac{DNP_3}{DNP_1} \right)^2 \quad (22)$$

Equation (22) implies that cycles to failure go as the inverse of the pitch, or the maximum DNP, squared:

$$N_f \propto 1/Pitch^2 \quad (23a)$$

or $N_f \propto 1/DNP^2$ (23b)

Equation (23b) captures the trend of the N_f vs. DNP datasets in the right half of Figure 3, with trendlines having slopes of -2 forced through the data points. For these two datasets that relate to different dwell times in ATC, the number of I/Os was constant ($8 \times 8 = 64$ I/Os). For each dataset, the three data points and the associated DNP values correspond to components with variable pitches of 1.0, 1.4 and 1.8 mm.

Wafer Level Package Example # 2

Kaysar Rahim et al., 2009, thermally cycled 12×12 I/O WLP assemblies with 0.4 and 0.5 mm ball pitch. The ratio of characteristic lives was reported as 1.3, with the 0.4 mm pitch assemblies having longer lives (Table 4 in Kaysar Rahim et al., 2009).

Assuming that pad sizes and solder volumes were identical for the two ball pitches, the present model - equation (22) - predicts a life ratio:

$$\frac{N_{f1}(0.4mm)}{N_{f3}(0.5mm)} = \left(\frac{P_3}{P_1} \right)^2 = \left(\frac{0.5mm}{0.4mm} \right)^2 = 1.56 \quad (24)$$

that is, 20% more than the 1.3 ratio from test results. Confidence bands were not available for the data reported by Kaysar Rahim et al. The 20% difference between test and predicted life ratios remains acceptable given that characteristic lives have median error margins of $\pm 15\%$, possibly as much as $\pm 32\%$ at the 90% confidence level (see Figure A.2 in Appendix). Last, note that standard

models would have predicted a life ratio of 1 since they do not account for the pitch stiffness effect.

Combined DNP and Stand-Off Height Effect

Equation (14) predicts that, everything else being equal, and for devices with a fixed pitch P , cycles to failure go as:

$$N_f \propto 1/\left(\frac{L}{h_s} \right) \text{ or } \frac{h_s}{L} \quad (24)$$

This trend, which is at a departure from standard models, is supported by several examples of ATC test data, three of which are presented below.

Leadless Ceramic Chip Carrier Example

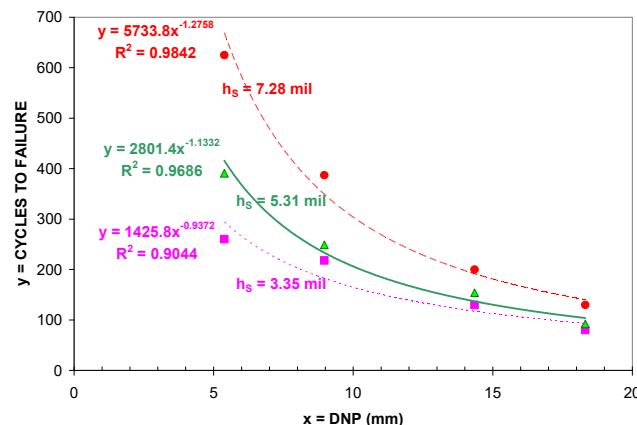


Figure 8: Cycles to failure vs. corner joint DNPs for ceramic chip carriers on printed wiring boards. Each of the three datasets is for a controlled stand-off height ($h_s = 3.35, 5.31$ or 7.28 mil). Test cycles to failure (solid data points) are from Itoh et al., 1982. R^2 's are correlation coefficients for each power-law trendline.

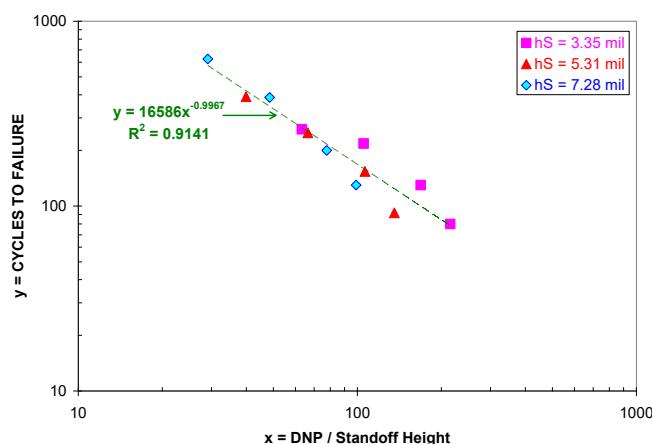


Figure 9: Fig. 8's data re-plotted as cycles-to-failure vs. ratio of DNP to stand-off height ("DNP/ h_s ") on log-log scales. The power-law trendline is across the merged datasets (stand-off height " h_s " = 3.35, 5.31 and 7.28 mil).

Itoh et al., 1982, subjected 50 mil pitch ceramic chip carriers of different sizes on printed wiring boards to harsh ATC

conditions: -65/125°C with 30 minute dwells and 5 minute ramps. The stand-off height between board and components, h_s , was a control variable with settings of 3.35, 5.31 and 7.28 mil. The test cycles to failure from Itoh et al.'s are plotted versus the chip carrier DNP's for each of the three stand-off height values in Figure 8 (using linear scales). For each dataset, a power-law trendline is added in. The three curves for the three different stand-off heights have power-law exponents from -1.27 to -0.93. These exponents are close to -1, as expected from the model (equation (16)) when the component pitch is constant.

The data from Figure 8 is re-plotted in Figure 9 (on log-log scales) as cycles to failure versus the ratio of DNP to Standoff-Height. A power-law trendline that is fitted through the merged datasets gives a slope of -0.9967 with a correlation coefficient R^2 of 0.91. The empirical slope of the cycles to failure vs. the DNP/Stand-off height ratio is very close to the slope of -1 that is predicted by equation (24) for constant pitch scenarios. This time, the "constant pitch" model is validated for peripheral chip carriers as opposed to area-array components in previous examples (Wafer Level Package Example # 1 and CBGA example).

Flip-Chip On Board (FCOB) Without Underfill Example

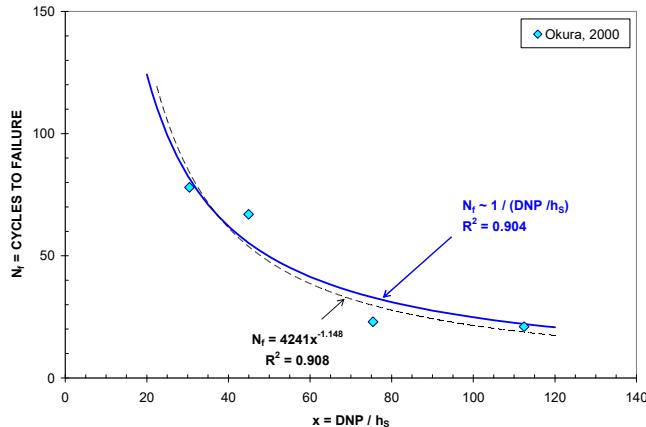


Figure 10: Graph of cycles to failure vs. ratio of DNP to stand-off height: FCOB data points are from Okura, 2000. Empirical power-law trendline (dashed line) gives an exponent of -1.148. The model line (solid blue) with an exponent of -1 from equation (24) fits equally well through the data.

Okura, 2000, cycled FCOB SnPb assemblies without underfill between -55°C and 80°C with 10°C/minute ramps and 5 minute dwells. The design-of-experiment included two chip sizes (5 x 5 mm, 48 I/O and 10 x 10 mm, 112 I/O) and two stand-off heights. The I/O pads were distributed on two peripheral rows with constant, staggered pitch. This gives four data points in the plot of cycles to failure vs. the ratio of maximum DNP to stand-off height in Figure 10. The cycles to failure are from Table 2.3, "Geometry 1" column in Okura, 2000, where "Geometry 1" refers to assemblies with solder mask defined pads on the test board.

Empirical fitting of a power-law trendline through the data gives an exponent of -1.148 and a correlation coefficient $R^2 = 0.908$ (black dashed line in Figure 10). Forcing the present model - equation (24) - through the data points (solid blue line in Figure 10), the correlation coefficient barely changes, $R^2 = 0.904$ for the model vs. 0.908 for the empirical curve fitting. Ohura's FCOB data gives support to the $1 / (\text{DNP}/h_s)$ dependence of cycles to failure under the constant pitch scenario.

MicroSMD Example: Stand-Off Height Effect

Nguyen et al., 1998, tested 14 I/O "microSMD" wafer level chip scale package assemblies under thermal shock conditions (-40/125°C). For stand-off heights of 4.8 and 5.9 mil, and all other parameters being constant, the median cycles to failure were 651 and 750 cycles, respectively ("N50"s in Figure 12 of Nguyen et al.). That is, the test life ratio is: $750/651 = 1.15$.

The present model - equation (24) - predicts a linear relationship between cycles to failure and low stand-off height. For the microSMD assemblies of interest, this gives a predicted life ratio: $5.9 \text{ mil} / 4.8 \text{ mil} = 1.23$, i.e. 6.9% more than the test life ratio. The standard models, with a power-law exponent of about 2 would predict a life improvement of $(5.9 \text{ mil} / 4.8 \text{ mil})^2 = 1.51$ times, that is, 31% more than the test life ratio of 1.15. While a 31% error may be acceptable, the present model prediction is closer to the test life ratio than standard model's predictions.

Combined DNP and ΔT Effect

Equation (14) also predicts that, everything else being equal, and for devices with a fixed pitch P , cycles to failure go as:

$$N_f \propto \frac{1}{L \cdot \Delta T^2} \quad (25)$$

Again, this is at a departure from standard models where both the DNP factor L and the temperature swing ΔT are nearly squared.

Ceramic Chip Example

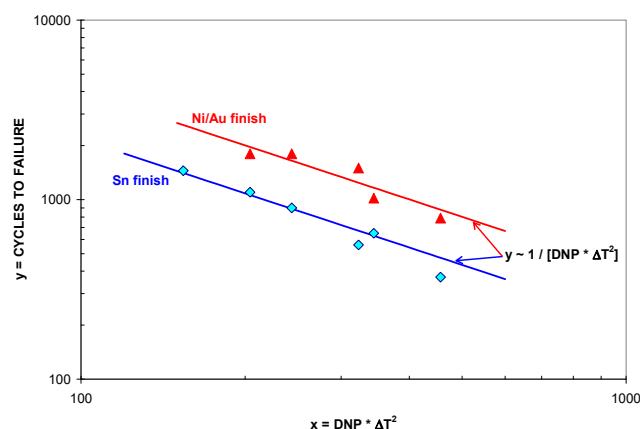


Figure 11: Cycles to failure versus $\text{DNP} * \Delta T^2$ (on log-log scales): data points are for Sn or Ni/Au finish datasets from

Roellig et al., 2007. Model lines (solid blue for Sn and red for NiAu finish test vehicles) are power-law trendlines that are forced through each dataset with an exponent of -1 after equation (25).

Roellig et al., 2007 designed a special test vehicle using ceramic chips on printed wiring boards. The SnAgCu chip assemblies have five joints, one at the center and two pairs of corner joints on opposite sides of the test vehicles. The spacing, or pitch, between adjacent corner joints on one side of the device is fixed at 0.8 mm and the span of the device between the opposite sides of the array of joints varies from 0.8 to 3.2 mm. The test vehicles were thermally cycled under three conditions but we only consider conditions “TCT1” (-40/150°C) and “TCT3” (-40/125°C) that had similar ramp rates, dwell times and cycle duration. That way, the temperature swing ΔT is an independent test variable. The other parameters of the thermal profiles are kept constant so we can test the validity of equation (25) for different DNP’s and ΔT ’s, everything else being equal.

The results of this analysis are plotted as cycles to failure vs. $DNP \cdot \Delta T^2$ in Figure 11 (on log-log scales). The model (equation (25)) is forced through each dataset (Sn and NiAu finish) with a slope of -1. The “forced” model lines follow the test trends well, giving support to the use of the ΔT^2 factor in the model - equation (14) or (25) - for given ramp rates and dwell times.

Global CTE Mismatch Effect

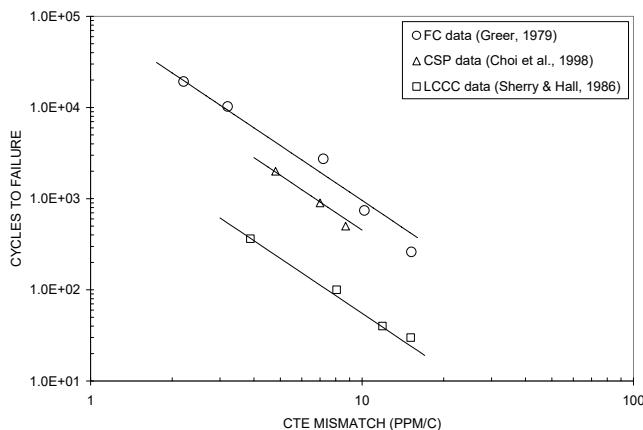


Figure 12: Fit of model to cycles to failure vs. global CTE mismatch data on log-log scales. Power-law trendlines that are force-fitted to the data all have a slope of -2.

For completeness and good measure, the model is also validated for the global CTE mismatch effect:

$$N_f \propto 1/\Delta\alpha^2 \quad (26)$$

Power-law trendlines with a slope of -2 are forced through three datasets of cycles to failure vs. global CTE mismatch on log-log scales in Figure 12. The model fits the data well, even for small CTE mismatches of about 2 ppm/ $^{\circ}$ C. The data is for bare Flip-Chip (FC) assemblies (Greer et al., 1979), Leadless Ceramic Chip Carriers (Sherry & Hall,

1986), and Chip Scale Packages (Choi et al., 1998). To this author’s knowledge, datasets such as these are rare throughout the literature. As much as “CTE mismatches” are talked about, component and board CTEs are not measured in a routine manner, let alone reported. This practice of not measuring CTEs is also at a departure from IPC-9701 guidelines. As a result, many life cycle test results cannot be analyzed in context or interpreted properly.

DISCUSSION: MODEL ASSUMPTIONS

The two main assumptions of the model are:

- The global, in-plane CTE mismatch between board and components is the driving force behind solder fatigue failures. The rationale behind this assumption is that the calculated maximum strain energy density per cycle – as given by equations (6) and (13) – is based on solder joint shear stresses and strains arising from the in-plane thermal expansion differential between board and component only.
- When local CTE mismatches between solder and components or boards are significant, their effect on solder joint life can be addressed by using more detailed strain energy, hysteresis loop models as in Clech, 1996 and 2005.
- Solder joint stress relaxation at the temperature extremes is significant or close to complete. This condition is met when dwell times are long enough, temperatures are high enough and/or the assembly is stiff enough.

Based on validation examples in the previous section of the paper, the above assumptions hold for a variety of ceramic components, flip-chip without underfill and wafer-level chip scale packages mounted on organic circuit boards. Given the above assumptions, the model is thought to be of use for reliability assessment of worst-case components on a product board, i.e., critical components that are likely to fail first because of their large enough size and small enough CTEs compared to the in-plane CTEs of circuit boards.

CONCLUSIONS

- A first order model has been developed that highlights the effect of the assembly pitch on solder joint reliability under thermal cycling conditions.
- Besides determining the maximum DNP at critical corner joint locations, the assembly pitch has a direct effect on the stiffness of a slice of an assembly of width the pitch. Everything else being equal, a smaller pitch makes for more compliant assembly slices that stretch and bend more easily than large pitch slices during thermal cycling.
- As a result of the pitch stiffness effect, solder joint life goes as the inverse of the product of the pitch and the maximum DNP. This is a simple design rule or “rule of thumb” that is of use when considering design changes from one chip size to a different chip size, smaller or larger. Concurrent changes in pad sizes and solder ball diameters, and their effect on solder joint life also have to

be considered. The latter parameters are not factored in the present model. Their impact on solder joint life will be addressed in a future publication.

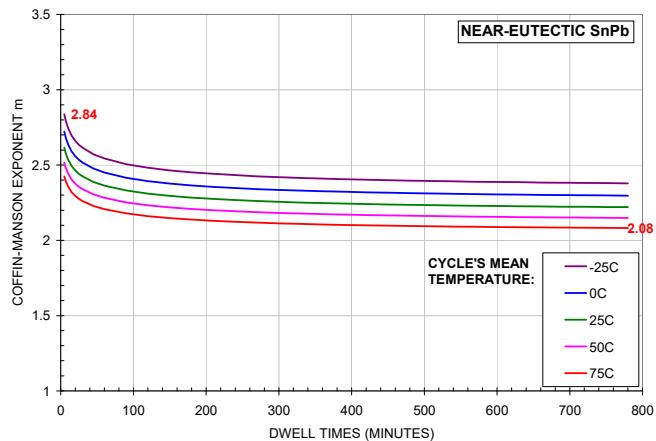
- A consequence of the pitch stiffness effect is that, for assemblies with a fixed pitch, solder joint cyclic life goes as the inverse of the DNP when component size increases. This is at a significant departure from standard models and IPC-9701. The fundamental reason behind this discrepancy is that standard models are based on solder joint fatigue life being strain-range dependent (a la "Coffin-Manson"), whereas the present model is strain-energy based with the assembly stiffness (or compliance) relieving some of the shear strains associated with the thermal expansion differential between board and components.
- The model, including the pitch stiffness effect, is supported by over a dozen experiments as well as SnPb and lead-free test data from independent sources.
- While this paper highlights the pitch stiffness effect in a simplified algebraic model – equation (14) – and with supporting test data, the pitch stiffness effect is not new and is already factored in life prediction models developed by the author for SnPb assemblies (Clech, 1996) and SAC lead-free assemblies (Clech, 2005). The latter models include an assembly stiffness parameter K, and thus the pitch, in the slope of isothermal stress reduction lines that are used to compute stress/strain hysteresis loops during thermal cycling.
- Standard models or modified versions of the standard models that do not include an assembly pitch parameter, and thus do not account for the pitch stiffness effect, should be examined closely and validated against relevant ATC test data prior to use.

REFERENCES

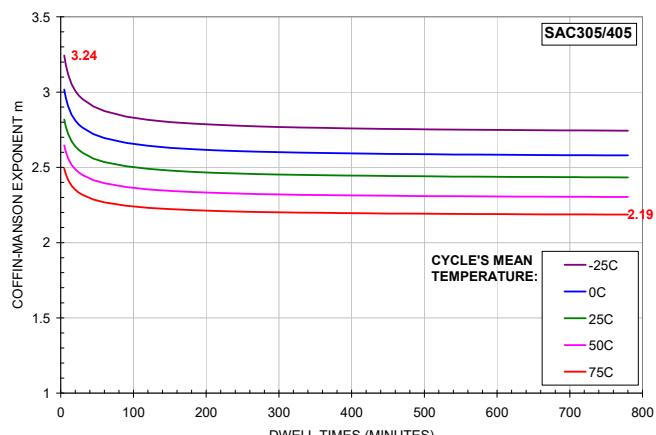
- Amick, P., "Reliability life testing of CTE-compatible surface-mount modules", Proceedings, Nepcon West 1993, Anaheim, CA, February 7-11, 1993, Vol. 3, pp. 1540-1543.
- Choi, K. S., Kim, Y.-G., Choi, S., Park, I.-S., Lee, J.-H. and Ku, J.-Y., "Solder joint reliability of the BLP package", Proceedings, IPC / SMTA Assembly Expo, Providence, RI, October 24-29, 1998, pp. S19-3-1 - S19-3-6.
- Clech, J-P., Langerman, F. M. and Augis, J. A., "Local CTE mismatch in SM leaded packages: a potential reliability concern," IEEE Proceedings, 40th ECTC, Las Vegas, Nevada, May 21-23, 1990, pp. 368-376.
- Clech, J-P., "Solder Reliability Solutions: a PC-based design-for-reliability tool", Proceedings, Surface Mount International Conference, SMTA, 1996, pp. 136-151.
- Clech, J-P., "Acceleration Factors and Thermal Cycling Test Efficiency for Lead-Free Sn-Ag-Cu Assemblies", Proceedings, Surface Mount International Conference, SMTA, Chicago, Illinois, September 25 -29, 2005.
- Clech, J-P., Henshall, G. and Miremadi, J. "Closed-form, strain-energy based acceleration factors for thermal cycling of lead-free assemblies", Proceedings, SMTA International Conference, Oct. 4-8, 2009, San Diego, CA.
- Clech, J-P., "Board, package and die thickness effects under thermal cycling conditions", Proceedings, SMTA International Conference, September 27 - October 1, 2015, Rosemont, IL.
- Engelmaier, W., "Fatigue life of leadless chip carrier solder joints during power cycling", *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. 6, No. 3, September 1983, pp. 232-237.
- Engelmaier, "Creep-fatigue model for SAC405/305 solder joint reliability estimation - a proposal," *Global SMT & Packaging*, Vol. 8, No. 12, December 2008, pp. 46-48.
- Farooq, M., Goldmann, L., Martin, G., Goldsmith, C. and Bergeron, C., "Thermo-mechanical fatigue reliability of Pb-free ceramic ball grid arrays: experimental data and lifetime prediction modeling", IEEE Proceedings, ECTC 2003.
- Freescale, Wafer Level Chip Scale Package (WLCSP), <http://international.electronica-azi.ro/2015/03/11/wafer-level-chip-scale-package-wlcsp/>, March 11, 2015.
- Gatz, W. and Evans, T., "Thermal cycle reliability study of vapor phase BGA solder joints", Proceedings, IPC APEX Expo, 2012.
- Goldmann, L. S., "Geometric optimization of controlled collapse interconnections", *IBM Journal of Research and Development*, May 1969, pp. 251-265.
- Greer, S. E., "Low Expansivity Organic Substrate for Flip-Chip Bonding", *IEEE Transactions On Components, Hybrids and Manufacturing Technology*, Vol. 2, No. 1, March 1979, pp. 140-144.
- Itoh, M., Sakai, Y., Miwa, M. and Taketomi, K., "Direct mounting of chip carriers on printed wiring board", *NEC Research and Development*, No. 65, April 1982, pp. 33-38.
- IPC-9701, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, IPC - Association Connecting Electronics Industries, January 2002/IPC-9701A, February 2006.
- Kaysar Rahim, M. S., Zhou, T., Fan, X. and Rupp, G., "Board Level Temperature Cycling Study of Large Array Wafer Level Package", Proceedings, IEEE, 59th Electronic Components and Technology Conference, pp. 898-902, San Diego, CA, May 25-29, 2009.
- Meilunas, M. and Borgesen, P., "Effects of cycling parameters on the thermal fatigue life of mixed SnAgCu/SnPb solder joints", *ASME Transactions, Journal of Electronic Packaging*, June 2011, Vol. 133, pp. 021001-1/021001-5.
- Nguyen, L., Kelkar, N., Kao, T., Prabhu, A. and Takiar, H., "Wafer Level Chip Scale Packaging – Solder joint reliability", *IMAPS, The International Journal of Microcircuits and Electronic Packaging*, Vol. 21, Number 4, Fourth Quarter 1998, pp. 367-373.
- Norris, K. C. and A. H. Landzberg, A. H, "Reliability of Controlled Collapse Interconnections," *IBM Journal of Research and Development*, May 1969, pp. 266-271.

- Okura, J. H., "Effects of temperature and moisture on durability of low cost Flip Chip On Board (FCOB) assemblies", Ph. D. dissertation, Dept. of Mechanical Engineering, University of Maryland, College Park, 2000.
- Roellig, M., Dudek, R., Wiese, S., Boehme, B., Wunderle, B., Wolter, K-J. and Michel, B., "Fatigue analysis of miniaturized lead-free solder contacts based on a novel test concept", *Microelectronics Reliability*, 2007, Vol. 47, pp. 187–195.
- Sherry, W. M. and Hall, P. M., "Materials, structures, and mechanics of solder joints for surface mount microelectronics technology", Conference Proceedings, Interconnection Technology in Electronics, Fellbach, Germany, Feb. 1986, pp. 47-61.
- Wild, R. N., "Properties of some low melt fusible solder alloys," IBM Technical Report No. 712000408, Oct. 1971.
- Yang, H., Elenius, P., Barrett, S., Schneider, C., Leal, J., Moraca, R., Moody, R., Kweon, Y-D., Patterson, D. and Goodman, T., "Reliability characterization in Ultra CSP™ package development", Proceedings, IEEE, 50th Electronic Components and Technology Conference, Las Vegas, NV, May 21-24, 2000, pp. 1376-1383.

APPENDIX

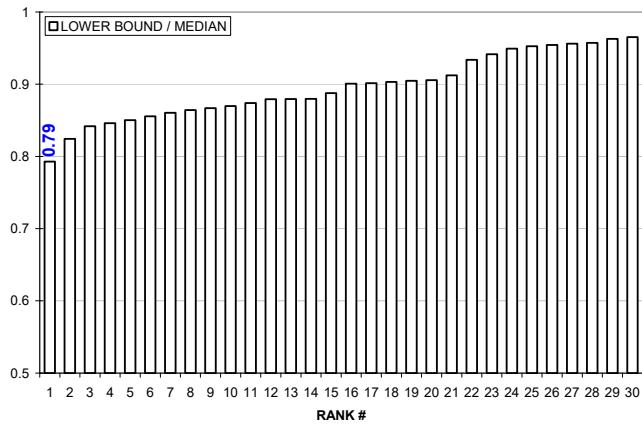


(a)

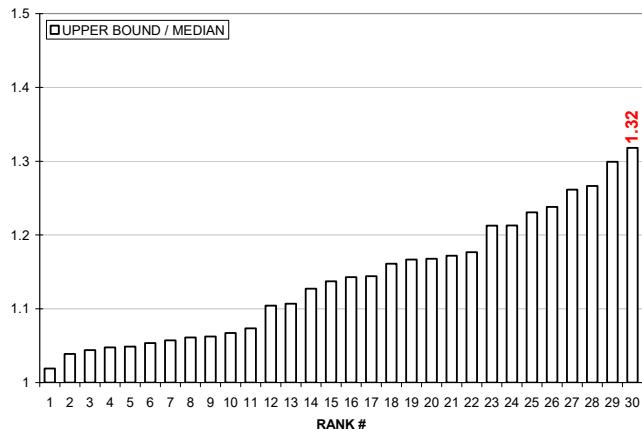


(b)

Figure A.1: Engelmaier's "Coffin-Manson" exponent m for a) near-eutectic SnPb and b) SAC305/405 solders as a function of dwell time (greater than 5 minutes) and mean cyclic temperature from -25°C to 75°C. The equation for "m" and the model constants are from Engelmaier, 2008.



(a)



(b)

Figure A.2: Ratio of “median” values to (a) “lower” and (b) “upper” bound values of characteristic lives at the 90% confidence level. In each graph, ratios are rank-ordered by increasing values across 30 independent experiments from throughout the literature. Based on mid-points (rank # 15 and #16), “median” ratios are 1.1 to 1.15, implying a typical error of 10% to 15% on characteristic lives, but as much as 1.21 to 1.32 for extreme values, suggesting possibly larger errors on characteristic lives, up to the range 21% to 32% or more, at the 90% confidence level.