

# BOARD LEVEL FAILURE ANALYSIS AND DEMOUNT CHALLENGES FOR PACKAGE ON PACKAGE

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## ABSTRACT

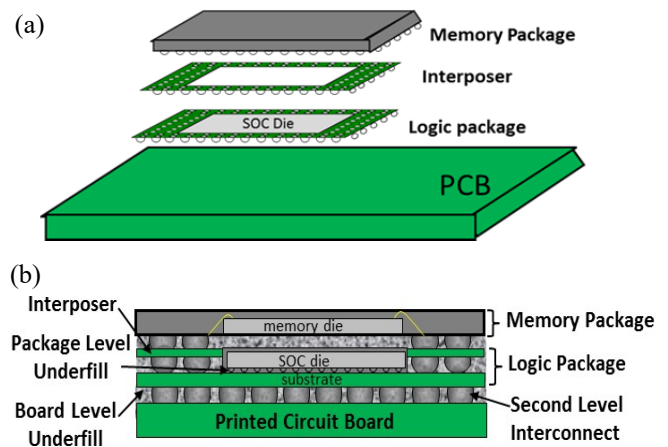
The demand to build products using Package on Package (PoP) technology is increasing rapidly especially for handheld products such as mobile communications, tablet and camera based technology. Generally, PoP is an integrated circuit packaging that vertically combine discrete logic and memory ball grid array (BGA) packages. It is different from traditional packaging whereby each die is placed in its own package and mounted directly on the printed circuit board (PCB) side-by-side. The main driving force for PoP development is to allow higher component density in devices as the PoP structure promotes space saving. This packaging also leads to better electrical performance as there are shorter path for communication between microprocessor and memory. However, the board level failure analysis (FA) becomes more challenging when the packaging technology transits from traditional packaging to PoP packaging. For instance, the multiple interfaces of PoP packaging hinders the dye and pull (DnP) test at a selectively interface for solder joint evaluation. Other methods such as 2D X-ray imaging could only provide preliminary indication of the gross defect. To-date, there are limited works being documented for board level FA for PoP component mounted on PCB. Moreover, underfill is sometimes applied to the PoP packaging to enhance the reliability of the product. With the introduction of underfill, conventional thermal method to demount component for fault isolation or component testing creates another challenge. Hence it is highly desirable to streamline the methodologies to address these challenges for better root cause analysis. This paper discusses about the board level FA and component demount experiments for PoP mounted on PCB. The FA methods includes 2D and 3D X-ray imaging, cross section and DnP test. PoP component demounting from board and its challenges are also discussed in this paper. The demount methods cover thermal, mechanical milling and micro-abrasion technique.

Key words: PoP, failure analysis, rework, interconnect, printed circuit board

## INTRODUCTION

PoP technology is rapidly evolving to keep pace with the increasing demand for size and cost reduction, coupled with improved signal processing performance and memory capabilities. PoP is a stacked package where two packaged integrated circuits are placed directly on top of each other rather than the bare die. This kind of vertical spacing has

emerged as the preferred stacked packaging platform of choice in portable electronic products such as mobile phones, digital cameras, portable media players, gaming and other handheld mobile applications. Figure 1 a illustrates one of the example of PoP's structure with mixed logic-memory stacking where the logic package (such as SOC) is on the bottom and the memory package is on top. An interposer is in between memory package and logic package to serve as an electrical interface routing between the two packages. The logic package is on the bottom because it needs many more BGA connections to various input/output pins on the PCB. The bottom logic package is designed according to JEDEC JC-11 standards, delivered by the logic supplier and tested to the same performance and reliability levels as a standard component. Whereas the top component is delivered by the memory supplier to the same levels and product flow as a standard component. These two components are stacked using a modification of the standard surface mount technology (SMT) assembly flow maintaining a single solder reflow process. During the assembly of the electronics products, the bottom package of the PoP stacking is placed directly on the PCB using SMT assembly process. Sometime the PoP vertical stacking structure requires implementation of underfill to ensure device reliability. Figure 1 b shows the cross section view of PoP package assembled on board with the implementation of underfill.



**Figure 1. a)** Illustration of mixed logic-memory stacking of PoP structure; **b)** Cross section view of PoP package assembled on PCB with the implementation of underfill.

Underfill is a type of liquid encapsulate, usually consisted of epoxy resin heavily filled with silicon dioxide. It is applied between the chip, component or/and substrate after interconnection formed. Upon curing, the hardened underfill exhibits high modulus, low coefficient of thermal expansion matching that of the solder joint, low moisture absorption and good adhesion to the component and the substrate. It not only provides stress relief for the solder interconnections by redistributing the stresses, but also protects the interconnections from harsh and hazardous environmental by delaying the gases or vapor diffusion processes [1]. Several works regarding the study of underfill material for PoP to achieve reliable board level performances have been reported [2, 3]. In spite of a great success of such stacked and compact package in the market, its architecture poses serious challenges to existing inspection or board level FA techniques such as optical inspection, 2D X-ray or scanning acoustic microscopy (SAM). Furthermore the use of underfill material especially the thermo-cure or non-reworkable type makes the component demount or rework process more complex. Without the underfill, the PoP component can be easily demounted from the PCB using standard thermal rework method by melting the solder balls. The demounted component can then be sent for further electrical testing. If the underfill is thermally reworkable and process has been well optimized for a particular underfill, it is possible to demount a PoP from board [4]. However if the failure signature is temperature sensitive, it may not be best to use this methodology as it requires high temperature and multiple heating cycles to fully separate each layer of PoP.

For board level FA, the most basic thing for the analysts is to isolate if the failure is on a board, in a component, or far deeper in the device. In case of a PoP package it gets more complex as once the board related failure is eliminated and isolated to PoP package the question becomes whether the failure is on SoC, interposer or memory. It is particular crucial when there is incoming material issue and the fault isolation to a particular package is critical to avoid any delays in product release. Hence only after the fault isolation, the further in-depth analysis for investigation of underlying failure mechanism and its root cause is carried out. Usually in FA process flow, non-destructive analysis is done first to understand the failure location and potential root cause. It provides an indication of areas where further destructive FA may need to be performed and guides in the selection of the destructive technique. For instance, traditional 2D X-ray inspection is very useful for inspecting solder related defects such as voids, insufficient solder, misalignment and solder bridging [5]. However, for PoP assembled on board, its utility becomes very limited when it involves identification of defects at complex stacked packages. The overlapping of solder joint at stacked packages hinders the precise isolation of defective layer. To overcome this limitation, 3D X-ray imaging is an alternative non-destructive way to check the internal structure of the PoP assembled on PCB. 3D X-ray imaging involves a utilization of a high-resolution 3D X-ray microscope with

submicron resolution imaging of intact packages for virtual cross sectioning with a fast time to result. The virtual cross sectioning helps in analyzing the complex electronic products, covering the analysis from die level, package level to board level interconnect [6]. In our work, we have successfully utilized the 3D X-ray tool to identify the defective location of PoP on board. Another well-known non-destructive imaging method for the package internal defect is scanning acoustic microscopy (SAM). SAM uses a high frequency ultrasound transducer to emit sound waves that are either echoed by or transmitted through a material. SAM is commonly used to analyze internal defects such as void, delamination, crack and fracture that may be hidden within inherently susceptible materials and device types. However for PoP assembled on PCB, the ability to image and detect the defects on the assembled consumer products is much limited due to the complexity of multilayer stacking from PoP component down to PCB [7]. Recently, novel techniques such as on-board package decapsulation and microabrasion have been shown for FA applications. These are particular useful when thermal treatment needs to be avoided on packages during FA [8, 9]. These techniques can be easily applied to PoP package for precise root cause analysis as well. For example, memory of PoP package can be selectively decapsulated while still mounted on board by microabrasion or chemical decapsulation and inspected for issue prior damaging the entire PoP stack up.

Next in-depth FA flow after preliminary FA findings from non-destructive technique is important for the understanding of the failure mechanism and assisting in root cause analysis. It can be carried out using various types of destructive FA techniques such as DnP, cross sectioning or decapsulation. The DnP method allows the failed solder joint to be marked with a red dye regardless of the location in the BGA. Details such as disbond type, location and frequency can be obtained by performing mapping of dyed component. Whereas cross section technique allows analyst to evaluate the cause of specific failure location that cannot be accurately determined from external appearance alone. Examples of cross section approach is to check on solderability, changes of intermetallic compound structure, PCB or coating delamination, failure initiation sites and so on [10]. However, up to date, there is no work has been reported on the applicability of the typical board level FA techniques for PoP assembled on board. This paper will focus on the essential board level FA methodologies development for PoP assembled on board and some underfill PoP component demount experiments.

## EXPERIMENTAL

Several PoP with the stacking of memory|interposer|SOC assembled on PCB were received for board level physical FA. The assessment of applicability of board level physical FA methods were divided into two categories: non-destructive and destructive.

## Board Level FA Techniques for PoP Assembled on Board

The development of non-destructive FA techniques for PoP on board is important because the failed products are unaffected by analysis. 2D X-ray imaging has been widely used in the past as an effective tool for diagnosing solder defects such as solder short under BGA type package. However for PoP on board, 2D X-ray alone is insufficient in pin pointing the defects for multi-stacking BGAs. Therefore, the non-destructive methods used in our work cover both 2D X-ray and 3D X-ray imaging.

The destructive methods used are DnP and cross section. The dye penetration process was carried out using red solvent followed by vacuum and drying processes. The pull operation was then conducted to break every single solder joint and the defective joint will be marked with red dye stain on its breaking interface. Besides DnP, another destructive method carried out is cross section. For cross section analysis, the area of interest was first encapsulated using mixture of epoxy resin and hardener in the ratio of 3:1. After curing, grinding and polishing processes using different grades of silicon carbide papers and alumina powders were carried out.

### Underfill PoP Demount and Underfill Removal Experiments

Besides exploration and assessment on several board level FA techniques for PoP assembled on board, evaluation on underfill PoP demounting technique and underfill removal were carried out. The main purpose for demounting PoP component from board is to send the whole PoP component or the single SOC package to component level electrical testing. The evaluated methods includes thermal, mechanical milling and micro-abrasion.

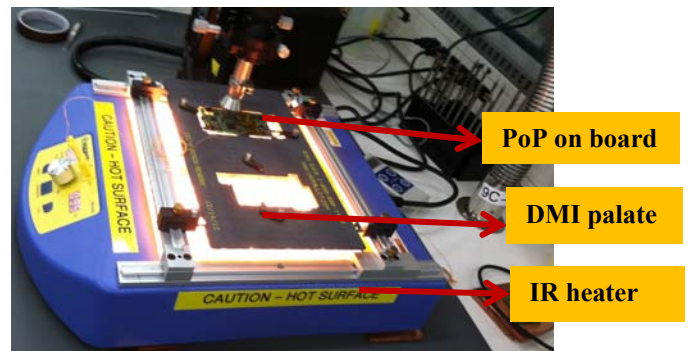
#### Thermal Method

Theoretically, thermal approach for demounting reworkable underfill package involves heating up the package above glass transition temperature ( $T_g$ ) to soften the underfill and then apply twisting/prying force to separate package from PCB.  $T_g$  for underfill material is usually lower than reflow temperature, thus underfill package is expected able to be demounted from board at reflow temperature. However, it has been found that even at reflow temperature, the underfill material maintains its integrity at reflow temperature. Hence a great deal of force is required to separate the package from PCB leading to damage. In present case, to remove the PoP from the PCB, the board was loaded onto a pallet as shown in Figure 2. This pallet is used to hold the board firmly to safely remove the component while the experiment is being performed. The assembly was placed on an IR bottom heater set at 180 °C in power mode. The board was then preheated for 70 seconds at these settings. The top heater was positioned directly over the PoP which is to be removed. The nozzle of the top heater was lowered to hover closely over the component. Once the board was preheated, profile on the top heater started which consisted of four zones as described in the Table 1. The profile ran through

each zone ramping in heat until it reached zone 4. In zone 4, when there were only 20 seconds left, the nozzle of the top heater was quickly raised and moved away. The component was picked off in zone four of the profile when about 15 seconds were left to ensure minimal damage in that small window of time. After the component was successfully removed, the bottom heater was turned off and the top heater was allowed to run through its cool down zone and eventually shut off.

**Table 1.** Profile Setup for Top Heater used for Component Demount

Zones	Temperature (°C)	Time (seconds)
1	220	60
2	340	60
3	360	60
4	420	60



**Figure 2.** Setup for PoP component demount from board using thermal method.

#### Mechanical Milling Method

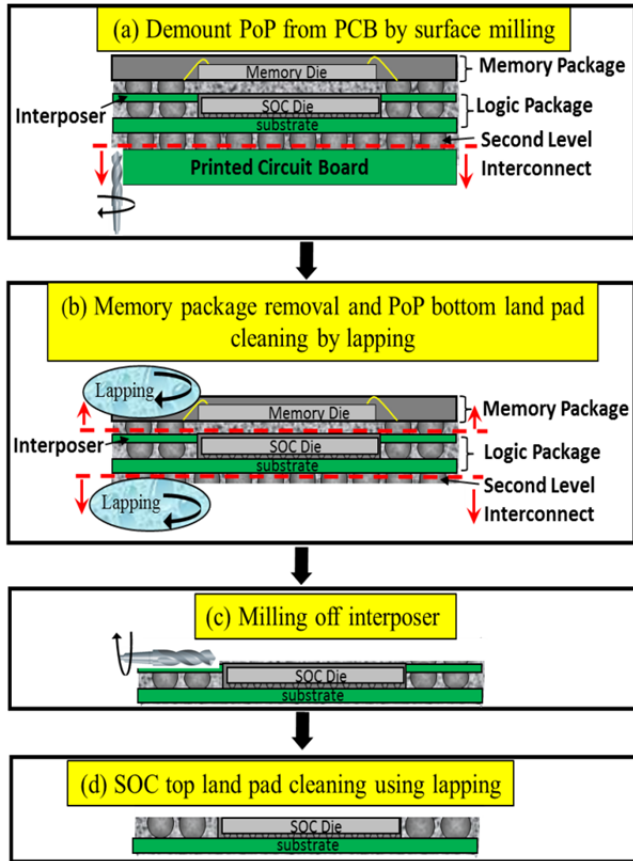
The milling depth was determined by measuring the thickness of PCB using micrometer prior to mechanical milling process. Figure 3 illustrates the process flow of SOC removal from PoP stacking (memory|interposer|SOC) assembled on board using combination of both mechanical milling and lapping methods. For surface milling process to demount the whole PoP component, the board was placed on the fixture with component facing downwards. After milling off the PCB and took out the PoP component, the bottom land pad of component was then cleaned by lapping process. The PoP component can be re-mounted back to the gold board for some PoP component testing or any validation purpose. For further in-depth electrical testing of SOC, the memory and interposer need to be removed. The further vertical milling was used for precisely removal of interposer after lapping off the top memory.

#### Micro-Abrasion Method

For PoP component with underfill, the excessive underfill could not be removed thoroughly using thermal method or mechanical milling method. In our work, micro-abrasive blaster was used to remove the unwanted underfill at the PoP component after the component was demounted from PCB. The system comprised of abrasive media tank, blast enclosure, abrasive media, handheld nozzle and compressed

dry air supply. The fine abrasive media with dry air was propelled through a nozzle to the package surface to remove

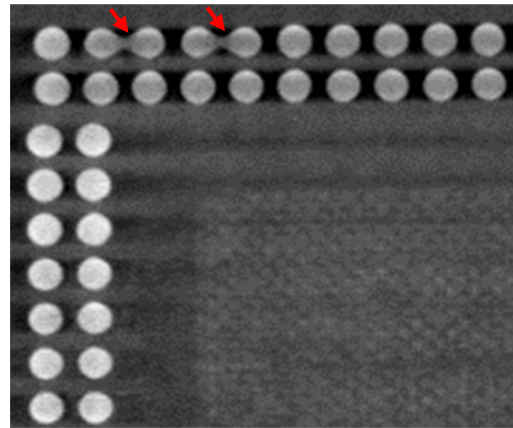
excessive underfill material. The pressure used for the blasting process is about 30-35 psi. Two types of abrasive media were studied in the underfill removal experiment which are fine magnesium sulfate monohydrate and walnut shell.



**Figure 3.** Flow of SOC removal steps for POP component on board using combination of both mechanical milling and mechanical lapping methods.

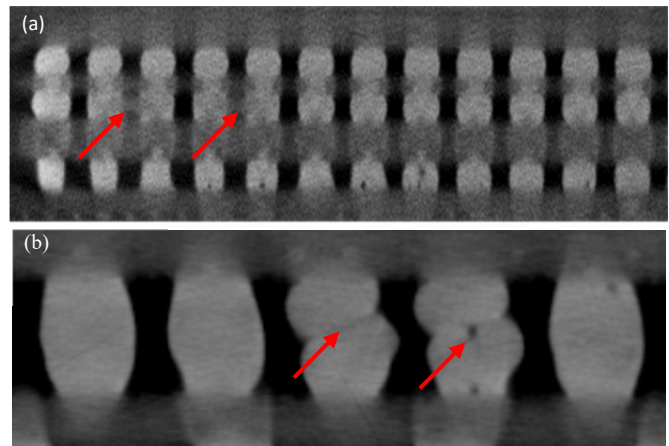
### EXPERIMENTAL RESULTS AND DISCUSSION

Prior to in-depth destructive FA, X-ray imaging was carried out to pin point the defect location. However as shown in Figure 4, solder bridging was detected at the peripheral solder joints of PoP using 2D X-ray imaging but exact layer (memory|interposer|SOC) of solder bridging remained unknown. The overlapping of solder joint due to multilayer stacking has hindered the detail defect identification by planar viewing.



**Figure 4.** 2D X-ray of solder bridging at the peripheral solder joints of PoP assembled on board but exact layer of solder bridging remained unknown.

On the other hand, 3D X-ray imaging is capable to analyze different layers of PoP and successfully isolated the defect to specific layer and location of PoP. Example of defects detected by our 3D X-ray imaging tool is solder bridging at the interface between interposer and memory (Figure 5 a) and head on pillow defect (Figure 5 b).



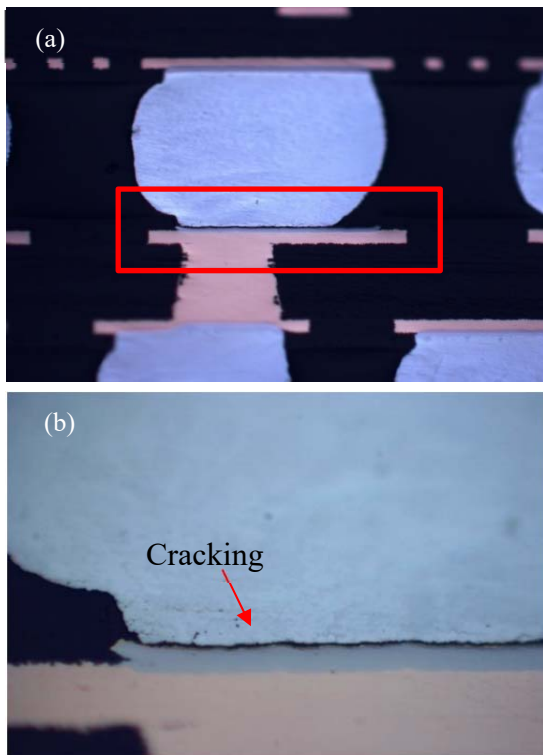
**Figure 5.** a) Exact layer of solder bridging; b) Head on pillow defect for PoP assembled on board were identified using 3D X-ray imaging.

For DnP work on non-underfill PoP component, result showed that the red dye is able to penetrate into the PoP component if the component is without underfill. However the problem exists when we tried to selectively pull out the specific stacking of PoP component for visual inspection. The component tends to break at weaker interface of the stacking instead of intended interface. This resulted the incomplete inspection and mapping of overall breaking interface for the failed part. Figure 6 a,b shows the poor breaking interface after mechanical pulling process. On the other hand, cross section technique is still applicable to PoP component mounted on board regardless the PoP is with underfill or without underfill. As seen in Figure 7 a,b, cross section analysis had successfully revealed the cracked solder joint at the memory side. Such defects is undetectable

through 2D X-ray inspection or DnP test. From the cross section, analyst can investigate the failure mechanism by analyzing the IMC formation, surface finish of soldering pad, bond pad thickness measurement, and contamination of breaking interface. The cross-sectioned failed part can also be subjected to scanning electron microscopy for further morphology and elemental analysis.



**Figure 6.** Improper breaking interface after pulling process.

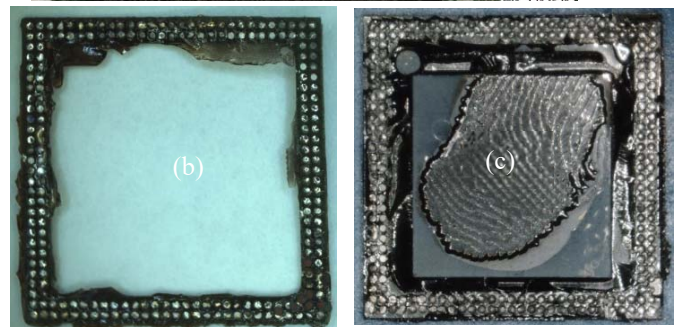
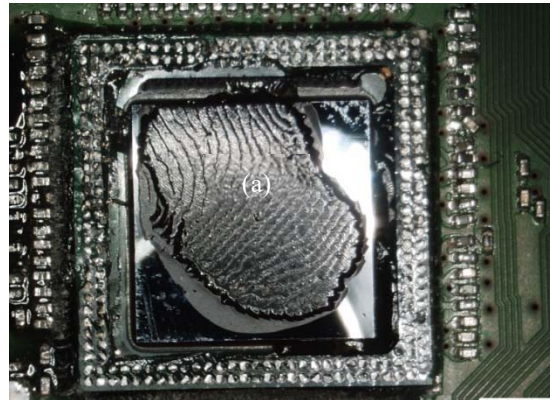


**Figure 7.** a) Low magnification inspection; b) High magnification inspection of cracked solder joint at memory side using cross section technique.

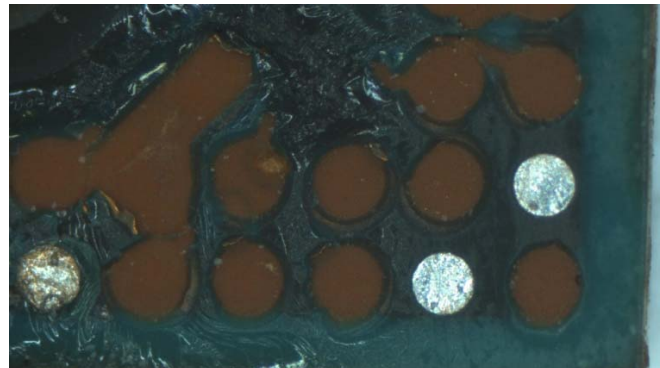
#### PoP Component Demount and Underfill Removal

Fully underfill PoP component mounted on PCB was subjected to thermal demounting process and the experimental result was not promising. As seen in Figure 8, three stacking of PoP component: memory, interposer and SOC had been separated with massive underfill material surrounded them. The success rate of underfill PoP component rework or demount using thermal method is inconsistent and low due to several key reasons: 1) full coverage of underfill at each stacking; 2) underfill material

did not melt as how solder did during peak reflow temperature; 3) slight twisting force for component pick up when the thermal profile reached the peak temperature could induce component pad damage. Figure 9 shows the example of lifted pad of the component induced during the twisting motion from thermal demount work.

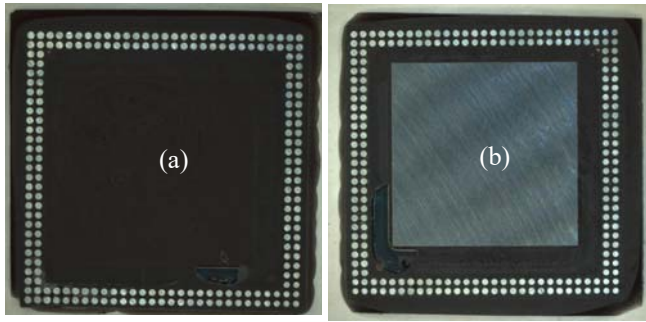


**Figure 8.** a) SOC on board; b) interposer; c) memory was separated using thermal method.



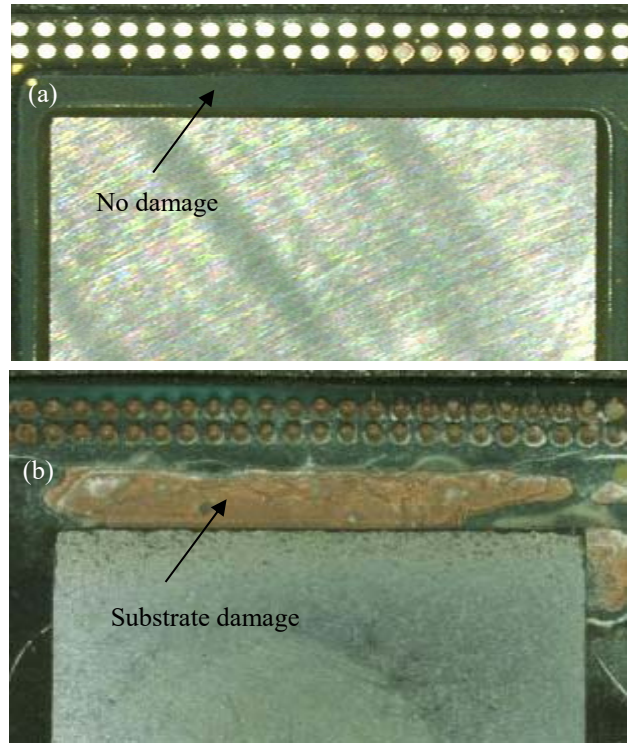
**Figure 9.** SOC land pad damage resulted from twisting motion during thermal demount experiment.

For mechanical milling method, the whole PoP component was successfully removed from board without applying heat. No visual damage to the component land pad was observed post removal process. The only drawback of this method is the need to sacrifice the board in order to remove component. Figure 10 a shows the interposer|SOC stacking post memory removal using both milling and lapping process. SOC die backside was clearly visible with further lapping process (Figure 10 b).



**Figure 10. a)** Interposer/SOC stacking after memory removal using mechanical method; **b)** SOC die backside was visible after lapping.

The excessive underfill surrounded the edge of die backside was then ablated by two different types of abrasive media: fine magnesium sulfate monohydrate and walnut shell. In our experiment, walnut shell successfully removed the underfill from the edges of the die backside in approximately 2 minutes under 35psi air pressure, exposing the substrate surface without any visual damage (Figure 11 a). On the other hand, magnesium sulfate monohydrate resulted physical damage to the component substrate, exposing copper layer (Figure 11 b). The data revealed the significant of the selection of abrasive media for the underfill removal purpose. The effect of an abrasive media to the removal process is contributed by its three key characteristics: particle shape, hardness and particle size. For instance soft abrasive media likes walnut shell can reduce the heat buildup on the substrate and thus reduce warping and pitting. However the ability to remove the material is not as aggressive as harder abrasive media. Fine kieserite is aggressive in removing underfill material but it is easily damage the component. The cleaned and removed component can then be proceed with further component level testing. The further SOC testing post removal and cleaning process from underfill PoP component had been reported by Ng *et. al.* [11].



**Figure 11. a)** Excessive underfill was cleaned off without damaging the substrate post ablation using walnut shell; **b)** Substrate damage with exposed copper layer post ablation using magnesium sulfate monohydrate.

Table 2 is the summary of all the board level FA techniques and PoP component demount techniques discussed in this paper. The pros and cons for each techniques is summarized too.

**Table 2.** Summary of FA Techniques used for PoP Assembled on Board and Their Pros and Cons.

Techniques	Pros	Cons
2D X-ray imaging	Non-destructive internal structure inspection for gross defects or solder joint abnormality	Unable to pin point the exact defective layer/location due to multi stacking of BGAs of PoP component on PCB.
3D X-ray imaging	Non-destructive virtual cross sectioning to pin point the exact defective layer of PoP component assembled on board.	Difficult to see the cracks (specially fine cracks) unless high resolution scan is done which may take days for a small scan area
Dye and pull	Allows the failed solder joint to be marked with red dye regardless of the location in the BGA	Unable to selectively pull the intended layer of PoP for whole layer BGAs inspection.  Not applicable if the PoP mounted on board is with underfill
Cross sectioning	Allows evaluation of the cause of specific failure location that cannot be accurately determined from external appearance	Need the identification of failure location before cross section otherwise time consuming  Destructive method
Component demount: Mechanical milling & lapping	Enable PoP component demount from PCB for PoP testing  Enable SOC package demounting from PoP stacking for SOC testing	Sacrifice PCB for PoP component demounting  Sacrifice memory and interposer for SOC package demounting
Component demount: Thermal method	Can demount layer by layer of PoP component from PCB	Inconsistent and low success rate  Not suitable for temperature sensitive failure signature
Underfill removal: Micro-Abrasion	Able to remove excessive underfill without damaging the package	Manual method and hence recipe needs fine tuning for each user.

## CONCLUSION

In our work, various board level FA methodologies for PoP assembled on boards were evaluated. The result showed 3D X-ray imaging can overcome the limitation of 2D X-ray imaging in detecting the anomalies of multilayer solder joints in the non-destructive way. 3D X-ray imaging technique demonstrated its capability in isolating the defect down to specific stacking of PoP component mounted on board which is very useful for further failure mechanism investigation using destructive analysis method. Cross section method had also been proven to be one of the destructive FA technique for the root cause analysis of PoP component assembled on board. On the other hand, DnP method is not recommended for stack by stack solder joint evaluation of PoP as the component breakage tends to happen at weaker interface of the stacking instead of intended interface during pulling process. For underfill PoP demount, combination of mechanical milling and auto-lapping process had showed a promising result. Micro-abrasion techniques using walnut shell can be used for excessive underfill cleaning post demount process. Whereas thermal method is not able to demount the underfill PoP as underfill material did not melt at reflow temperature as how solder behaves. Furthermore twisting force applied during component pick up at reflow temperature potentially damage the PoP component.

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