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3D INTEGRATION
A THERMAL-ELECTRICAL-MECHANICAL-RELIABILITY STUDY

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ABSTRACT
Increasing demand, regarding to advanced 3D-packages and high performance applications, accelerates the development of 3D-silicon integrated circuit, with the aim to miniaturize and to reduce the cost. Due to drastic dimension mismatches between interconnects, through-silicon-vias (TSV), and landing pads, the reliability of the systems and components are affected by thermal and thermal-electrical loads due to high temperature as well as high applied currents. This stress leads to degradation effects like electro- and thermomigration (EM, TM). Mechanical or thermal stress due to coefficient of thermal expansion (CTE) mismatch of the different materials on one hand and induced stress during the flip-chip-packaging process on the other hand can lead to delamination and cracking on the packing side or in the IC's.
Investigations of electro- and thermomigration as well as the mechanical stress concerning the reliability of the through silicon vias, BGA-PoP-Packages as well as µ-bumps which are the most critical areas for the emergence of failure, remains a major concern in reliability studies. Generally measurements are time consuming and expensive and the time-to-market cycle is in the focus of interest too. Due to this, simulations offer a possibility for a fast analysis of weak links and problematical areas in the investigated structures and avoid re-design.

Key words: µ-bump, PoP, migration, TSV, delamination, cracking, reliability

INTRODUCTION
Due to the exponential growth in device density the miniaturization down to ultra large scale integration (ULSI) reached physical and economical limits. As one consequence the development of electronic devices was made with an increasing number of ICs, which have to be placed in a constant or shrinking amount of space. The width of interconnects, as well as the dimensions of solder balls and bumps or copper pillars for flip-chip application and therefore the distance (pitch) between them decreases. As a result of the finer pitch, the density of solder bumps in flip-chip designs increases. Solutions for the vertical assembly of ICs and complete packages have been developed. This for instance allows the usage of small 3-D assembly technologies like package-on-package or TSV in compact applications (figure 1). The reduction in the geometrical dimensions leads to an increase in the carried current density in the solder bumps, pillars, interconnects or TSV's. Especially TSV has a critical role in 3-D applications [21]. The reliability in the frame of migration or thermal stress effects is determined by aging test. To shorten these time-consuming long-term tests, highly accelerated stress tests of bump and metallization systems under high current and temperature loads are used for reliability characterization. To understand the failure mechanism and physical background simulations can assist the tests. The prediction of local weak spots in interconnects contacts as well as TSV and solders bumps by finite element simulations is described as a helpful procedure [5, 20]. Beside this the modern 3-D integration leads to more complex material compositions in the systems concerning the different physical material properties leading for instance to intrinsic stress during the processing. Therefore the process induced stress should be considered in the simulations [2]. Higher applied currents on interconnect, contacts and bumps result in Joule heating as well as high temperature gradients in the bump and metallization systems. The exponential temperature dependence of the diffusion coefficient influences the temperature acceleration and the mass flux becomes more important compared to the influence of the applied current on the mass flux. Thus TM effects can not anymore be neglected [1].

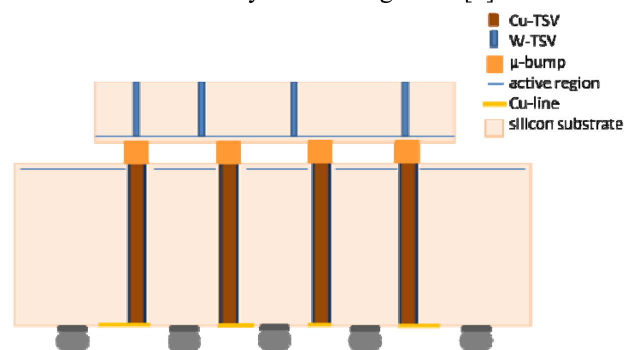

Figure 1*:* Simplified illustration of 3-D integration.

Simulation results of accumulated stress and plastic strain show that interface stress between copper and silicon is an indicator for a potential failure such as delamination and

die cracking. The stress in the through silicon via also depends on the filling material, on the size of holes and on the thickness of the wafers. Increasing via diameter increases the stress in the through silicon via and the effect of thermal expansion mismatch between copper, silicon and silica [20]. Also electromigration (EM) in TSV was detected, although the dimensions in comparison to interconnects of for instance 65nm technology node are quite big. Simulation investigations of BGA-bumps are described in detail in [5]. Also the mechanical behavior of TSV was investigated by simulations [20].

Concerning the simulation in 3-D integration all possible effects of the interconnect system and the packaging have to be in view, and have to be investigated in detail.

GOAL, WORKFLOW AND MODELING

The degradation in interconnects, BGA- and µ-bumps, pillars and TSV under high current and temperature load is investigated and the current, temperature and mechanical stress distribution calculated. As a result the weakest spots in the structure can be determined. The finite element analyses and the mass flux divergence calculation of these phenomena will show the suitability of the method by comparison with experimental results.

Beside the electromigration due to the joule heating, temperature gradient driven thermomigration can occur in the bumps. Also accelerated intermetallic compound (IMC) growth due to electromigration (EM) is found after stress testing. Out of this the reliability prediction due to the different migration mechanisms like electro- and thermomigration (TM) become more and more important.

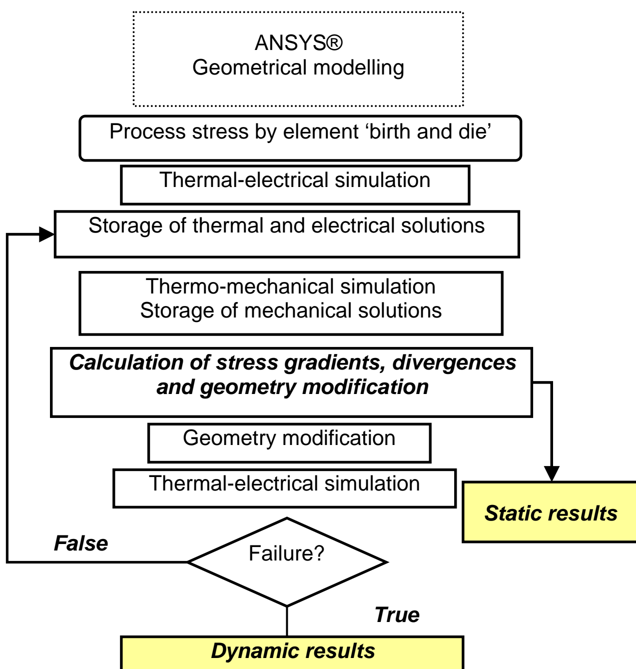

Figure 2: Workflow in ANSYS®.

The geometrical dimensions used in the simulations are normally taken from layouts, SEM or TEM pictures as well as literature. Based on the parameters a finite element model with an adequate mesh concerning electrical or mechanical simulation has to be constructed with all boundaries. For packages heat conductivity and radiation have to be considered. In the case of interconnect structures this effects can be neglected. The main heat distribution there is heat conductivity. A typical metallization scheme with power metal in layer 6 is shown in figure 3. In the next step the material properties for the simulations are taken from literature or measurements. If the simulations are carried out with ANSYS® the element 'birth and die' capability can be used to determine the process induced stress [13]. This facility virtually removes (or adds) materials by management of the stiffness. In a first step the whole finite element model is made including all material properties and boundaries. Afterwards all elements not used for the first process step are removed. The removed materials are still present in the model, but they have only an insignificant contribution to the matrix of stiffness. When the elements of a material are removed, their strain is set to zero. When the elements of a material are reactivated, the original physical properties are set back.

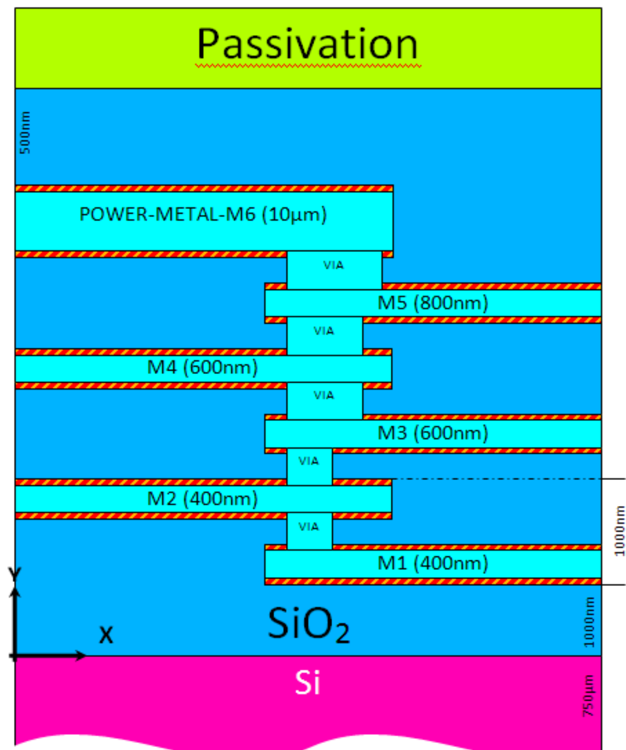

Figure 3: Example of a metallization scheme with power metal in layer 6.

Out of this the pre-stress out of the specific temperatures of every single process step is calculated for the whole metallization system. After doing the finite element analysis all results are stored in files for a further processing with an external program. The stress gradients, the distribution of hydrostatic stress and the local mass flux and mass flux divergence distribution of the different migration mechanisms are calculated and the results restored for graphical interpretation. The workflow in ANSYS® is shown in figure 2. The influence of grain boundaries or interface migration is represented by the measured activation energy. The calculation gives the result for each node in the finite element mesh for a worst case scenario of the coincidence of maximum stress,

maximum mass flux divergence, triple point or interface. Out of this the weakest point in the structure is identified and the different migration mechanisms under applied current can be calculated.

MASS FLUX AND MASS FLUX DIVERGENCE

EM is highly temperature dependent. The divergence of the mass flux density is a scalar product of the local current density and the local temperature gradients. The mass flux divergence depends on the amount of these two vectors and the angle between them. A positive mass flux divergence leads to a possible void growth and a negative mass flux divergence to a hillock formation.
An external program is used for the determination of the stress gradients as well as hydrostatic stress, the mass flux and the mass flux divergences [2]. The electromigration mass flux is defined by

$$\overrightarrow{J_{EM}} = \frac{N}{k_B T} e Z^* \left(\vec{j} - \vec{j}_{th} \right) \rho \; D_0 \exp\left(-\frac{E_A}{k_B T} \right) \quad (1)$$

and the thermomigration mass flux is defined by

$$\overrightarrow{J_{TM}} = -\frac{N Q^*}{k_B T^2} D_0 \exp\left(-\frac{E_A}{k_B T} \right) grad\, T \quad (2)$$

the electromigration mass flux divergence is defined by

$$div\, \overrightarrow{J_{EM}} = \left(\frac{E_A}{k_B T^2} + \frac{\alpha_\rho}{1 + \alpha_\rho (T - T_0)} - \frac{1}{T} \right) \cdot \overrightarrow{J_{EM}} \cdot grad\, T \quad (3)$$

and the thermomigration mass flux divergence is defined by

$$div\, \overrightarrow{J_{TM}} = \left(\frac{E_A}{k_B T^2} - \frac{2}{T} \right) \cdot \overrightarrow{J_{TM}} \cdot grad\, T - \frac{QND}{k_B T^2} \cdot \Delta T \quad (4)$$

N is the atomic concentration, k_B the Boltzmann constant, T the local temperature, ρ the resistivity, Ω the atomic volume, $Q^*/k_B T^2$ is referred as Soret coefficient. A value of $Q^* > 0$ means a heat flux is generated to keep the solute atoms isothermal, which takes place towards the dissolved flux. Is $Q^* < 0$ the flux of dissolved particles and the heat flux are counter set. It follows that in an isothermal system, a density gradient produces a thermal flux and vice versa a temperature gradient leads to a material flux. The activation energy E_A was taken from measurements or literature. In the case of interconnect system the effect of stress migration has to be analyzed.

SIMULATION EXAMPLES

Migration effects like electro- and thermomigration can act as a failure mechanism in ball grid arrays (BGA) used in power modules [4]. An investigation of the current and temperature load on the thermal electrical mechanical behavior of BGA bumps is described in [5]. The failure location after EM stress test and a mass flux divergence analysis of a PoP-BGA will be compared in concern of the thermal-electrical results. Furthermore the influence of the stress distribution on the possible local fracture appearances will be shown through an example exemplary in a Package on Package (PoP). Using the FE-analyses a massive shear load was found. This can lead to local fractures in the bump.

As an illustration a flip-chip bump is investigated concerning its thermal-electrical behavior. Especially the thickness of the aluminum metallization in the die was in the focus here.

For a simplified assembly, a smaller pitch between the bumps CuSn-pillars, bumps with a thin layer of Sn on the top, can be used. These layer thicknesses can vary and the influence on the thermal-electrical behavior was investigated [15, 16].

A comparison between BGA-bumps and µ-bumps, flip-chip bumps as well as Cu-Sn pillar bumps will be investigated under the same applied current and the mass flux divergence will be calculated. It is assumed that the reliability of the µ-bump as well as the Cu-Sn pillars have an electro- and thermomigration risk.

For high power applications with a high performance, a low resistance of the TSV material is necessary. The resistivity of doped poly-silicon is too high. The resistivity of copper is about three times lower compared to tungsten. Nevertheless the thermal expansion coefficient, of copper is 6.5 times and of tungsten 1.7 times higher than that of silicon. The reliability of W-filled vias under high-current stress is reported in [21]. In this study it was found that compared to the W-TSV the bumps have the reliability risk [21]. On the other hand EM failures could be found depending on the current flow direction above and under the TSV [22, 23].

MATERIAL PROPERTIES

The mechanical and electrical material parameters of the solder and interconnect used in the investigations are given in table 1. The material parameters for the calculation of the mass flux and mass flux divergence are given in table 2.

Material	**α [1/K]**	**E [GPa]**	**ρ [Ωµm]**	**K [W/(mK)]**
SnAgCu (SAC)	$2.8\ 10^{-3}$	41.4	0.132	58.7
Cu	$1.6\ 10^{-3}$	125	0.0174	395
Al	$2.3\ 10^{-3}$	68.9	0.0316	237

Table 1: Mechanical and electrical parameters of the solder and interconnect.

Material	**D_0 [m²/s]**	**Z***	**Q [eV]**	**E_A [eV]**
SnAgCu (SAC)	27×10^{-3}	-23	-0.0084	0.792
Cu	17×10^{-5}	-4	0.217	0.9
Al	78×10^{-6}	10	-0.104	0.7

Table 2: Material parameters of the solder and interconnect [7-9].

BGA POP BUMP

In previous investigations was shown that current crowding is the major reason for the electromigration induced void formation at the edges between the cooper traces and the SAC bumps [9, 10]. High electric field strength leads to an increased current density and joule heating at those edges. Due to the high current density the

mass flux due to electromigration is increased and in combination with the raised temperature gradients an accelerated void formation appears. Additionally the EM induced mass flux accelerates the IMC growth at the interfaces. In figure 4 (right) the failure location after the EM stress test was determined by SEM inspection after micro-section of the bump. The mass flux divergence distribution in the bump (left) shows high values on the top of the bump. At this location void formation occurs after EM stress load.

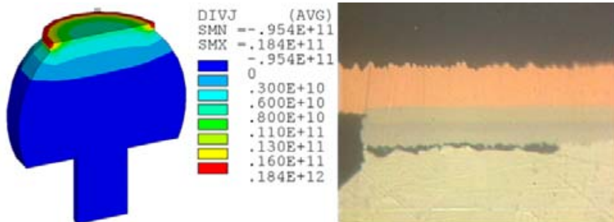

Figure 4: Mass flux divergence (left) and SEM inspection of the failure location on top of the bump (right).

DETERMINATION OF CRACK EVOLUTION IN A BGA BUMP

The influence of the stress distribution at the bump surface will be discussed particularly on the possible local fracture appearances at this position. As a follow-up step of the stress analysis the distribution of the local stress components was carried out by finite element analyses. Different principles for a cracking modeling are described in [11]. One way to indicate the location of cracking appearances is the first principal stress criterion. The material cracks whenever one of the principal stress components exceeds the ultimate tensile strength (UTS). So the principal stresses $\sigma 1$, $\sigma 2$ and $\sigma 3$ have to be calculated and compared with the UTS. According to the first principal stress criterion cracking is expected to appear along the surface of the bump. The influence of the stress distribution on the possible local fracture appearances is illustrated in a 400µm diameter bump. By the FE-analyses a shear load was found. This can lead to local fractures in the bump. In figure 5 the indication of the cracking appearance on top of the bump is shown as an example. The circles indicate an open crack and the circles with crosses indicate a closed crack. The left side of figure 5 shows the hydrostatic stress distribution with maximum values at the top corners of the bump.

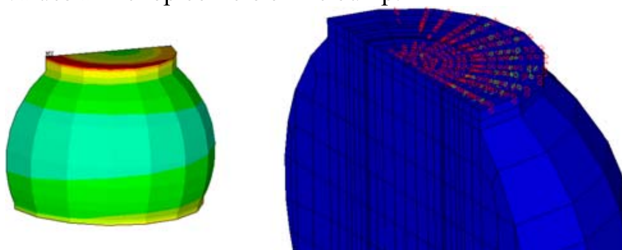

Figure 5: Hydrostatic stress distribution (left) and possible cracking evolution on top of the bump.

FLIP-CHIP SAC BUMP

The accelerated trend to smaller and lighter electronics has accentuated many efforts towards size reduction and increased performance in electronic products. Moreover, RF performances are limited by parasitic effects due to the RLC network between the wirebond from the dies to the leadframe. The use of flip-chip bonding technology employing micro bumps for very fine pitch packaging permits high integration and limits parasitic inductances. However, both electromigration (EM) and thermomigration (TM) may have serious reliability issues for fine-pitch Pb-free solder bumps in the flip-chip technology used in consumer electronic products.

In this investigation the thermal-electrical behavior of a flip-chip SAC-bump and a die containing a power metallization (figure 3) was determined. The model is shown in figure 6 right. High current crowding is found at the bond pad opening. Due to this at this position the highest mass flux divergences occur (figure 6, left). The maximum temperature was found in the aluminum metallization of the die.

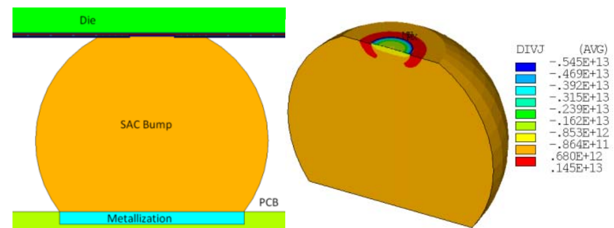

Figure 6: Flip-Chip SAC bump and mass flux divergence distribution.

In figure 7 the mass flux divergence values depending on the applied current are given for an aluminum metallization with a thickness of 1µm and a power metallization of 5µm. In the case of thicker aluminum the current crowding at the bond pad opening decreases. Due to this the mass flux and the mass flux divergence decrease as well.

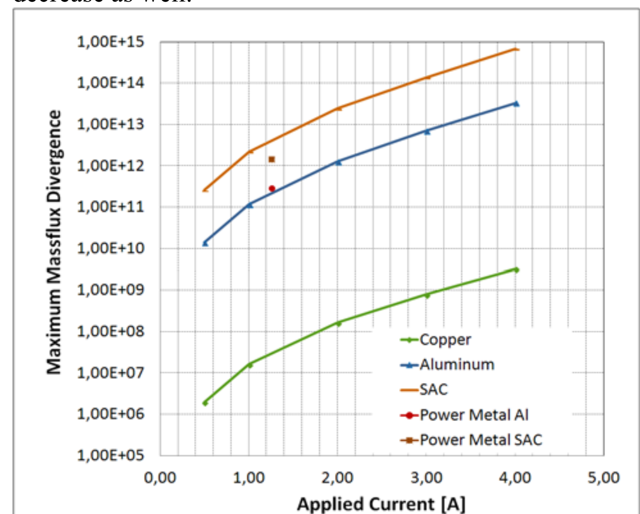

Figure 7: Maximum mass flux divergence depending of the applied current in a flip chip bump with die.

COPPER TIN PILLAR

The evolution of the solder joints lead to smaller bump diameters as well as thinner traces, expecting the same power consumption for the mounted ICs with a higher amount of current crowding. For a smaller pitch between the bumps and a low interconnect inductance as well as a simplified assembly, CuSn-pillars can be used. Due to this copper pillar bumps are the next generation flip chip interconnects with a thin layer of Sn on the top. The

benefit of copper pillars are low costs, lead free concerning green package solutions and a better electromigration performance for high current power applications. The CuSn-pillars can be formed under pressure and a temperature load. This leads to the formation of Cu_3Sn and Cu_6Sn_5 phases. In this section CuSn pillars with different Sn thickness and location in the bump like described in [12] were investigated. In [12] the CC was determined by simulations. Beside CC also the temperature gradients influence the reliability of the pillar.

The finite element mesh of the investigated CuSn-pillars is shown in figure 8. The bumps had a diameter of 24µm and a complete high of 45µm. Above the bumps a Cu trace and below the bumps a TSV (figure 2) were placed in the model.

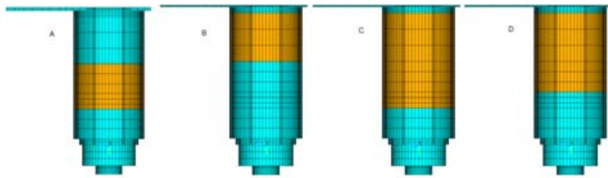

Figure 8: Mesh of the CuSn Pillar with Cu in magenta and Sn in yellow with different Sn thickness.

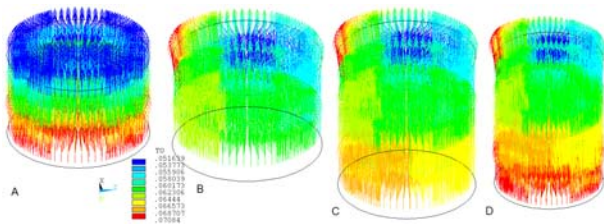

Figure 9: Temperature gradient distribution for the different pillar models.

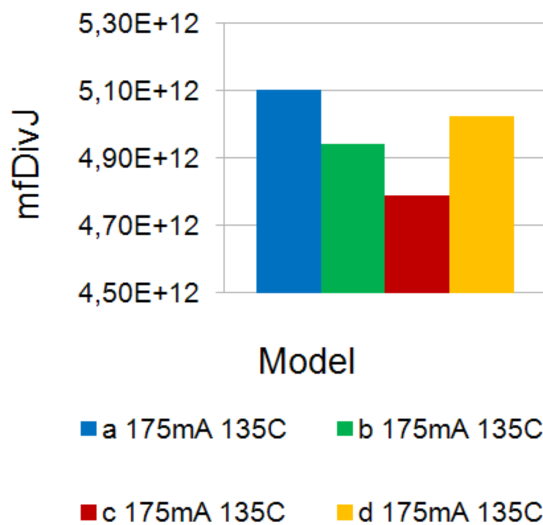

Figure 10: Mass flux divergence electromigration in copper tin pillar bumps.

The applied current was set to 175mA, the substrate temperature was varied from 135 to 150°C and the stress free temperature was set to 150°C. In figure 9 the temperature gradient distribution in the different bumps is shown. The homogenous temperature distribution the bumps can be achieved by a placement of the Sn in the middle (model A). In the case of model B-C high temperature gradients are found at the corner of the Sn and the Cu metallization and beneath the Sn in the pillar. At this position also strong current crowding occurs. Both can lead to a weak link at this position. Depending on the current flow direction the flux will be increased or decreased.

In figure 10 the maximum mass flux divergence due to electromigration is shown for the different pillar models for an applied current of 175mA and a stress temperature of 135°C.The lowest values are found in model C were the Sn is in the middle of the pillar.

µ-BUMP AND COMPARISION OF THE SOLDER JOINTS

A variation of the applied current in a Package-on-Package (PoP) bumps and µ-bump was carried out and the mass flux divergence distribution was determined [10, 18]. The simulations were carried out with anisotropic and temperature depending material parameters. The dimensions of the µ-bumps are similar to the test structures used in [17]. The diameter of the µ- bump is 25µm and the height is 10µm. Over and under the µ-bump a 100µm silicon layer resp. a 50µm thick silicon layer is representing the ICs of a CoC (Chip-on-Chip) structure. The ICs are covered with a 1µm thick Si3N4 passivation layer. The copper traces at the upper and lower contact surface have a height of 0.5µm and a width of 32µm with a pitch of 40µm. The Fe-Model of the µ-bump is shown in figure 11.

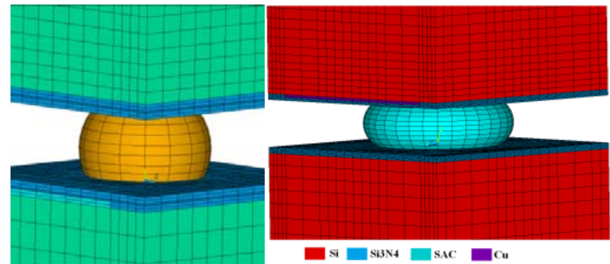

Figure 11: Flip-Chip SAC bump and µ-bump.

The µ-bumps show a strong current crowding as well as high temperature gradients. Due to this EM and TM may occur for smaller applied currents in comparison to BGA bumps. In figure 12 the maximum mass flux divergence for the SAC BGA bump as well as µ-bump depending on the applied current is shown.

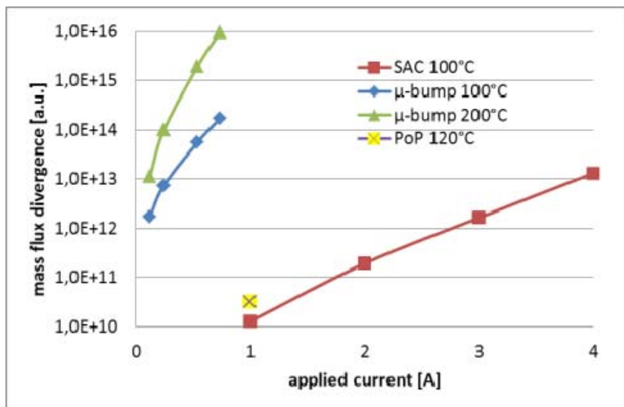

Figure 12: The different materials are indicated by colors. The mass flux divergence vs. the applied current for SAC bump and µ-bump.

TSV AND CIRCUIT DESIGN

3-D IC technology, an advanced IC package architecture, has drawn much interest in semiconductor manufacturing. A 3-D integrated circuit is a chip in which two or more layers of active electronic components are integrated both vertically and horizontally into a single circuit. For this kind of package through silicon vias (TSVs) provide high wiring density interconnection, thus improve electrical performance due to shorter interconnection from the chip to the substrate. However, TSV technology is still facing severe challenges as the physical design problems due to the existence of the copper vias remain resolved. Apart from thermal expansion mismatch, the problems are due in part to many factors including design parameters such as via radius, via aspect ratio, via pitch, chip thickness, and underfill thickness [24].

W-TSVs may outperform Cu-TSVs not only due to its ability to form sub-micron vias, but also W is not a potent diffusant in Si substrate as Cu and it only leaves very minimum stress in active Si owing to smaller difference in coefficient of thermal expansion (CTE) between W and Si. Therefore W-TSV is preferable for high density and high speed TSVs with small diameter and small capacitance for signal lines. However, W-TSV is not suitable for power/ground (GND) lines because of its higher resistance. Cu-TSV with larger diameter and lower resistance should be employed for TSVs for power/GND lines. Cu-TSVs with larger diameter are more preferable to suppress Cu diffusion since a barrier metal such as Ta can be conformal and uniformly formed into deep trench for TSV which effectively suppresses Cu diffusion. The influences of Cu diffusion on device characteristics can also suppress by placing Cu-TSVs for power/GND lines apart from the active areas.

Annealing temperature dependence of mechanical stress induced by TSVs. The mechanical stresses increase with the increase in TSV diameter for both Cu-TSV and W-TSV. The compressive stress was observed in Si substrate between Cu-TSVs when the annealing temperature was lower than 200°C. This tensile stress changed to pure compressive stress not accompanied by the tensile stress when annealed at the temperature higher than 200 °C. Large compressive stress still remained even after annealing at 400 °C although the Cu extrusion (pop-up) was observed [25]. In [24-44] TSV's with different dimensions are given. Due to the different dimensions a interpretation of the thermal-electrical and mechanical influences on the reliability is difficult, caused by the fact that all different cases have to be investigated. In table 3 the ITRS roadmap for TSV's is given [45].

Global Level	*2011-2014*	*2015-2018*
Minimum TSV diameter	4-8 µm	2-4µm
Minimum TSV pitch	8-16 µm	4-8 µm
Minimum TSVdepth	20-50 µm	20-50 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch (thermocompression)	10 µm	5 µm
Minimum contact pitch (solder µbump)	20 µm	10 µm
Number of die per stack	2-5	2-8

Table 3: Dimensions of Interconnect Level 3D-SIC/3D-SOC ITRS roadmap [45].

TSV AND MECHANICAL STRESS

The need of TSV for advanced interconnects has considerably increased in different applications. TSVs packages have many advantages such as improving electrical performances; delivering higher density and higher performance. Nevertheless, TSVs are susceptible to failure due to thermal expansion mismatch between materials during temperature variation. Therefore, the study of the reliability of the through silicon via and of most critical areas for the emergence of failure remains a major concern. Research on TSV reliability and finite element modeling investigations are further needed. In a previous study, [20] three geometric parameters and five material parameters were used in the evaluation of stress and strain in the TSV. The geometrical parameters were the via diameter, the substrate thickness and the copper layer thickness. Materials factors were composed by three quantitative parameters related to copper properties (young modulus, yield stress and ultimate strength) and two qualitative parameters: via filling and TSV substrate. The via filling parameter was used to investigate the effect of the material in the via with the variation of stress and strain. Silicon substrate was compared to ceramic substrate to seek about the effect of substrate properties in the variation of stress and strain. Based on simulation performed in a local model of the TSV and a statistical tool, stress and strain results showed that the interface between copper and silicon is an indicator for a potential failure. Moreover, Young modulus of copper and the via filling mode are mainly influential parameters: using a carpeted via decreases the plastic strain and the stress in the TSV.

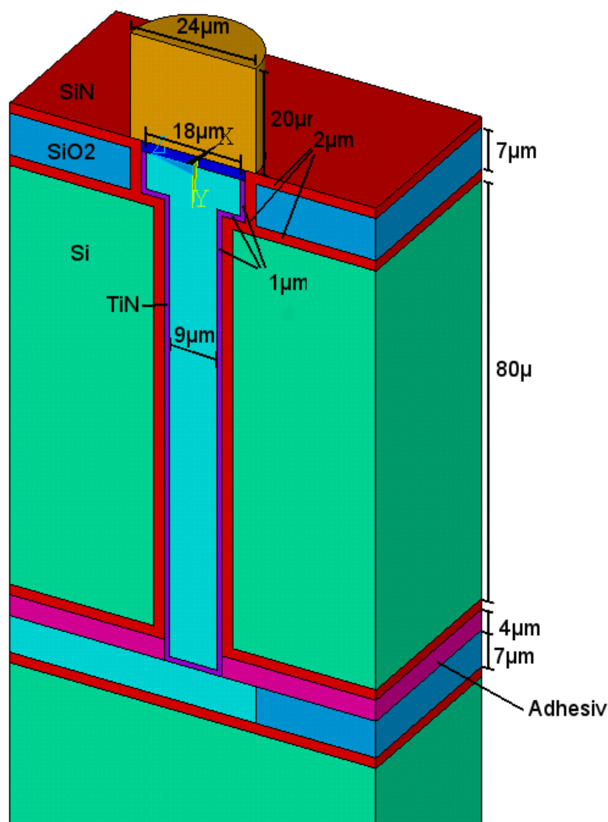

Figure 13: Model of the TSV.

MIGRATION IN A TSV WITH µ-BUMP

In Figure 13 the model of a TSV is shown. The diameter of the TSV was set to 9µm and the height was set to 80µm. The copper barrier in the TSV consists of SiN and TiN. The thickness of the interconnections is 7µm. The passivation on the Device is SiN.

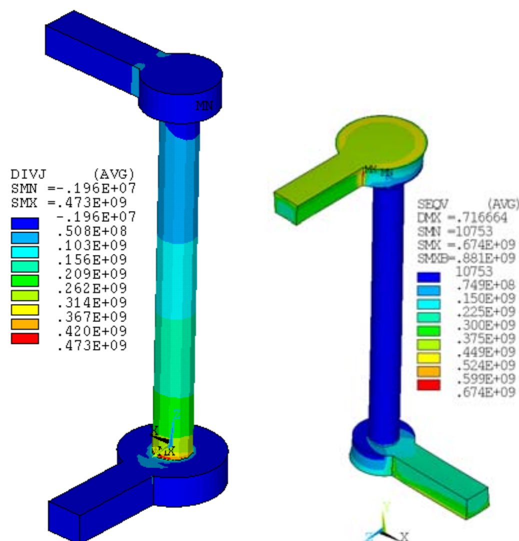

Figure 14: Mass flux divergence distribution upside down (left) and von Mises stress distribution (right).

A typical mechanical von Mises stress distribution is shown in figure 14 right. The maximum values occur in the copper metallization. The maximum mass flux divergences were found at the lower interconnect at the transition of the TSV barrier layers to the interconnect. The µ-bump shows in this case no influence on the electrical behaviour. The mass flux divergences in this case are three orders of magnitude lower compared to the bumps, but increasing applied current as well as enhanced local heating due to current crowding can lead to a reliability problem at this position.

CONCLUSION

With the help of simulations the weakest links as well as locations with high thermal-electrical and mechanical loads can be determined in 3-D applications. In this paper different examples like electro- and thermomigration effects as a failure mechanism in Package on Package PoP-BGA, CuSn pillars, µ-bumps, flip chip with power metal and TSV were presented. Furthermore the influence of the stress distribution on the possible local fracture appearances was shown in a (PoP).

The simulations help to avoid time consuming long term tests and give a hint for the possible failure location. Due to this work intensive micro sections for failure analyses can be placed more easily.

This paper proves that finite element simulation bring a big effort concerning reliability investigations in 3-D integration. In future the process induced stress should also be included in the simulations of bumps.

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REFERENCES

1. Y. Tao, L. Ding, et.al: “Investigation of Thermomigration in Composite SnPb Solder Joints” ECTC 2011, pp 1190-1194
2. K. Weide-Zaage: “Exemplified calculation of stress migration in a 90nm node via structure”, IEEE EuroSimE, 2010.
3. J. Ciptokusumo, K. Weide-Zaage, O. Aubel: “Mechanical Characterization of Copper based Metallizations with different Via-Bottom Geometries”, Physical and Failure Analysis of Integrated Circuits (IPFA), 2010 17th IEEE International Symposium on the Juli 2010, p.1-5I. S, 1963, pp. 271–350.
4. Y. Bulur, R.J. Fishburn, et. al: Electromigration Study on the Interconnects of High Density Power Modules. CHIPS, Nürnberg 2012
5. L. Meinshausen, K. Weide-Zaage, H. Fremont: “Electro- and Thermomigration induced Failure Mechanisms in Package on Package, Micro. Reliability accepted for publication.
6. Y.-S. Lai, K.-M. Chen, et al., “Electromigration of Sn-37Pb and Sn-3Ag-1.5Cu/Sn-3Ag-0.5Cu composite flip-chip solder bumps with Ti/Ni(V)/Cu under bump metallurgy", Micro. Rel., Vol.47 (2007), pp. 1273.
7. Y. Liu, L. Liang, S. Irving et al.:"3D Modeling of electromigration combined with thermal-mechanical effect for IC device and package", Microelectronics Reliability, Vol.48 (2008), pp.818-824.
8. H. Wever, G. Frohberg, P. Adam: “Elektro- und Thermotransport in Metallen“, 1973, Leipzig, Germany.
9. W. Feng, K. Weide-Zaage, F. Verdier: “Electrically driven matter transport effects in PoP interconnections”, IEEE Mechanical & Multi-Physics Simulation, and Experiments in

Microelectronics and Microsystems EuroSimE, 2009.
10. L. Meinshausen, K. Weide-Zaage, H. Fremont: “Virtual Prototyping of PoP interconnections regarding electrically activated mechanisms”, IEEE Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems EuroSimE, 2010.
11. J. Ciptokusumo, K. Weide-Zaage, O. Aubel, Principles for Simulation of Barrier Cracking due to high stress‘,Proc. 11nd Int. Conf. Benf. Therm. Mech. Simu. Microelec, EuroSimE 2010.
12. A. Syed, K. Dhandapani, et.al: “Cu Pillar and μ-bump Electromigration Reliability and Comparison with High Pb, SnPb, and SnAg bumps, IEEE Electronic Components and Technology Conf. 2011, pp. 332-339.
13. ANSYS®, Inc. Software products, multiphysics, ANSYS, Inc. Southpointe, Canonsburg (PA), USA
14. P.G. Shewman: „Diffusion in Solids“, Mac Graw-Hill Series in Materials Science and Engineering, 1963/1989.
15. Huffman, A.; Lueck, M.; et. al: “Effects of Assembly Process Parameters on the Structure and Thermal Stability of Sn-Capped Cu Bump Bonds”, ECTC Conf. 2007, pp. 1589-1596.
16. Syed, A.; Dhandapani, K. et. al: “Cu Pillar and μ-bump Electromigration Reliability and Comparison with High Pb, SnPb, and SnAg bumps, IEEE Electronic Components and Technology Conf. 2011, pp. 332-339.
17. Labie, R.; Limaye, P.; et. al: „Reliability testing of Cu-Sn intermetallic micro-bump interconnections for 3D-device stacking“, IEEE/Electronics-System-Integration-Conference (ESTC), Berlin, September 2010.
18. Meinshausen, L.; Weide-Zaage, K.; et. al: „Electro- and Thermomigration in Microbump Interconnects for 3D Integration“, IEEE Electronic Components and Technology Conf., June 2011, pp. 1444-1451.
19. Z. Xuefeng, W. Yiwe, I. Jang-Hi: “Chip–Package Interaction and Reliability Improvement by Structure Optimization for Ultralow-k Interconnects in Flip-Chip Packages”, IEEE Trans. Dev. Mat. Tech., Vol. 12, No. 2, 2012, pp. 462-469.
20. S. Barnat, H. Frémont, et. al.: “Design for reliability: Thermo-mechanical analyses of Stress in Through Silicon Via”, IEEE - EuroSimE (2010)
21. Knickerbocker, J.U., et al, “Development of next generation system-on-package (SOP) technology based on silicon carriers with fine-pitch interconnection,” IBM J. Res. Dev. 49 (4/5), 2005, pp. 725-754.
22. T. Frank, S. Moreau, et.al: “Electromigration Behavior of 3D-IC TSV Interconnects”, IEEE ECTC 2012, pp.326-330.
23. T. Frank, et al., “Resistance increase due to electromigration induced depletion under TSV”, IEEE International Reliability Physics Symposium (IRPS), 2011, pp. 347-352.
24. C. Kung, T.-T. Liao, et al. : "Parametric Analyses on Fatigue Reliability of 3D IC Packages with Built Through Silicon Vias (TSVs)", Mechatronics and Automation (ICMA), 2012, pp.121-126.
25. M. Murugesan, H. Kino, et al.: "High Density 3D LSI Technology using W/Cu Hybrid TSVs," Electron Devices Meeting (IEDM), 2011, pp. 6.6.1 - 6.6.4
26. M. Jung, D.-Z. Pan, et al.: "Chip/Package Co-Analysis of Thermo Mechanical Stress and Reliability in TSV-based 3D ICs", Design Automation Conference (DAC), 2012, pp.317 - 326.
27. G. Plas, P. Limaye, et al.: "Design issues and considerations for low-cost 3D TSV IC technology" in Proc. IEEE 2010, pp. 148–149.
28. M. Jung, D.-Z. Pan, et al.: "TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC", Computer-Aided Design of Integrated Circuits and Systems, Vol.31 (2012), pp.1194-1207.
29. T. Tanaka, J. Bea, et al.: "3D LSI Technology and Reliability Issues", Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), 2011, pp.1-4.
30. K. Lu, S.-K. Ryu, et al.: "Thermo mechanical Reliability of Through-Silicon Vias in 3D Interconnects", Reliability Physics Symposium (IRPS), 2011, pp. 3D.1.1 - 3D.1.7.
31. M. Koyanagi. : "3D Integration Technology and Reliability", Reliability Physics Symposium (IRPS), 2011, pp. 3F.1.1 - 3F.1.7.
32. T. Frank, C. Chappaz, et al.: "Resistance increase due to electro migration induced depletion under TSV", Reliability Physics Symposium (IRPS), 2011, pp. 3F.4.1 - 3F.4.6.
33. H. Kitada, N. Maeda, et al.: "Diffusion Resistance of Low Temperature Chemical Vapor Deposition Dielectrics for Multiple Through Silicon Vias on Bumpless Wafer-on-Wafer Technology", The Japan Society of Applied Physics, 2011, Vol.50 (2011), pp. 05ED02.34.
34. F. Carson, K. Ishibashi, et al.: "Development of super thin TSV PoP", CPMT Symposium Japan, 2010, pp. 1-4.
35. P. Ramm, M.J. Wolf, et al.: "Through Silicon Via Technology Processes and Reliability for Wafer Level 3D System Integration", ECTC 2008, pp. 841-846.
36. S. Yoon, K. Ishibashi, et al.: "Development of super thin TSV PoP ", CPMT Symposium Japan, 2011, pp 1-4.
37. K. Fujimoto, N. Maeda, et al.: "Development of Multi-Stack Process on Wafer-on-Wafer (WOW)", CPMT Symposium Japan, 2010, pp 1-4.
38. V. Sukharev, E. Zschech, et al. : "Multi-Scale Environment For Simulation And Materials Characterization In Stress Management For 3D IC TSV Based Technologies Effect Of Stress On The Device Characteristics", American Institute of Physics (AIP),Vol.1378(2010), pp.21-49.
39. X. Xu, A. Karmarkar, et al.: "3D TCAD Modeling For Stress Management In Through Silicon Via (TSV) Stacks ", American Institute of Physics (AIP), Vol.1378(2010), pp.53-66.

40. K. Yeap, U.-D. Hangenb, et al.: "Nanoindentation Study Of Elastic Anisotropy Of Cu Single Crystals And Grains In TSVs" , American Institue of Physics(AIP),Vol.1378(2010), pp.121-128.
41. I.-D. Wolf, "Raman Spectroscopy Analysis Of Mechanical Stress Near Cu-TSVs", American Institue of Physics (AIP),Vol.1378(2010), pp.138-149.
42. S.-K. Ryu, K. Lu, et al.: "Stress-Induced Delamination Of Through Silicon Via Structures"", American Institue of Physics (AIP),Vol.1378(2010), pp.153-167.
43. S. Niese, P. Karmarkar, et al.: "NanoXCT A High-Resolution Technique For TSV Characterization", American Institue of Physics (AIP),Vol.1378 (2010), pp.168-173.
44. M.-C. Hsieh, S.-T. .Wu, et al.: "Nonlinear thermal Stress Analysis and Design Guidelines for Through Silicon Vias (TSVs) in 3D IC integration", Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2011, pp.75-78.
45. itrs.net/Links/2011Winter/PublicPresentations.html