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PCB Manufacturability and Reliability Solutions for Fine Pitch PCB Server Boards

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Abstract
Industry demand for high-speed server product performance such as PCI express requires higher pin counts in order to support memory channels which in turn is driving pitch reduction in the printed circuit board (PCB). To provide better signal integrity for high-speed signals, ultra-low loss (ULL) PCB materials may need to be used, and back drilling is recommended to remove via stubs and minimize signal loss. Back drilling is the process whereby plated through holes (PTH) are drilled from the stub-side of the PCB with a larger drill diameter (i.e. back drill) to a specified depth in order to reduce the stub length. This improves signal integrity by minimizing interference or signal loss due to excess stub length. Current industry back drilling capabilities have supported greater than 1mm pitch with a minimum back drill-to-metal gap of greater than 0.15 mm. For pitches < 1mm, the drill-to-metal gap will need to be reduced to less than 0.15 mm. In addition, primary drill (PD) diameters will need to scale down. These changes pose manufacturability challenges with primary drill registration and higher aspect ratios (i.e. PCB thickness/PD). Reduced spacing compounded with drill registration issues can result in exposed copper, slivers//clipped traces, and layer-to-layer misregistration. Industry PCB manufacturing capability and experience with these finer pitches is immature. Next-generation server platforms will push the limits of current PCB industry capabilities, creating a need to identify and provide solutions to enable future manufacturing technologies for server PCBs requiring < 1 mm (0.94 mm) pitch designs. This paper will assess PCB vendor drill registration capability and will also evaluate PCB reliability using electrochemical migration (i.e. conductive anodic filament or CAF) and via reliability (i.e. interconnect stress testing or IST) testing. PCB manufacturing capability will be characterized as a function of back drill-to-metal gap capability and provide potential solution paths to enable PCB suppliers to fabricate reliable 0.94 mm pitch server boards.

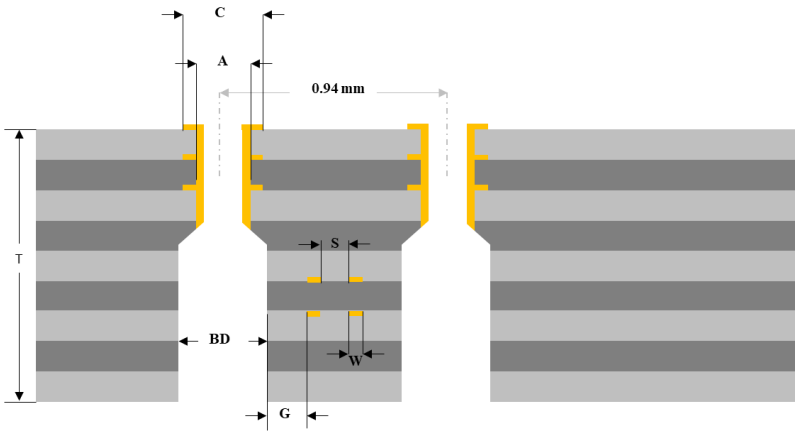
1.0 Introduction

Industry trends for faster high-speed busses such as future generations of PCI express require greater routing density [1]. In order to achieve faster speeds and better signal integrity, there may be a need to adapt back drilling into server designs. In addition, the potential need to adopt thicker PCB stack-ups into ~1.0 mm to 0.94 mm pitch designs to accommodate increased routing density increases the aspect ratio (i.e. PCB thickness/Primary Drill (PD)) during the drilling process. Customers may also choose to use ultra-low loss (ULL) PCB materials to improve electrical performance, which in turn requires a better understanding of the PCB processing, manufacturability, and reliability of these materials.

Figure 1 shows the server design evaluated in this work. The current work evaluates a 0.94 mm pitch design with an aspect of ~13:1 (i.e. 2.55 mm PCB Thickness/0.2 mm PD), but it is anticipated that even higher aspect ratio designs may be required in the future in order to accommodate increased routing density. PCB designs with aspect ratios ≥ ~13:1 pose higher risks for internal Electrochemical Migration (ECM), including CAF due to PD and back drill (BD) misregistration and via reliability. The current PCB industry BD diameter capability is (PD+0.2 mm), with (PD+0.150 mm) considered advanced by many PCB fabricators. With the trend of server designs moving to higher aspect ratios, combined with a BD-to-metal gaps (G) < 0.15 mm, this further exacerbates risks for non-traditional CAF and ECM failures due to the BD process.

CAF is a special type of electrochemical corrosion failure mode that occurs in PCBs. CAF was first discovered by Bell Labs researchers in 1976 [2-3], and later named in 1979 [4]. The CAF failure occurs under temperature-humidity-bias (THB) conditions, where a compound copper containing compound grows typically along the polymer glass interface from the anode towards the cathode; eventually forming a bridge and catastrophic failure (refer to Figure 2). Plated through-hole (PTH)-to-PTH conductor orientations are the most susceptible to CAF failure, and thus most work to date has focused on this type of conductor orientation. Ready et al [5] was the first to identify CAF to be atacamite ($Cu_2(OH)_3Cl$). Caputo et al [6] was the first to discover that the pre-cursor formation was CuCl, and when the powered PCB is exposed to a humid environment, the atacamite compound forms electrochemically. Since the failure mode related to back drill is nontraditional CAF, the authors will refer to this failure mode as a corrosion copper compound which can include dendrites, corrosion, or

CAF (represented by the green compound in Figure 3). When copper is exposed during the back-drill process, a growth path is provided for a copper containing compound or a conductive path type failure when the PCB is exposed to temperaturehumiditybias (THB) conditions



	Design Rule	Design Parameters
A	Primary Drill (PD) Diameter (mm)	0.2
BD	Back drill (BD) Diameter (mm)	0.4
G	BD-Metal Gap (mm)	0.125
C	PTH Pad Diameter (mm)	0.450
W	Trace Width (mm)	0.09
S	Trace Space (mm)	0.1
T	PCB Thickness (mm)	2.55

Figure 1: Current and future design rules for server PCBs using two-track routing

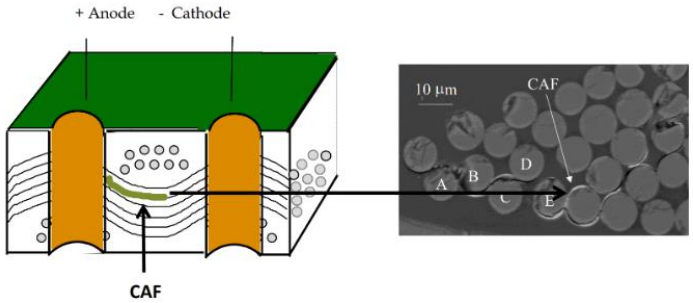


Figure 2: Traditional CAF failure for a PTH-PTH conductor orientation [4]

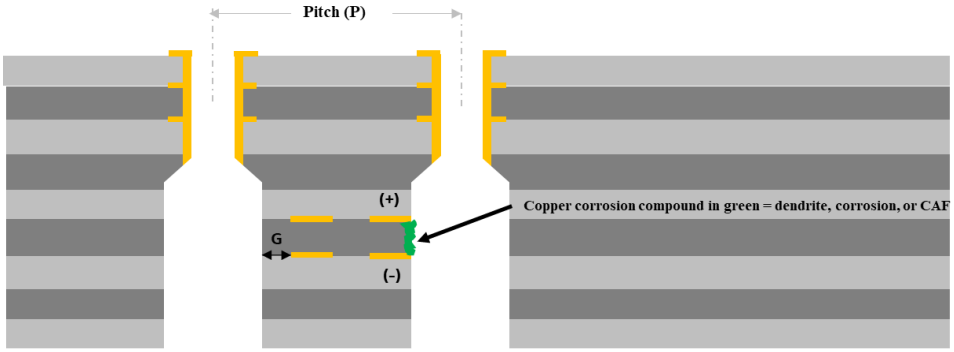


Figure 3: CAF or ECM failure mode related to BD

The movement to finer pitches requires smaller primary drill diameters. The combination of finer primary drill diameters with thicker PCB designs results in higher aspect ratios. The work by Knadle [7-8] first reported that the adoption of higher soldering temperature during the surface mount technology (SMT) process due to lead-free soldering of the BGA to the PCB combined with the cycling of the end product during normal use conditions posed via reliability concerns. The high aspect ratios and z-axis expansion/contraction due to the coefficient of thermal expansion (CTE) mismatch between the PTH copper

plated hole wall and the PCB laminate created the reliability concerns. One way to test for via reliability is by inducing thermal stress via a current and monitoring resistance change – this test is known as an interconnect stress test (IST). The details of this test have been adopted into a standard by IPC and can be found in the IPC-Test Manual TM 650, Number 2.6.26. Others have covered IST testing elsewhere, and the reader can refer to those publications [9-10]. The focus of this work is to get a better understand of the via reliability for back drill vs. standard plated thru-hole for plugged and unplugged vias. Due to minimal via reliability risks for back drilled vias (Figure 4 a), the focus of this paper will be on PTH via reliability concerns (i.e. Figure 4 b). The three predominant via failure modes highlighted in Figure 4 b that will be focused on in this paper are 1) PTH barrel cracking, 2) post-separation, and 3) corner/knee cracks for aspect ratios of (2550/200 ~13:1) on an ultralow loss PCB material.

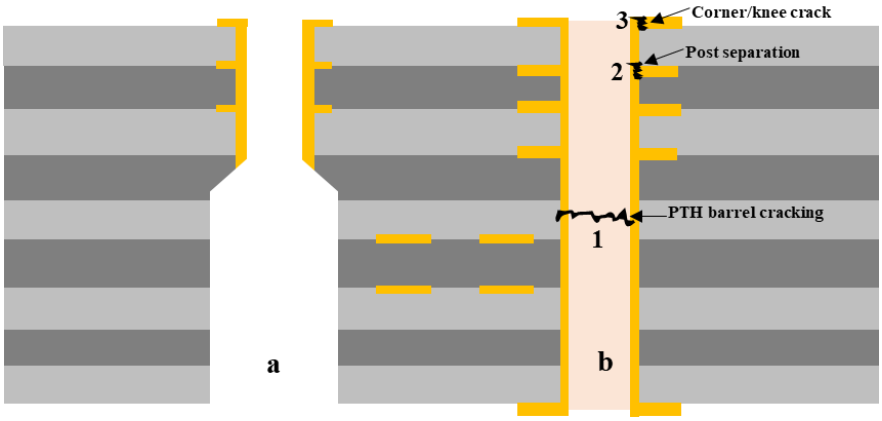


Figure 4: Via Reliability Failure Modes

The current trend towards finer pitches and higher aspect ratio server boards may require the adoption of back drill & the use of ultra-low loss (ULL) PCB materials to improve electrical performance. Limited information is currently available to the PCB industry on the PCB processing and manufacturability of ULL materials, and minimal PCB level reliability studies have been performed on these materials for back drill-to-metal gaps (G) < 175 µm. This paper will discuss: i) the current via registration capability of PCB suppliers, ii) CAF risks associated for G ≤ 175 µm, and iii) via reliability for aspect ratios of ~13:1.

2.0 Experimental Set-up

The DOE test board utilized a 2-up server mainboard to mimic a real-world product. The DOE test board was ~417 mm x ~480 mm, and different test vehicles were placed on it. Figure 5 and Table 1 summarizes the five different test vehicles included in the DOE test board. The CAF, IST, & via registration test vehicles on the DOE test board were manufactured using both 0.2 mm and 0.25 mm PD, but due to time constraints, only the coupons manufactured with the 0.2 mm primary drill were tested. The serpentine coupon with a minimum trace width of 0.075 mm, & trace space of 0.1 mm was evaluated, but the results will not be discussed in this paper. The stub-length coupon was also included on the DOE test board, but was not evaluated due to time constraints, and will not be discussed in this paper.

Table 1 – Test Vehicles on the DOE Test Board

Test Vehicle	Structure	Location on Panel	Plugged	Primary Drill (mm)	Tested
CAF	X & Y Structure	Edge	No	0.2	Yes
CAF	30°	Edge	No	0.2	No
CAF	X & Y Structure	Center	Yes	0.2	Yes
CAF	30°	Center	Yes	0.2	No
IST	N/A	Edge	No	0.2	Yes
IST	N/A	Center	Yes	0.2	Yes
Via Registration (REG)	N/A	Edge	No	0.2	Yes
Via Registration (REG)	N/A	Center	No	0.2	Yes
Serpentine (SERP)	Comb	Center	No	N/A	Yes
Stub length (STUB)	N/A	Center	No	0.2	No

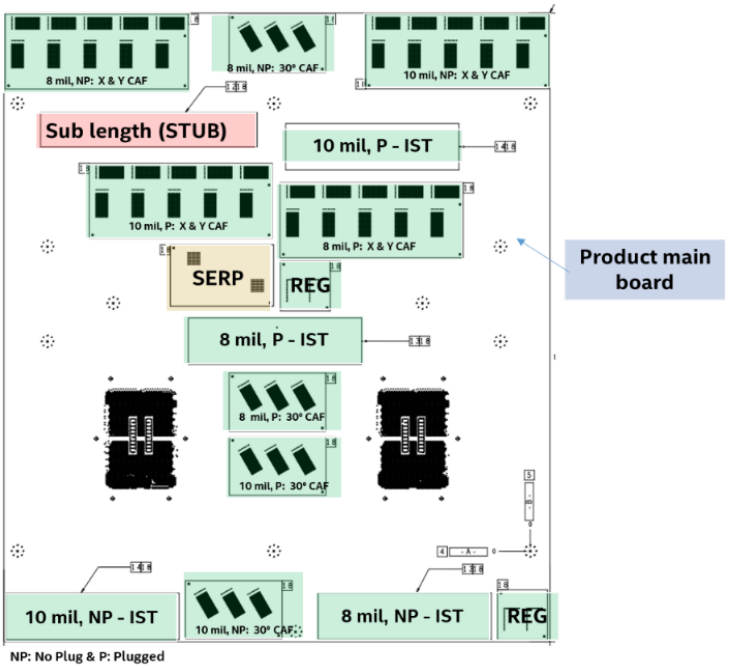
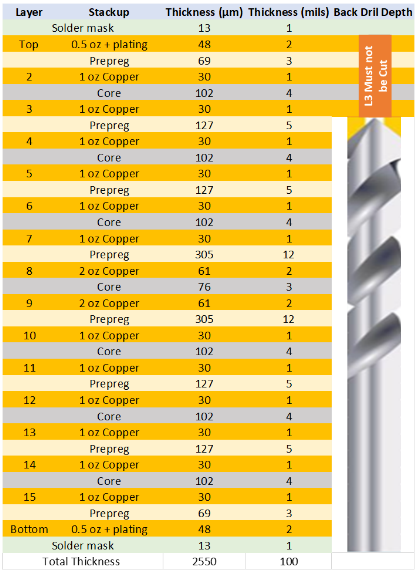


Figure 5: Layout of the DOE test vehicle with different test vehicles

2.1 PCB Stack-up and Back Drill (BD) Depth

The PCB stack-up was a 16 layer, ~2.55 mm (100 mil) thick PCB. The general stack-up and the back-drill depth is shown in Figure 6. Each supplier was able to select the prepreg thickness and glass but was required to ensure that the PCB thickness tolerance was ±10%, and the back-drill "must not be cut" layer was L3.



Layer	Stackup	Thickness (µm)	Thickness (mils)	Back Dril Depth
	Solder mask	13	1	
Top	0.5 oz + plating	48	2	
	Prepreg	69	3	
2	1 oz Copper	30	1	
	Core	102	4	
3	1 oz Copper	30	1	
	Prepreg	127	5	
4	1 oz Copper	30	1	
	Core	102	4	
5	1 oz Copper	30	1	
	Prepreg	127	5	
6	1 oz Copper	30	1	
	Core	102	4	
7	1 oz Copper	30	1	
	Prepreg	305	12	
8	2 oz Copper	61	2	
	Core	76	3	
9	2 oz Copper	61	2	
	Prepreg	305	12	
10	1 oz Copper	30	1	
	Core	102	4	
11	1 oz Copper	30	1	
	Prepreg	127	5	
12	1 oz Copper	30	1	
	Core	102	4	
13	1 oz Copper	30	1	
	Prepreg	127	5	
14	1 oz Copper	30	1	
	Core	102	4	
15	1 oz Copper	30	1	
	Prepreg	69	3	
Bottom	0.5 oz + plating	48	2	
	Solder mask	13	1	
	Total Thickness	2550	100	

Figure 6: Stack-up and Back drill depth

2.2. DOE Test Matrix

As was mentioned in section 2.1, due to time constraints and testing capacity, the focus of this study was on future product design requirements (i.e. primary drill = 0.200 mm). Each supplier built 30 panels following their regular high volume manufacturing (HVM) process flow and manufactured the DOE test boards in their HVM factories. Each supplier was required to use the same ultra-low loss (ULL) PCB and plugging material. Suppliers were given the freedom to run scout lots if they chose to do so. The DOE test matrix is summarized in Table 2.

Table 2 – DOE Test Matrix

PCB Supplier	Via Plugging	*Drill Diameter (mm)	Number of Panels	PCB material	Plugging material
A	No	0.2	30	ULL E	F
**B					
C					
A	Yes				
B					
C					
A	No	0.25			
**B					
C					
A	Yes				
**B					
C					

***The focus of this study is the product design primary drill diameter of 0.2 mm; **0.175 mm BD-metal was not evaluated**

2.3 Testing, Failure Modes, and Pass/Fail Criteria

The failure modes and test conditions are summarized in Table 3.

Table 3 – Testing Conditions

Test	Failure Mode	Test	Pass Criteria
CAF	Exposed copper/Slivers/drill damage	**Test:** 85 C/85% RH/25 V **Pre-condition:** 6X reflow	*Insulation Resistance ≥ $1x10^8$ Ω
IST	via barrel cracking & post separation	**Test:** Cycling from 25 °C-150 °C **Pre-condition:** 6X reflow	500 cycles with resistance change < 10%
Via Reg.	Shorting	Electrical	Open

***1 or 2-decade drops in insulation resistance (IR) were allowed throughout the test, but IR < $1x10^8$ Ω were not allowed in this test.**

3.0 Via Registration

The registration coupon shown in Figure 7 had the ability to evaluate primary drill registration for both 0.2 mm & 0.25 mm drill diameters. The data presented in this paper will focus on the 0.2 mm primary drill. The coupon was designed with ring structures increasing in increments of 0.025 mm (1 mil). The registration could be monitored layer by layer, but the registration value recorded was the value where all layers passed (i.e. no shorting).

Figure 8 shows that primary drill (PD) registration varies from supplier to supplier, with supplier A having the best PD registration, and suppliers B & C have about the same PD registration. The red line in Figure 8 represents where the drill will begin to expose metal on a design with a BD to metal gap of 0.125 mm. Supplier C had two data points that fell above the 0.125 mm red line, but these appear to be outliers. Further, CAF risks exist above the yellow dashed line because of potential back drill, layer-to-layer misregistration, and mechanical damage due to drilling which may trap plating salts and/or processing chemicals, which become conductive when exposed to temperature-humidity-bias (THB) conditions. Figure 9 shows an example where: (a) PD & BD are perfectly registered, (b) PD is misregistered by 0.075 mm, and the BD is perfectly registered off the PD, which results in a BD-metal gap of 0.05 mm, and (c) the cumulative effect of both the PD & BD each being misregistered by 0.075 mm, which would result in exposed copper. The data suggest that BD-metal gaps less than 0.175 mm are manufacturable by all suppliers, but there are some potential risks of exposed copper during the BD process, and thus plugging may be required to mitigate CAF risks. The data in this paper does indicate that supplier drill registration capability does vary from supplier to supplier, and it is important for customers to work with their PCB suppliers to optimize drilling capabilities.

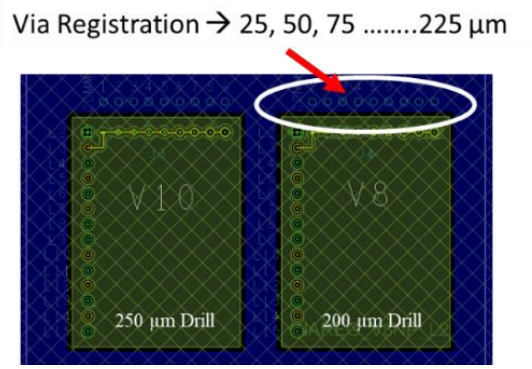


Figure 7: Via registration Coupon

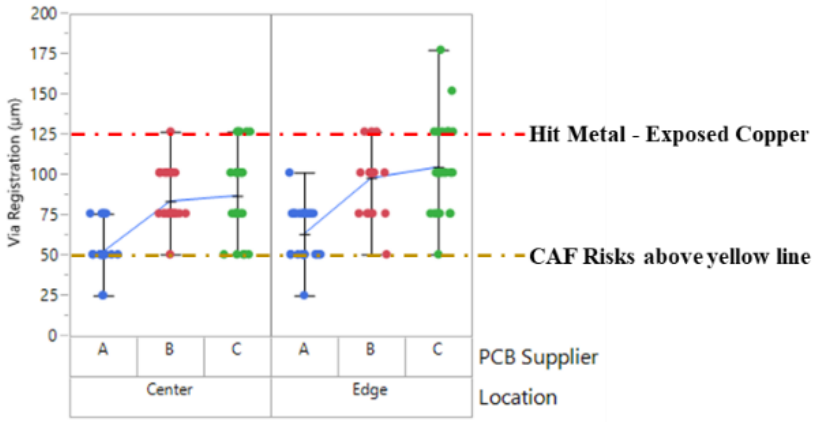


Figure 8: Variability plot showing the registration values using a PD of 200 µm for suppliers A, B, & C

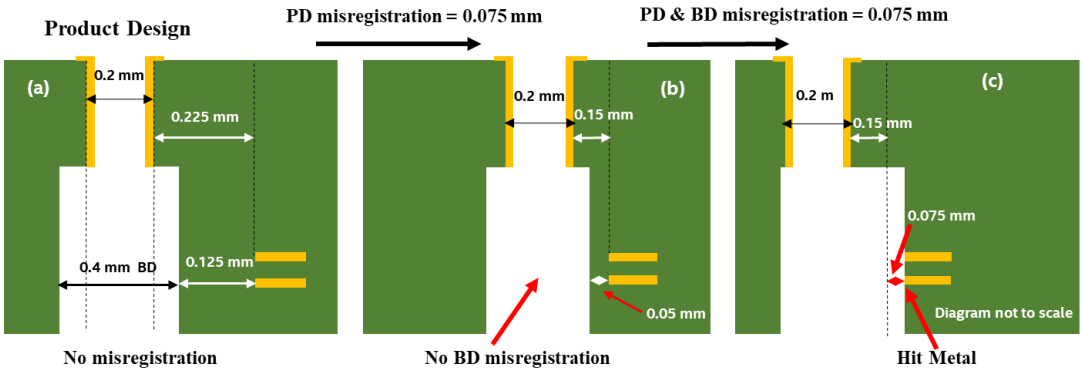


Figure 9: Example showing perfect registration, and PD and BD misregistration

4.0. Electrochemical Migration and Conductive Anodic Filament (CAF)

As was mentioned in section 3.0, PCB suppliers can manufacture server designs with BD-metal gaps less than 0.175 mm, but drill registration capability could result in exposed copper. Exposed copper poses CAF or other ECM risks, thus a better understanding of how to mitigate these risks due to back drilling is required. As was previously mentioned, most work on CAF has focused on the hole-to-hole conductor orientations because this conductor orientation is most susceptible to CAF failure. However, to the best of the author's knowledge, no CAF work has been published focusing on the CAF failure mode related to back drilling. The potential CAF or ECM failure mode related to back drill was previously discussed in section 1.0 (refer to Figure 3). The highest CAF or ECM risk posed during the back drill process is exposed copper or the reduction in the BD-Metal gap (G). If the design gap (G) is reduced to 0 µm (i.e. exposed copper) due to primary drill plus back drill misregistration, this can result in a copper corrosion product (i.e. represented in green in Figure 3) when exposed to temperature-humidity-bias (THB) conditions. This corrosion product can be CAF, dendrites, or some other corrosion product. If G is less than 0.175 mm, mechanical damage at the polymer glass interface during the back drill process can result in trapped plating salts and/or processing chemicals, which become conductive when exposed to temperature-humidity-bias (THB) conditions and result in the degradation of the insulation resistance (IR).

4.1 CAF or ECM BD Test Vehicle

The CAF test vehicle shown in Figure 10 had nominal BD-to-metal gaps of 0 mm, 0.1 mm, 0.125 mm, 0.15 mm, & 0.175 mm, with the BD depth discussed in Section 2.1, Figure 6. Each gap had an X & Y structure ganged into a single measurement point. The BD-to-metal gap of 0 mm (i.e. purposely exposed copper) was included as a sanity check, but will not be discussed in the paper. Coupons with and without via plugging were evaluated. The focus of this paper will be on the CAF and ECM results of coupons manufactured with the 0.2 mm primary drill. The sample size was 22 coupons. CAF testing followed IPC-TM-650, 2.6.25: "Conductive Anodic Filament Resistance Test: X & Y", where Insulation Resistance (IR) values were monitored every 6 hours. It must be noted hard fails (i.e. IR < $1x10^8$ Ω were not allowed throughout the entire tests). 1- or 2-decade IR drops were allowed.

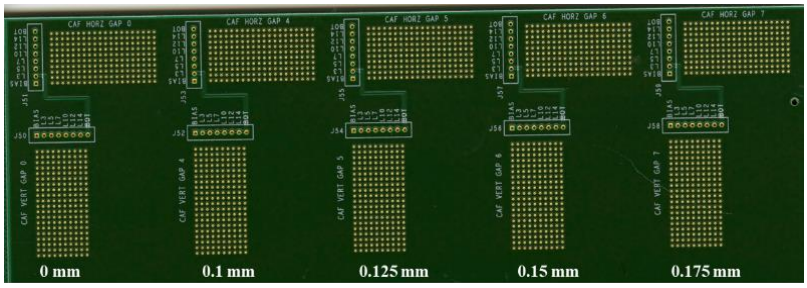


Figure 10: CAF or ECM test vehicle

4.3 CAF or ECM Results

The CAF results are summarized in Table 4. The results show that there are some CAF or ECM risks associated with BD-metal gaps of ≤ 0.175 mm. "Medium risk" equaled at least 1 coupon failing the CAF requirement (i.e. insulation resistance < 1 x 10^8 Ω). Plugging is a solution to mitigate CAF risks. For supplier B some marginal fails were observed, but the FA revealed that the BD wall/plugging material interface had some weak points or separation combined with some misregistration, which in turn allowed moisture to diffuse into this interface, creating conductive paths and marginal IR drops. With the optimization of the plugging process, this will be low risk and hence reflected in Table 4.

Table 4 – Summary of CAF or ECM Results

Supplier	Unplugged Vias				Plugged Vias			
	BD-Metal gaps (mm)				BD-Metal gaps (mm)			
	0.1	0.125	0.15	0.175	0.1	0.125	0.15	0.175
A	Medium Risk	Medium Risk	Medium Risk	Medium Risk	Low Risk	Low Risk	Low Risk	Low Risk
B	Medium Risk	Medium Risk	Medium Risk	Medium Risk	Low Risk	Low Risk	Low Risk	Low Risk
C	Medium Risk	Medium Risk	Medium Risk	Medium Risk	Low Risk	Low Risk	Low Risk	Low Risk

5.0. Interconnect Stress Test (IST)

The smaller via design rules and thicker PCB described previously results in an aspect ratio of ~13:1 for the design under consideration. In addition, there was limited internal IST data on the specific laminates under consideration for these designs. Based on the previous IST testing these factors elevated the concern for potential reliability risks with the via designs and motivated an initial IST experiment to begin to quantify the risk.

5.1 IST test vehicle

Standard IST coupon designs were created. The coupon of interest for this discussion consisted of two tests (i.e. sense) circuit types. One circuit tested the PTH via, and a second tested the same 200um PTH structure but with an included backdrill. As captured in Table 1, the location of these coupons on the production panel varied between an approximate central location and a location near the panel edge. Additionally, the back drilled coupons at the center of the panel were epoxy filled. Due to time constraints, a total of 8 coupons per supplier were tested.

5.2 IST Results

A summary of the results for the initial IST experiment is shown in Table 5. As can be seen in the results table there were some failures based on the 500 cycle criteria. Improving the reliability of these failed structures will be the focus of future work.

While the pass criteria for this initial experiment was 500 IST cycles, all coupons were set to run through 2000 cycles or until a complete failure occurred (i.e. failure of both sense circuits, or failure of the power circuit). As expected, the reduced aspect ratio of the back drilled vias resulted in zero failures. An unexpected result was the distribution of coupons that eventually failed for post-separation on the power circuits.

Post-separation failure on power circuits summary:

- 100% of center coupons failed before reaching 2000 cycles
- 100% of vendor C coupons failed before reaching 2000 cycles

Again, these power circuit failures were well above the 500 cycle threshold, but the frequency of occurrence makes the root cause worth investigating.

Table 5 – Summary of IST Results

Supplier	Drill Diameter (µm)	Panel Location	Plugged	Circuit Type	IST Result
A	200	Edge	No	PTH	**Fail**
				Back drill	**Pass**
		Center	Yes	PTH	**Pass**
				Back drill	**Pass**
B	200	Edge	No	PTH	**Pass**
				Back drill	**Pass**
		Center	Yes	PTH	**Pass**
				Back drill	**Pass**
C	200	Edge	No	PTH	**Pass**
				Back drill	**Pass**
		Center	Yes	PTH	**Fail**
				Back drill	**Pass**

6.0 Conclusion

The movement to high-speed server designs in order to meet customer demands for better electrical performance may result in higher demand in the future for the adoption of back drilling in the PCB manufacturing process. Ultra-low loss (ULL) PCB materials may also be needed to satisfy the electrical performance requirements. Limited PCB manufacturing and reliability data exist for future fine pitch designs using BD-metal gaps < 0.175 mm and ULL materials. This work found that PCB fabricators tested in this study are capable of manufacturing server designs with PD registration ranging from ~ 0.050 mm to 0.125 mm, but there is variability from supplier to supplier. The data suggests that designs that have BD-metal gaps ≤ 0.175 mm could result in exposed copper or a reduced BD-metal gap due to drill misregistration. If the copper is exposed or mechanical damage with a reduced BD-metal gap occurs due to drill misregistration, this could pose CAF or ECM risks. This work found that plugging is a solution to mitigate CAF risks for BD-metal gaps at ≤ 0.175 mm. The IST data shows that there may be some via reliability risks for higher aspect ratio PCB designs, and a better understanding of the PCB suppliers drilling, and the plating process is required. Failure analysis and more testing is required for the current suppliers, and there is a need to test a wider range of ULL material to get a better understanding of the influence of PCB material on the via reliability. It is important for customers to work with there PCB suppliers to better understand the PCB manufacturing process flow and run scout lots during the PCB manufacturing process so that the drilling, plating, scaling of the inner layer registration, and via plugging can be optimized. Further work is also needed to better understand the impact of ULL materials on PCB reliability.

7.0 Acknowledgments

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