

NEW PACKAGING AND INTERCONNECT TECHNOLOGIES FOR ULTRA THIN CHIPS

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ABSTRACT

This paper shows different approaches to use the availability of ultrathin chips for the realization of new packages with high density and improved performance.

For several years technologies have been developed for the embedding of chips in circuit boards in order to achieve 3-D-packages using conventional processes from PCB manufacturing.

Ultrathin chips are suited to be integrated in rigid circuit boards as well as on and in multilayer flexible substrates. The use of interposers prior to embedding can facilitate the embedding of components with ultra fine pitches.

An example for a complex RFID-based product will be shown which is enabled by the integration of ultrathin dies.

INTRODUCTION

A visionary approach for the future production of printed circuit boards was the development of integration technologies for active and passive components in the different layers of the boards. This enables extremely high density of functionality and components in 3 dimensions. The goal is to achieve this progress while maintaining the processes typical for PCB manufacturing. Different approaches have been described for the embedding in FR4 [1,2]. A suitable solution for the integration of chips with very fine pitch is the iBoard technology [3]. It is based on the flip-chip assembly of the fine pitch chips on thin interposers with fan out design.

Besides the rigid organic substrates flexible circuits become increasingly important in PCB industry for applications ranging from consumer products to medical implants. Recent developments – e.g. in the project SHIFT [4,5] – allow the integration of components also in multilayer flex substrates which allows an even higher density with low overall thickness. The technologies which are the prerequisites for this solution and experimental results are shown in this paper.

Important aspects which were investigated for the different new technologies are the constraints regarding pitch and

chip geometries [6]. In order to be embedded in a substrate the components have to be thin. For the integration in rigid circuit boards, 50 μm chip thickness were chosen, for the flexible substrates 20 μm are required.

TECHNOLOGIES

Ultrathin Chips

The wafer thinning is a commonplace procedure in front end wafer fabrication. Typically wafers are thinned down to 120 or 80 μm thickness before dicing into single chips and subsequent packaging. Using commercial thinning services wafer thicknesses of 50 μm are also readily available. Thinning below 50 μm , however, still is critical. This regime is therefore called ultra thin. Wafer handling and dicing becomes more subtle. Micro cracks at edges and corners of chips which may be induced by mechanical dicing are prone to propagate into the bulk of the chips and cause failure. This is especially critical for processes with high mechanical loads like flip chip bonding. For ultra thin chips it is therefore advisable to use a dicing by thinning technique, where separation grooves are etched into the wafer prior to grinding.

In the present studies chips with a thickness of 50 μm for FR4 and 20 μm for flexible multilayers have been used to develop and investigate the performance of two distinct embedding technologies.

Details of the thinning process and the encountered problems have been the topic of several publications [7,8] will not be presented and discussed in the present paper.

Assembly of Ultrathin Chips

It has been shown that ultrathin chips are suitable for flip-chip processes [9]. Especially in combination with flexible substrate it is important to achieve thin flip-chip contacts in similar dimensions as the two contact partners. For chips and substrates down to 10 μm the interconnect height should also not exceed 10 μm .

This is possible with solder as well as adhesive bonding technologies.

Thermode Bonding

For thin solder joint CuSn bump metallurgy is a very good solution. It can be deposited by electroplating with very fine pitch. The bump is formed by plating a thin layer of Sn on top of Cu sockets. Uniformity of the thin layers during electroplating is most important to ensure consistent quality of flip chip bonded assemblies. Bump height deviations of 3% have been achieved using diffuser plating rings in the cup plater. All bumps have been used in the as plated condition without prior reflow process. The reflow would consume already too much of the little solder volume by IMC formation. The topography of a CuSn-bump as plated can be seen in Figure 1.

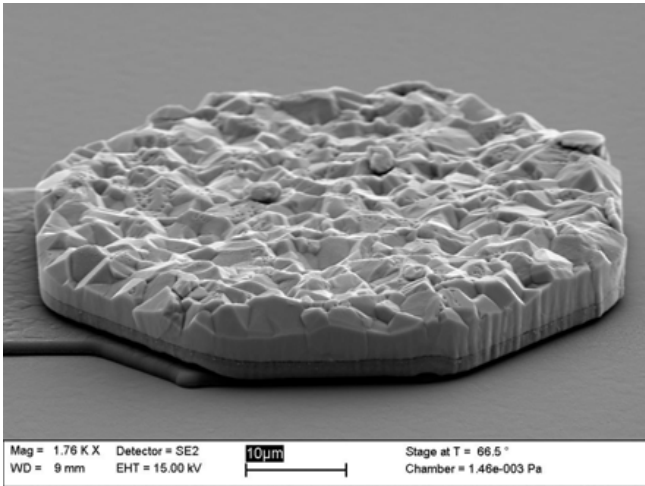


Figure 1: Electroplated CuSn bump on test chip, (bump height 6µm, chip thickness 30µm)

The thermode bonding technology is based on fast reflow soldering by pulse heating. The fast process allows the use of low cost materials with low temperature resistance for flip chip soldering at high temperatures without damage of the flex. It is even possible to apply the underfill material before the placement of the die and perform underfilling and bonding in one step. The preapplication of noflow underfiller can either be done by stencil printing or by dispensing. The use of noflow underfiller today is limited by soldering temperatures. In case of eutectic SnCu solder noflow underfiller was successfully established. A typical thin solder joint is shown in Figure 2.

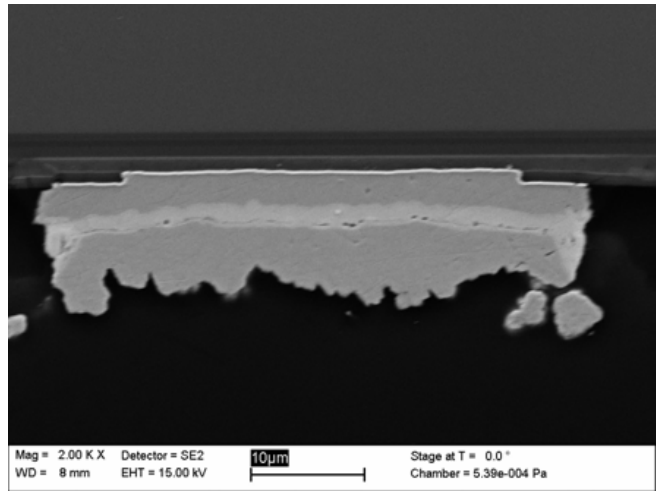


Figure 2: Ultrathin CuSn solder joint

ACA Bonding

Common bumps for ACA technology are either made by mechanical stud bump bonding [6] or various chemical deposition technologies, ranging from evaporation to plating processes. Electroless nickel deposition is often used, as it benefits from its low cost potential [7,8]. The standard electroless nickel UBM for high reliability has a thickness of 5 µm but only a minimum of 1 µm is necessary to have a closed and void free nickel layer [9]. For thin interconnects NiAu with a thickness of 3 µm is used typically. Driver or RFID chips are often available with electroplated Au bumps which are also very well suited for ACA processes. The bump thickness is typically >10µm for the commercial chips but the process works well with 5 µm.

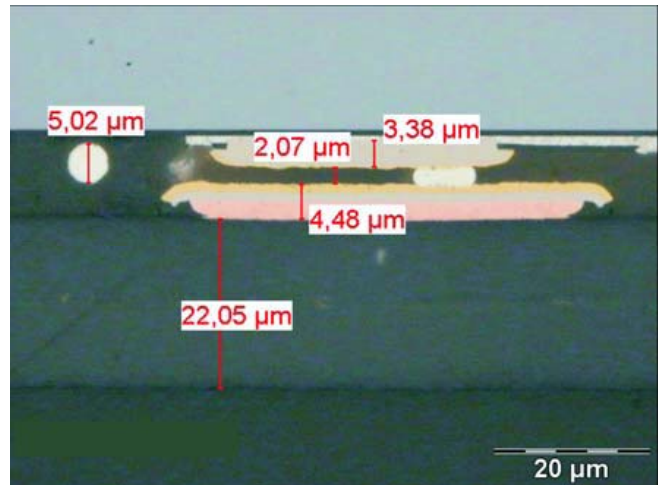


Figure 3: ultrathin ACP contact, on PI thin film substrate with CuNiAu metallization

The ACA bonding process requires pressure to trap electrically conductive particles between the chip bumps and the substrate metallization to form an electrical contact. Applied heat on the bonding tool and chuck is needed to cure the adhesive, which is usually an epoxy based material.

Adhesives are of paste or film form either. A thin contact with NiAu metallization on both sides is shown in Figure 3.

Embedded Flip Chip

In the past flip chip on flex aimed at the highest degree of miniaturization. Recent developments use flip-chip on flex as a prerequisite for embedding.

For the build up of a multilayer flex, commercial PI sheets of 25 μm polyimide with 17 μm thick copper wiring are used. Onto the substrates ultra thin flip chips are mounted. The electrical interconnect is established using either anisotropic conductive adhesive or thin solder interconnects. No difference regarding yield or performance could be found in comparison of those technologies. Multiple flex boards with assembled chips and adhesive foils are then stacked together and laminated in a commercial stage press. Subsequently the layers of the stack are interconnected by through hole drilling and metallization. Finally the outer surfaces of the whole stack are structured.

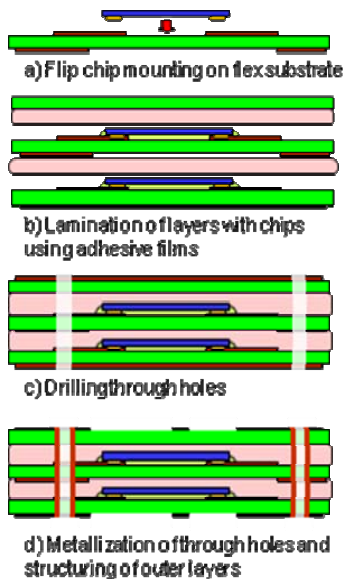


Figure 4: Process flow for the Flip Chip in Flex technology

Using this process flow multilayer flexes with 4 layers of embedded dies and an overall thickness of 450 μm were realized [Figure 5]. No breaking of the chips was observed during lamination.

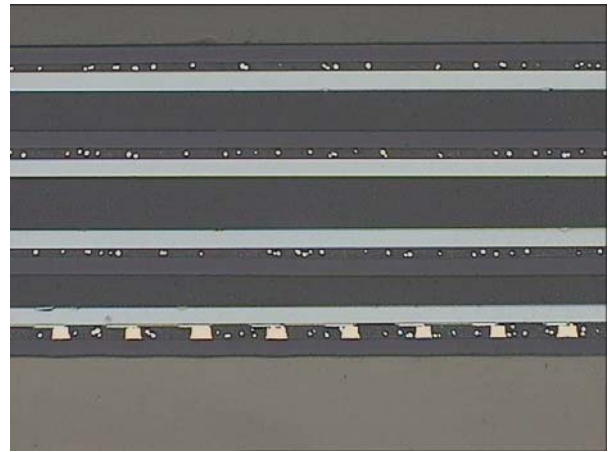


Figure 5: Multilayer flex with 4 layers of embedded dies Embedding in FR4

Ultrathin chips can be integrated in rigid circuit boards by different technologies, e.g. Chip in Polymer [2, 10]. If the pitch of the chips is very fine ($< 100 \mu\text{m}$), it is suitable to assemble the ICs on a flexible interposer (e.g. PI) with thin Cu metallization (5 μm) which enables the required fine structuring.

An example for a driver chip with 50 μm pitch on a thinfilm HiCoFlex [11,12] is shown in Figure 6. The chip thickness is relevant for the yield during the integration process. The chips are typically 50 μm or thinner to avoid damaging of the silicon during lamination. The difference between the ultrathin die and a conventional flip-chip assembly is shown in Figure 4.

For pitches $> 100 \mu\text{m}$ thin FR4 interposers can be applied. The design is a fan out of the I/Os so that the resulting Pitch is uncritical for the following processes. The use of an interposer separates the chip assembly from the embedding process. This interposer can be tested before being integrated in the board.

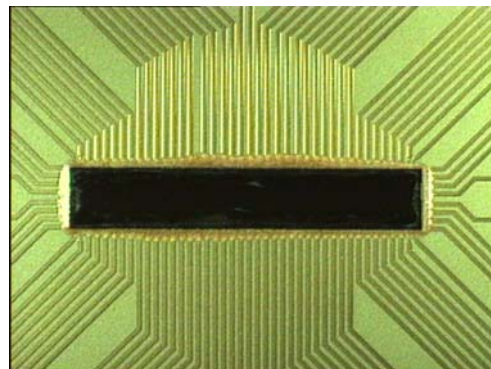


Figure 6: Driver IC with 50 μm Pitch on HiCoFlex

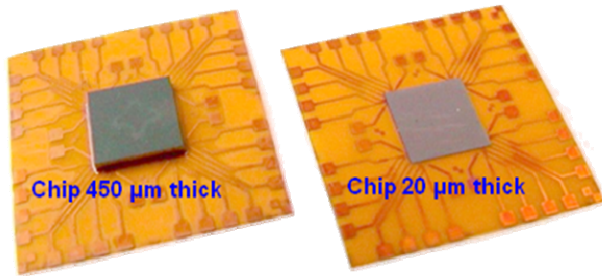


Figure 7: Interposer with thick and thin flip chip in comparison

The interposers are placed between the prepregs of a multilayer and then laminated. Due to the fan out the interposer can be connected by conventional methods which are always used in the manufacturing process of multilayer boards. The process flow is shown in Figure 8. If the interposer is in the neutral area of the build-up the holes are drilled conventionally. For the integration directly underneath the outer layer, the interconnection by laser vias is used successfully.

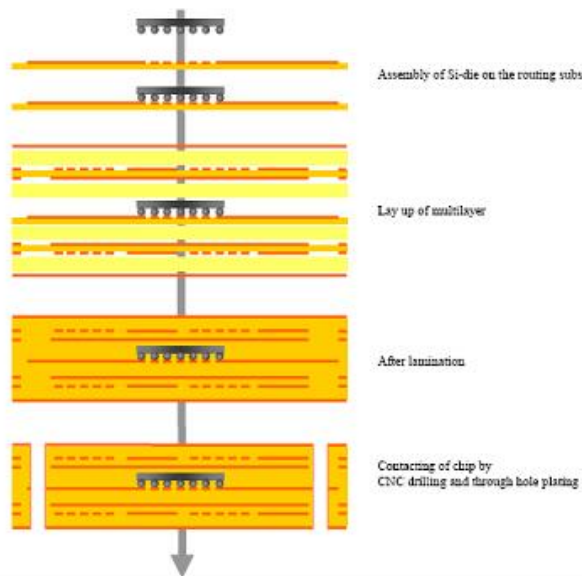


Figure 8: Process flow of iBoard integration process

APPLICATION EXAMPLE

A complex module with 6 integrated ICs is described as an example for flip-Chip assembly of ultrathin chips and the integration in PCB.

The goal was the replacement of paper labels with text and barcode on transport containers for letters. As a solution with high potential for automation a passive RFID-Label with E ink display was developed. Energy and data are transmitted according to ISO15693 to two different antennas (13,56 MHz) which are positioned outside the display area. In order to realize a display with 982 segments and symbols 4 driver ICs with 324 I/Os each were required. These commercial ICs have a pitch of 50 μm. Therefore a flip-chip integration on a conventional printed circuit board is not possible. Depending on the process flow some embedding

technologies do also not yet allow to contact 25 μm pads, e.g. directly by drilling vias to those pads. The integration by iBoard technology was chosen to solve this problem. In a first step the 50 μm thin chips with Au bumps had to be assembled in ACA technology on a thinfilm HiCoFlex interposer [11,12] with CuNiAu end metallization. The overall thickness of the assembled interposer was only 90 μm. The cross section in Figure 9 shows how critical the positioning accuracy is for such fine pitches with a bump distance of < 8 μm.

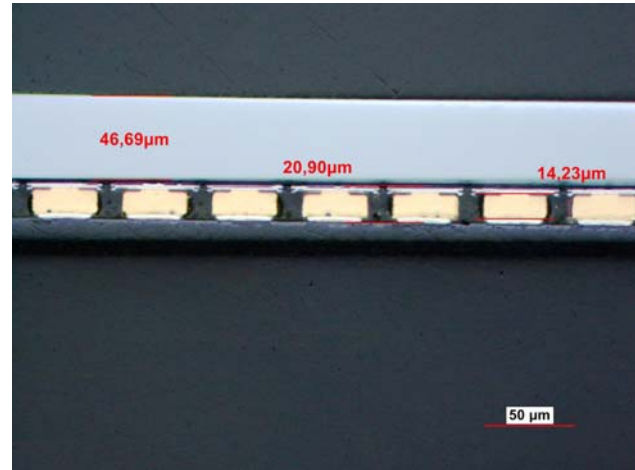


Figure 9: cross section of ACA contacts on thinfilm interposer

The other necessary ICs are a microcontroller and the RFID frontend. As these chips have only minimum pitches > 100 μm, they could be assembled on thin FR4 interposers with Cu end metallization.

The 4 driver interposers, controller interposer and RFID interposer were then integrated in a 6-layer FR4 board as shown in the process flow in figure 8. The driver chips do not break during the lamination process although their geometry is critical (Figure 12). The red mark in Figure 11 shows the position of a driver in an X-ray image of the final board.

A few necessary passive SMD components were then assembled on the back side of the board. On the front side the e-ink FPL was laminated together with protection layers.

Powered by the reader the content of memory and display can be changed even in motion. The display then remains unchanged with high contrast for months without energy supply. The final module is shown in Figure 10.



Figure 10: Display RFID demonstrator with 6 embedded chips and E ink foil (160mm X 65mm X 1mm)

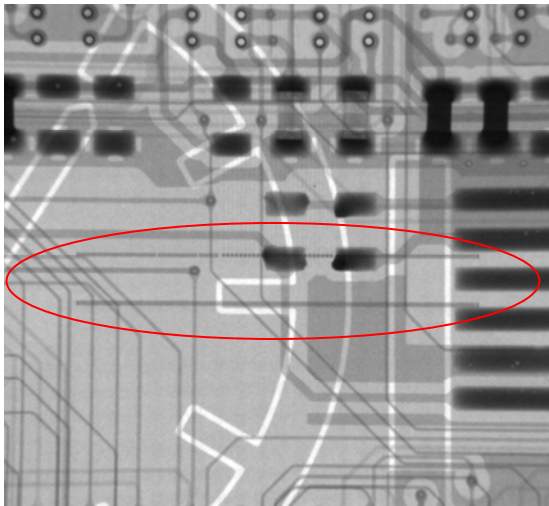


Figure 11: X-ray image of integrated driver IC

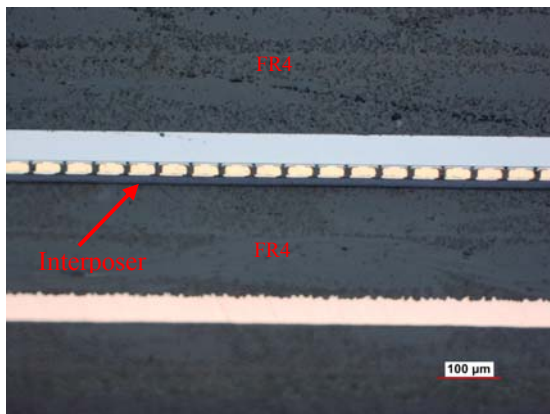


Figure 12: Cross section of integrated driver IC

CONCLUSION

In general the supply of ultra thin chips or components is the bottleneck for the new enabling embedding technologies of active components. The assembly of thin chips can be realized with good results by various flip-chip technologies. Contact thicknesses $< 10 \mu\text{m}$ can be achieved.

Embedding of thin chips in flexible multilayer flexes can be used to obtain thin modules with several layers of active components. As a demonstrator 4 layers with –ICs have been realized with $450 \mu\text{m}$ thickness.

For the integration of chips with pitches $< 100 \mu\text{m}$ the iBoard technology has shown very promising results. Using

either FR4 or thinfilm PI interposers, a wide range of chip types with different bump metallurgies can be integrated with chip thicknesses of $50 \mu\text{m}$ or even higher.

As an example for the potential of this technology a display RFID module with 6 integrated ICs has been described.

Although there are many potential applications for such technologies the manufacturers are reluctant to use modules with embedded components processed in printed circuit board technology. Only the growing necessity to use this technology in order to overcome the gap between chip pitches and line geometries on FR4 has lead to the big interest in recent years. One prerequisite to achieve a higher degree of acceptance would be the availability of the corresponding design tools for this 3D integration to facilitate the design flow.

ACKNOWLEDGEMENTS

The work presented was partially done within funded projects: The project SHIFT was funded by the European Commission and the project Pariflex by the Federal Ministry of education and research.

The authors want to thank Thomas Gottwald and Alexander Neumann from Schweizer Electronic AG for providing the iBoard technology for the display RFID modules.

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