As originally published in the SMTA International Conference Proceedings.

TOOLS AND TECHNIQUES FOR MATERIAL ASSESSMENT IN ADVANCED TECHNOLOGIES

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ABSTRACT

As complexity in advanced manufacturing increases, especially for consumer electronics, the need to characterize the materials and processes used in electronic assembly also increases. OEM and EMS companies look to perform characterizations as early as possible in the process to be able to limit quality related issues and improve both assembly yields and ultimate device reliability. Many analytical methods are available to us on the market that each has their own risks and benefits. This paper will help identify some of these key limitations in the methods used for characterizing and evaluating solders, circuit board materials and surface finishes available in the market today.

BACKGROUND

The real cost of failures in manufacturing is significant but is one that is not accounted for during up front calculations. Line-down situations, product recalls, engineering time spent on customer interactions and failure analysis can quickly add up to millions of dollars depending on the product. It is critical that all resources are optimized in order to effectively determine root cause in the shortest possible timeframe. Unfortunately the industry is moving away from a skilled labor force that can accurately assess failures and determine root cause. Often, too much time is spent tracing false positives and incorrect assumptions leading to ineffective corrective actions and “Band-Aid” solutions. In an industry that values “5S” practices, fishbone diagrams and “5 whys” we have lost our ability to employ intuition and experience. Lean manufacturing practices can be very beneficial for failure analysis since often Lean manufacturing practices are associated with tracking lot and date codes of materials used during production, which can be linked to failures. Having this data can be critical in determining root cause and assessing the extent of a failures effect on a population of fielded products.

To that end we must therefore assess failures using techniques that will be able to isolate material and process variations. Whether it be manufacturing process, material quality issues, product design, excessive stresses (in factory or in field), or an inherent weakness in a material selected for the product (e.g. lead-free solder alloy susceptibility to failure). Most companies do not have the resources to employ a staff of engineers and purchase software to conduct physics of failure (PoF) analysis techniques. Also product modeling techniques may only highlight an area of high stress in an idealized condition. An experienced failure analyst needs to take into account the outliers of a manufacturing process or design in order to properly determine and consequently implement a successful corrective action plan.

This paper will begin by isolating some key questions that can be asked of the supplier, manufacturing engineers, supplier quality engineers, and reliability engineering teams. Once these critical questions have been answered, only then can we assess what analytical techniques should be employed. From this high level perspective limitations and opportunities in low and high cost analytical techniques will be discussed.

INTRODUCTION

This paper is written in a logical format that follows the procedure that an engineer should take in performing a material (product or process) assessment. Initially one must understand the scope and nature of the defect or failure. This is followed by material inspection and finally root cause or corrective action strategies. In this paper, the focus is not only on a discussion of optical and Scanning Electron Microscopy (SEM) procedures for material inspection. There are many more techniques available to the engineer. The optical techniques discussed in this paper can be performed with little resources that could be very helpful in determining root cause (if performed correctly). With that in mind, this paper includes some possible risks with performing these techniques that should be kept in mind. SEM has been included in this paper since it is a common first resource when selecting more sophisticated analytical techniques. This paper presents a common error in SEM analysis of solder joint cross-section inspection.

ASSESSING DAMAGE

It is critical that the extent of a failure is assessed, whether the product is a million unit cell phone or a $10,000 military circuit board assembly where less than 10 are being manufactured. The difficulty in determining the extent of the failure is the same; the success of a product is typically defined by high yield and high

reliability. The engineer responsible for determining root cause for a failure must segregate the failure into categories and determine how many opportunities there are for further failures. These categories will often determine if the failure is being caused in house or by a supplier, subcontractor, or user. Questions must be asked that will determine if the failure is die level (0th), die attach level (1st), component attach to PCB (2nd), or final assembly (3rd). Areas that can fall between these levels are often material specific such as circuit board failures or post component attach process defects (cleaning, coating, test). Often the failures can fall into the following catigories;

A. Material Quality

Material quality can fall into many categories however more often we consider paste, board, component, adhesives, coatings, cleaners, etc. Each of these materials has their limitations and complications. For example, circuit board manufacturing is a complex process utilizing mechanical (drill), thermo-mechanical (press/cure) and chemical (plating/etching/stripping) processes. Each process has its own unique limitations and characteristic failures.

Q: What are the date or lot codes of the failed devices/boards/paste?

Q: What solder alloy was used for the SMT process? (Sn/Pb paste with lead-free component?)

Q: What component broker was used? Are they on our Approved Vendor Lists?

Q: How thick is the solder mask?

Q: What plating is being used on the component?

Q: What surface finish is defined on the board drawing? What thickness requirements for the surface finish are outlined on the PCB drawing?

B. Assembly Process

Assembly processes vary widely for electronic devices in our industry. Each process has operational windows that will produce high yield and reliable product. In order to assess the possibility of failure in each we must first understand the stresses that the product may face during assembly.

Q: What processes are being used for this product (print, placement, inspection, reflow, cleaning, dispense, final assembly, test, etc.)?

Q: How was profile development performed for this specific product?

Q: Were printing materials changed? New stencil?

Q: Is full I/O inspection being performed on placement machine?

Q: What torque specification is used for tooling whole locations when mounting product to chassis? What order are screws placed? How are boards supported?

Q: How are boards handled following assembly?

Q: How is the multi-up panel singulated?

Q: Is paste being under or over printed for a particular design? (1-2 mil reduction?)

C. Design

Design can affect many aspects of yield and reliability of a product. Simply following component manufacture recommendations for land patterns and stencil apertures may not be sufficient to overcome some unique product requirement. Proper design must be taken into account for managing reliability and determining root cause of failures.

Q: How close are fragile capacitors or associated passives to edge of PCB?

Q: What are the aspect ratios of the stencil?

Q: How close are critical components to tooling holes?

Q: Has the PCB manufacturer made modifications to PCB design from drawing?

Q: Is the failed part in a location of high stress? Has it been moved as compared to previous revision of the product?

Q: Is conformal coating being used on this product? What material has been selected?

D. Reliability

Functional testing, ICT, drop, vibration, ESS, HALT, HAST, are methods used to determine susceptibility of failure in manufacturing and in the field, however correlating them to true field reliability is difficult if not impossible for most reliability engineers. In order to interpret the failure modes identified by common failure analysis practices we must understand all the mechanical and thermo-mechanical stress conditions a product was subjected to, prior to the failure occurring. Often reliability issues are not associated with a single root cause. Therefore it is common in today's research to see topics in assembly pre-stress. It has been shown that thermal or mechanical pre-stress can dramatically affect the reliability of components [1,2]. Root causes for these accelerated failure conditions are not fully understood.

Q: What manufacturing and final assembly stresses is this product subjected to?

Q: What is the end use condition of this product?

Q: Is ICT fixturing designed properly (functioning as expected)?

Q: How were profiles developed and product fixtured in thermal and mechanical testing equipment?

Q: Were components removed immediately following failure or allowed to be tested far beyond their failure point in accelerated life testing?

Q: Can a particular I/O be identified as the failure location? A component? A circuit?

Q: Is the failure a short or an open?

Q: What environmental temperatures, corrosive media, or humidity was the product subjected to prior to failure?

OPTICAL ANALYTICAL TECHNIQUES

Once a failure has been identified, prior to root cause determination, the first objective should be identifying failure mode. Failure mode must be established using techniques that do not subject the product to further stresses and risk of damage. Several non-destructive and destructive techniques are considered low cost and can be very effective in assessing root cause. However if handled or interpreted incorrectly can be costly.

The simplest example of low cost analysis is optical microscopy. The IPC-A-610, E-2010 standard section 1.9 recommends limiting magnification for inspection purposes to 1.5x-40x depending on the size of the land pattern [3]. In cases of cleanliness or conformal coating inspection the maximum suggested magnification defined in IPC-A-610 is 4x [3]. Often this is done to limit the uneducated user of identifying anomalies that may not affect the overall performance of the product. Therefore it is best to have comparative samples from passing lots of product. These baseline samples often can segregate typical conditions from non-characteristic conditions. Having baselines of good products can also allow for higher magnification inspection of design and quality while reducing the risk of misinterpretation.

Optical microscopy is inherently non-destructive and can be used to identify failures in any of the categories listed in the previous section. Lighting techniques should be diversified in order to highlight defects. Low angle lighting, co-axial lighting, spot lighting and ring lighting can all be used at low magnification in order to illuminate surfaces. Lighting can have dramatic effects on illustrating contamination or fracture conditions that may normally be invisible. Often tin whiskering (Figure 1) and other surface conditions (figures 2-4) will only be visible when adjusting lighting techniques.

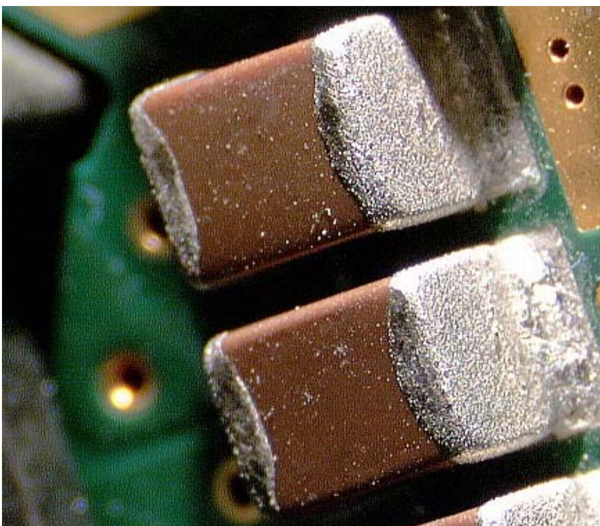


Figure 1, Low angle lighting to identify whiskering

Figure 2, Optical microscopy of dendrites

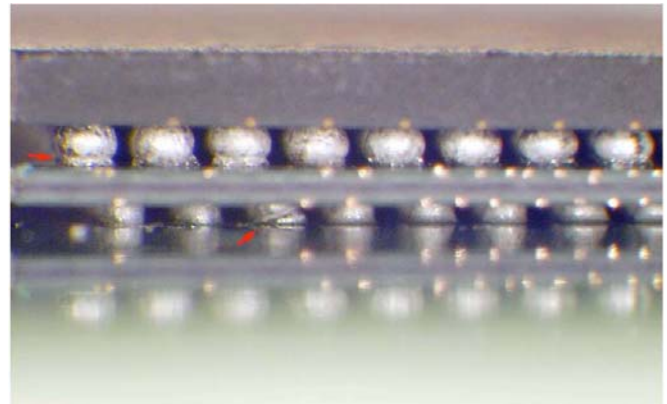


Figure 3, PoP Head in Pillow failure

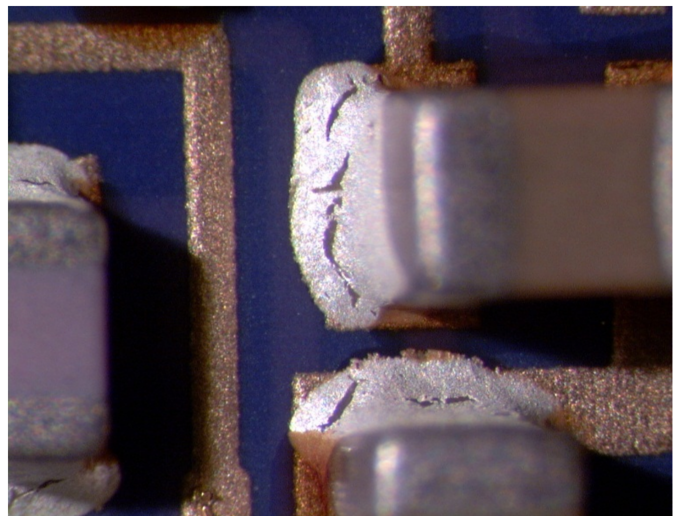


Figure 4, Cracking in conductive adhesive illuminated with low angle lighting

Optical microscopy at higher magnification can be useful for assessing lead free solder joints. There is a lack of contrast in lead-free solder joints since they are 95% or more tin (Sn). In order to differentiate between

alloys and precipitate structures in lead-free it is often useful to employ dark field or cross-polarized lighting techniques. A schematic of a polarizing microscope can be seen in figure 5 along with examples of various lighting techniques in figure 6.

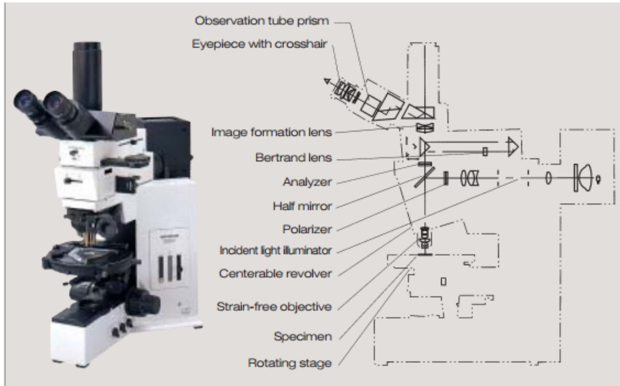


Figure 5, External view and construction of an incident light polarizing microscope [4]

It should be stated in order to get the contrast produced by images in figure 6c cross-sectioning techniques must be optimized and perfected to eliminate not only scratches but the damage caused by the grinding and polishing steps to soft Sn-based solder. The details for preparing a sample for polarized light inspection are not covered in this report.

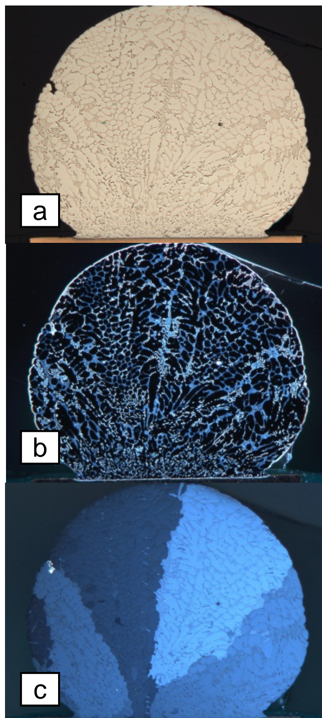


Figure 6, Identical SAC305 solder joint cross-section observed in a) bright field b) dark field and c) cross-polarization

In addition to solder joint condition laminate failures may also be difficult to view using standard lighting techniques. Failures described as pad craters, where the top layer copper is separated from the circuit board due to thermal or mechanical stresses can be difficult to identify. Often the investigator optimizes lighting for inspection of the solder joint. This leaves the laminate material dark and underexposed. In order to properly image the laminate the solder joint requires over exposure as shown in figure 7.

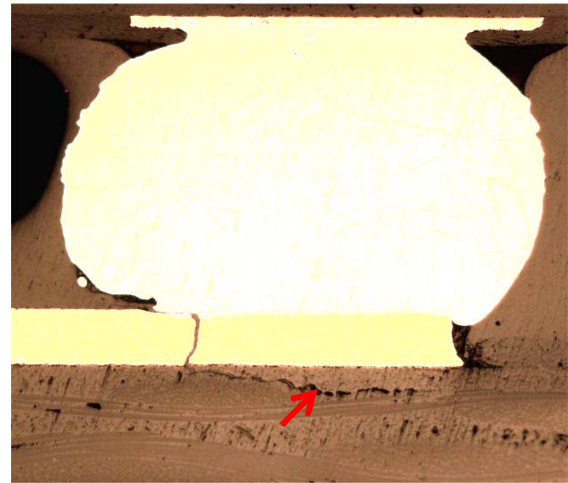


Figure 7, Pad cratering, overexposed bright field image

Poor cross-sectioning techniques can make evaluation of solder joint conditions difficult. Examples of poor sections can be seen in figure 8. Improperly polished sections, where scratches and debris from the initial grinding operations occur, should be avoided. Improper visual interpretation of these “Laboratory artifacts” can produce false positives with respect to fractures or separations, conductive particulates or foreign materials, intermetallic anomalies, and laminate or dielectric defects.

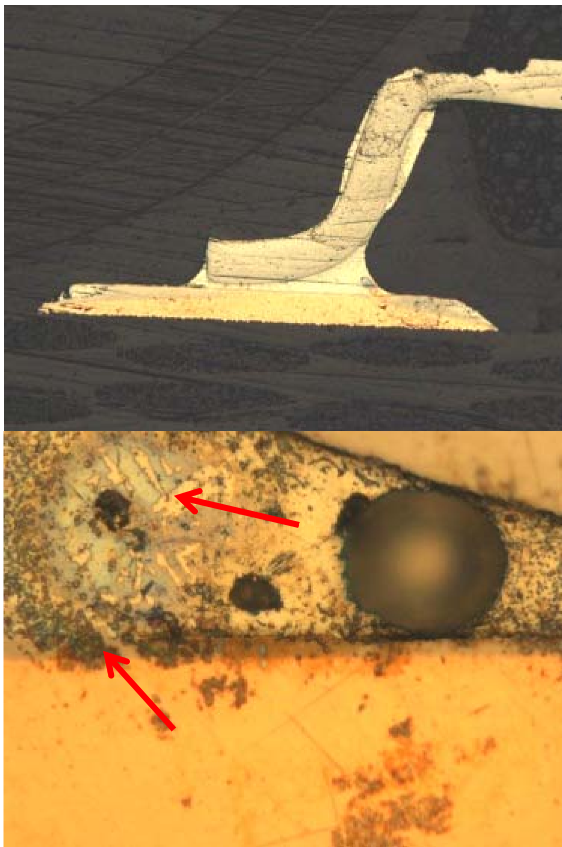


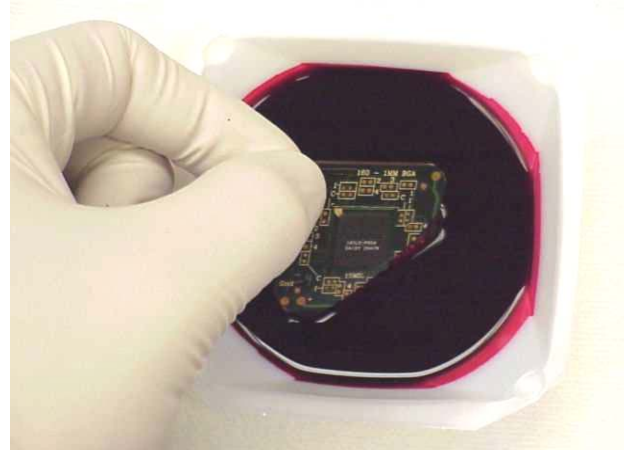
Figure 8, Poor cross-sectioning results in difficult to interepret samples. In the above image large scratches are observed. In the below image polishing residues cover the surface.

Dye penetration can also be an effective low cost analysis technique; in particular for failures were a specific target I/O has not been identified. Multiple devices can be tested and multiple failure modes can be identified. Graphic representations can be developed with locations of failures, percentages of fracturing and types of failure modes (e.g. component side pad crater, component side IMC, bulk solder, PCB pad IMC, PCB pad crater).

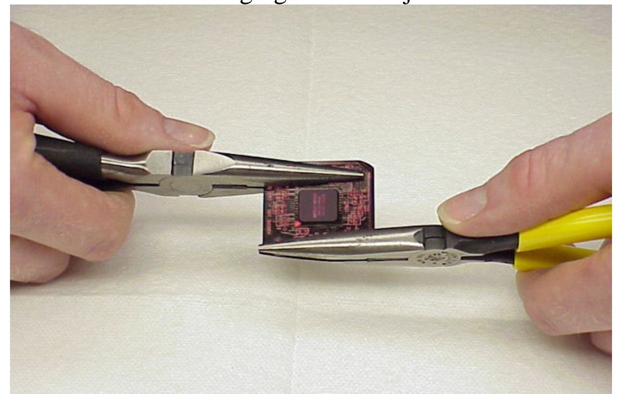
A short description of the method is listed below with the dye used for the test. At highest risk for processing error is the curing (step 6) of the dye. One must ensure that all the dye is dried prior to removal of the components. Otherwise liquid dye could migrate onto surfaces causing false interpretation. Figure 9 also shows the result of the test on pad cratering failure modes and IMC failure modes.

Dye Penetration Procedure

1. Carefully cut the region of interest from the assembly by using a low stress technique. A water cooled diamond band saw is often an effective extraction method. Ensure at least ½ inch spacing exists between the edge of the coupon and the component being tested.
2. Clean the assembly with isopropyl alcohol (IPA) or an appropriate flux remover using an ultrasonic bath, and dry. This step should also clean most cutting debris from step 1.
3. The assembly is immersed in red dye (Dykem steel layout fluid #80496) to stain all exterior and fracture surfaces.



4. While submerged in the dye bath is placed in a vacuum of 9 in Hg for 1 minute to eliminate air from under the device. Ultrasonic baths are also useful during this step. When using an ultrasonic bath the circuit board should be placed vertically in the dye. The liquid is allowed to penetrate for 1 hour.
5. Excess dye is removed. Dye removal can be optimized by placing the coupon vertically and placing a paper towel at the bottom edge of the device to wick dye from under the component.
6. The component is dried 30-60 minutes at 100-125°C.
7. The component is mechanically pried off the board using pliers to twist the board, or a thin screwdriver can be carefully placed between the component and the board to lift the component away from the board surface without damaging the solder joints.



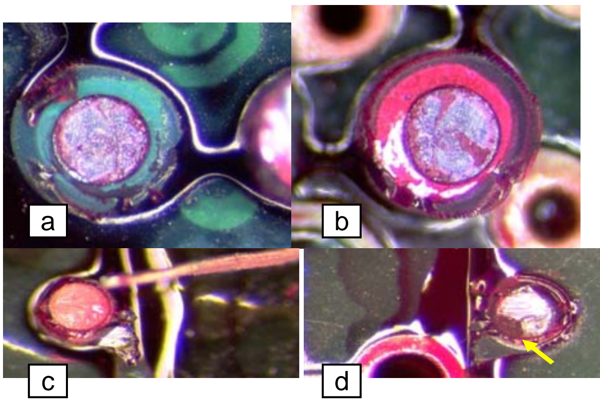


Figure 9, Dye testing results; a, b) board side IMC failure and associated ball removed with component; c, d) PCB pad crater component and ball side.

SEM INSPECTION TECHNIQUES

Most analytical techniques requiring outsourcing will range in cost from several thousand dollars to complete a root cause inspection, to several hundred dollars per hour for use of sophisticated analytical equipment. As an example current, Dual Beam FIB fees can exceed thousands of dollars to analyze a sample. Slightly lower cost techniques such as Scanning Electron Microscopy (SEM) analysis are a useful tool for identifying failure mode conditions, however the inspection can be poorly executed resulting in misinterpretation and confusion.

The most common error in SEM analysis is the use of secondary electron (SE) detectors for metallurgical cross-section inspection of intermetallic. Without getting into technical details, SE is used for imaging topography. Cross-sections are by design flat, so atomic contrast between Ni, Cu, solder and intermetallic is not optimized. Back scatter electron (BSE) detectors provide excellent atomic number contrast and therefore should almost exclusively be used for imaging metallic cross-sections of electronic devices. Examples of BSE vs. SE images for a cross-section are shown in figures 10 and 11.

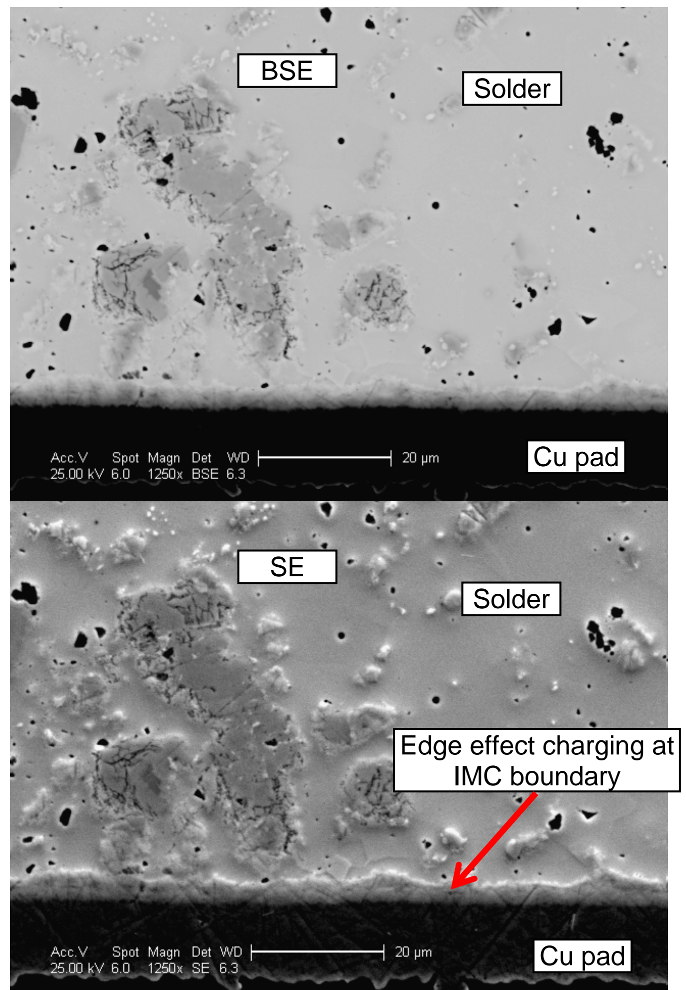


Figure 10, BSE and SE images of identical cross-section locations at 1250x

As can be seen from the images in figure 10 and 11 the ability to distinguish intermetallic regions is compromised using SE detectors, however SE can provide greater detail due to the inherent planarity variation in cross-sections due to the hardness differences in the materials. Harder materials like IMC grind and polish away more slowly than the softer Sn leaving a step between the materials. These steps are highlighted in SE due to edge effect charging.

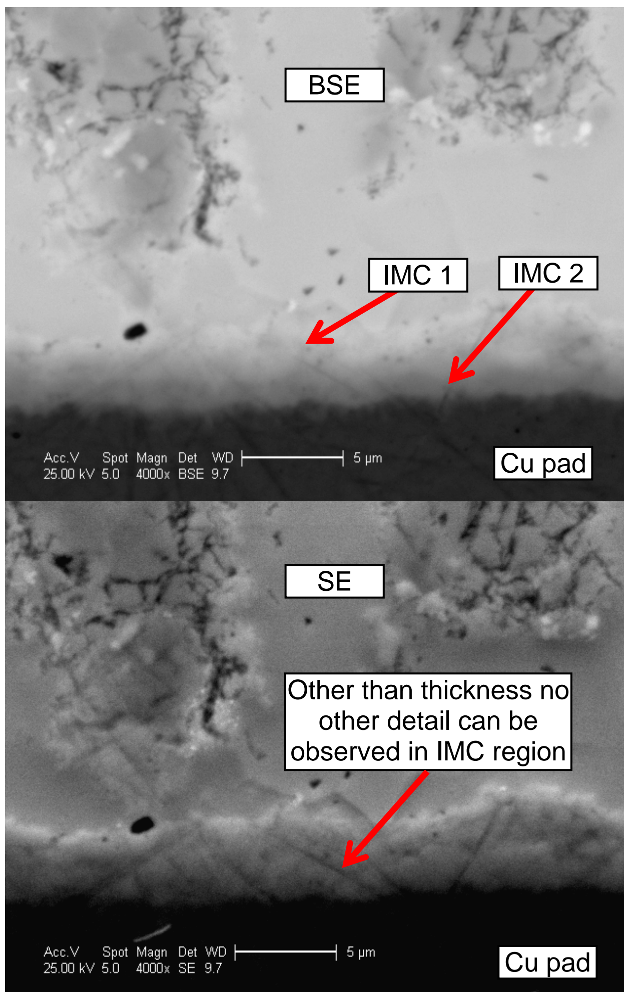


Figure 11, BSE and SE images of identical cross-section locations at 4000x

DETERMINING ROOT CAUSE

Once understandings of the product's use condition, pedigree, and failure mode have been determined the responsible engineer must try to connect the failure mode to the environmental or process condition. This can be accomplished by either comparison to known good product or continued testing. Testing requires materials that may not be on hand and sufficient time to complete test. Both are often not available. Often the most concise conclusions are reached from identification of a clear defect or a dramatic reduction in fallout in the next manufacturing cycle following a corrective action.

CONCLUSION

This paper simply discusses a small fraction of the techniques available to engineers tasked with material assessment. The intent of this discussion was to illustrate the methodology, benefits, and limitations of critical techniques that an engineer may utilize in determining the root cause of a failure. Moreover, any technique used by an engineer has its limitations and requires consideration.

Cost of failure misinterpretation and delay is astronomical and is the cause of significant waste in time and money in an electronics manufacturing factory. With some simple analytical techniques, isolation of the failure and determination of the root cause may be possible. In order to accomplish "root cause" the data collected from analytical techniques discussed in this paper (and others) must be combined with knowledge and experience. Only then can production and field failures be effectively limited and controlled.

ACKNOWLEDGEMENTS

The authors of this paper would like to acknowledge Shantanu Joshi, a graduate student from Binghamton University's System Science and Industrial Engineering department for providing the cross-section samples.

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