As originally published in the IPC Printed Circuit Expo, APEX & Designer Summit Proceedings.

Thermal Cycle Testing of PWBs – Methodology

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Reliability testing of printed wire boards (PWBs) by thermal cycling offers the ability to compare relative survivability through assembly and reliability in the end use environment. This article delineates an eleven step method to establish a test protocol that will maximize accuracy, applicability and reduced costs and reduce the propensity for confounded data in thermal cycle testing of bare PWBs exposed to lead-free assembly and rework simulation. The method presented in this paper is targeted to the unique challenges afforded by lead-free testing applications and testing of the integrity of conductive interconnections and dielectric materials.

Thermal cycle testing of PWBs has traditionally been focused on the failure of the conductive circuits and interconnections. Testing is typically achieved by thermal cycling a representative coupon with the same constructions and design attributes as the associated PWB. The coupon replicates the PWB layer count and interconnects structures like plated through holes (PTHs), buried vias, blind vias, or microvias. The representative coupon is frequently on the production panel and directly reflects the fabrication attributes and variables of the PWBs from the same panel.

There are two general methods of heating the test coupon, heating the coupons environment (air, liquid, sand) and transferring heat by conduction/convection or heating the coupon directly with heating circuits that are internal to the coupon. By either method the test coupons are subjected to temperatures cycling with the lower end temperature at approximately –60°**C** and the upper limit typically not exceeding 260°**C**. Traditionally a 10% increase in resistance of a circuit was considered a failure.

Reliability testing starts with selecting the test method. The importance of this step is that each test method has certain advantages and limitations. Thermal cycling ovens are capable of achieving temperature ranges between -60 and ~140°C. Ovens are limited in speed and high end temperature. Thermal ovens require a hold time at an isotherm to assure all samples achieve the test temperature. The hold time ages the dielectric material changing physical properties like the glass transition temperature (Tg), coefficient of thermal expansion (CTE) and viscoelastic properties such as the storage modulus (Young's' modulus). One test method, highly accelerated thermal shock (HATS ™) reduces the cycle time to as low as five minutes. Internal heat methods (SITS, IST) have the advantage of precise temperature control to higher test temperatures (300°C) and fast cycle times (5 minutes or less). There is no hold time at temperature in internal heating methods and dielectric material is less likely to have thermal induced aging by this method. The disadvantage of the internal heating method is that the lower thermal limit is ambient (~22°C). Although solder joints are significantly affected by low temperature thermal excursions, PWBs are less vulnerable to negative temperature testing. It appears that testing to temperature near Tg improves the ability to discern discrepant and unreliable conditions.

There are three reliability test approaches; compliance testing, reliability testing, and survivability testing. In compliance testing representative coupons are tested to the minimum cycle requirement, and once achieved, testing stops. In reliability, design of experiment and product life tests, testing continues until a 50% failure rate is achieved. In survivability testing the test temperature is increase to assembly temperatures (ex. 220°C) and testing is terminated at 50 thermal excursions.

IST and HATS ™ have the advantage of being able to sense failures as a 10% increase in resistance while other methods are frequently limited to monitoring for damage by an event detector. An event detector requires of resistance change that are orders of magnitude larger than the methods used in HATS ™ and IST. Once a test method has been selected test samples may be produced. HATS™ and IST methods require customized coupons with certain electrical and physical attributes for their respective test method.

In any test method the selection of which attributes will be tested has a profound effect on the acuity of the test. In an ideal world one would test all attributes; from a practical point of view testing is usually limited to a few critical attributes. Hole size is one critical attribute and testing usually includes the smallest hole. Smaller holes effectively test the reliability of the barrel of the PTH. As hole sizes diminish it becomes a challenge to effectively get chemistries into the hole for cleaning and electroplating. Holes 0.010" or less, are difficult to produce and are particularly sensitive to overall copper thickness and copper distribution within the PTH. Holes larger than 0.018" are less of a fabrication challenge. Large holes tend to be robust and resistant to the stress induced by thermal expansion. Stress appears to be redirected into the internal interconnection making large hole designs more sensitive to testing the robustness of internal interconnections. Material studies often include grid size (hole to hole spacing) variations. Grid size influences material damage typically expressed as delamination, cohesive failure or crazing of the dielectric. In DOE applications, orthogonal attributes; ones that are considered contrasting and unique, are selected. It is prudent with the advent of lead-free testing to include a material evaluation as an integral part of the thermal test. Traditional thermal test vehicles use microsectioning to confirm or refute material damage. IST coupons frequently have a material test circuits included.

Surface finish may have a profound effect on reliability testing. For compliance or acceptance testing the surface finish of the product should be reflected in the test vehicle. For testing and ranking variables like materials or different designs, surface finish may dominate the test results limiting acuity or even confounding test results. There are two surface finishes that have been demonstrated to influence reliability results; reflowed solder and finishes that incorporate nickel. Either reflowed solder or nickel can mask reliability data in specific instances.

Hot air solder leveling (HASL) is, by its' nature, an extra thermal excursion that is in effect equivalent to an extra assembly cycle. It appears that some materials are robust with up to three thermal excursions but are degraded after the fourth excursion. In a lead-free application the extra thermal excursion associated with a HASL process may have a significant impact. Any fusing or reflow process should be considered when establishing comparative reliability tests.

In high temperature testing and preconditioning where thermal excursions exceed the liquidous temperature of a solder finish, copper cracks made be bridged with solder. The effect is that cycles to failure are artificially extended due to solder filling the developing cracks. Instead of presenting a catastrophic failure the circuit appears self healing. If a coupon is subjected to high temperature thermal excursions like assembly and rework simulation and becomes damaged in the process the solder may reflow and fill the cracks in the PTH. If the coupon is then subjected to thermal excursions below liquidous, cracks frequently develop in the solder filling the original copper crack (figure 1).

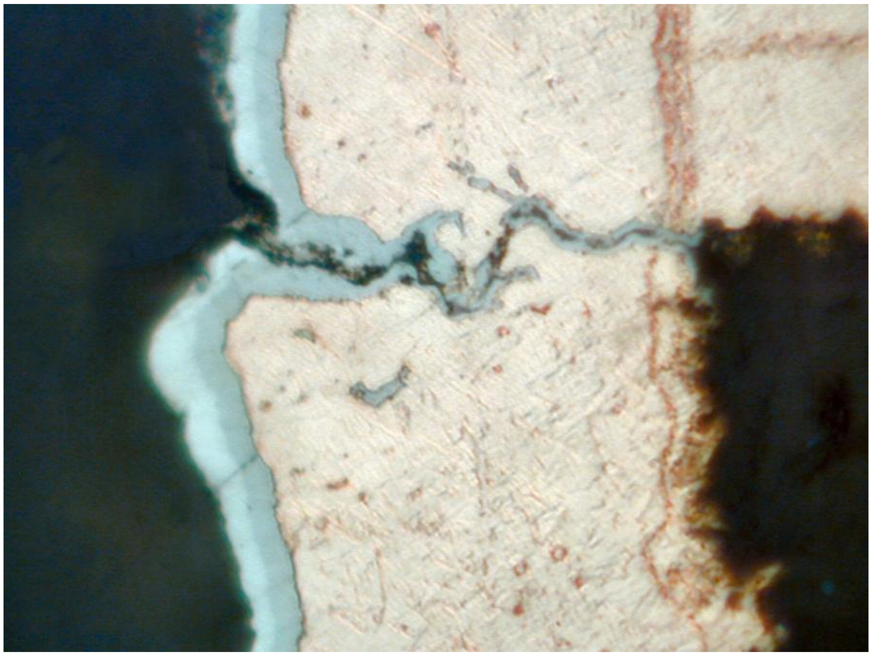


Figure 1 - Copper Crack with Reflowed Solder Cracked

Nickel is robust in most applications extending cycles to failure. Cracks in the PTH start at a glass fiber and stop when the nickel layer is reached (figure 2). It should be mentioned, however, that occasionally nickel with nicks, bubbles, variable thickness, or nickel cracks may reduce thermal cycles to failure. Electroless nickel is known for even plating thickness throughout the PTH, while certain electrolytic nickel baths appears to be prone to variations in nickel thickness. With aspect ratios of 8:1 or greater, achieving a uniform and even nickel distribution throughout the barrel of the PTH can be a challenge. It appears that compromised nickel may initiate a crack which propagates toward the dielectric (figure 3). Weak nickel can reduce thermal cycles to failure. On well applied nickel the cycles to failure is significantly extended.

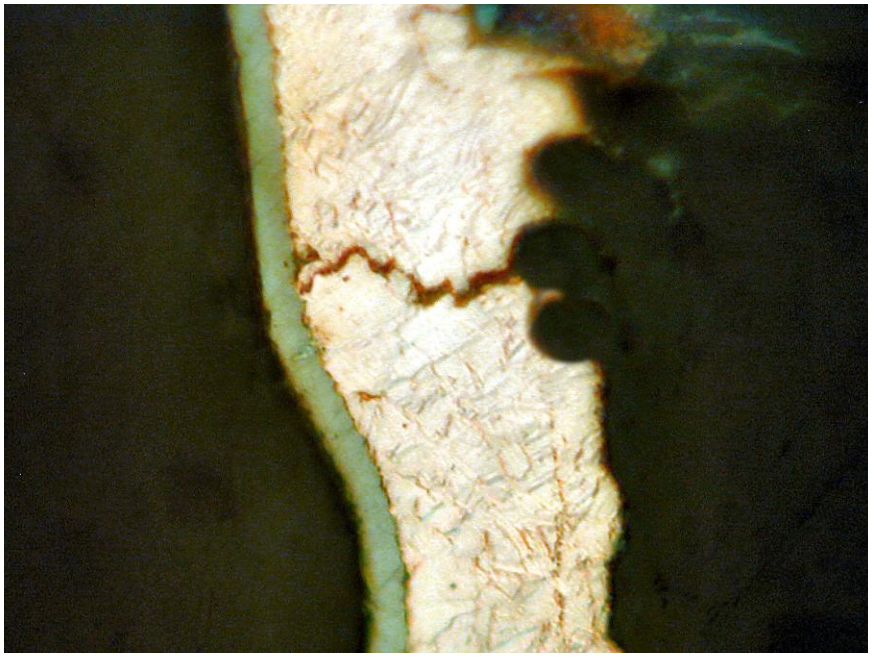


Figure 2 - Nickel Protection – Cracks Stops at Nickel Finish

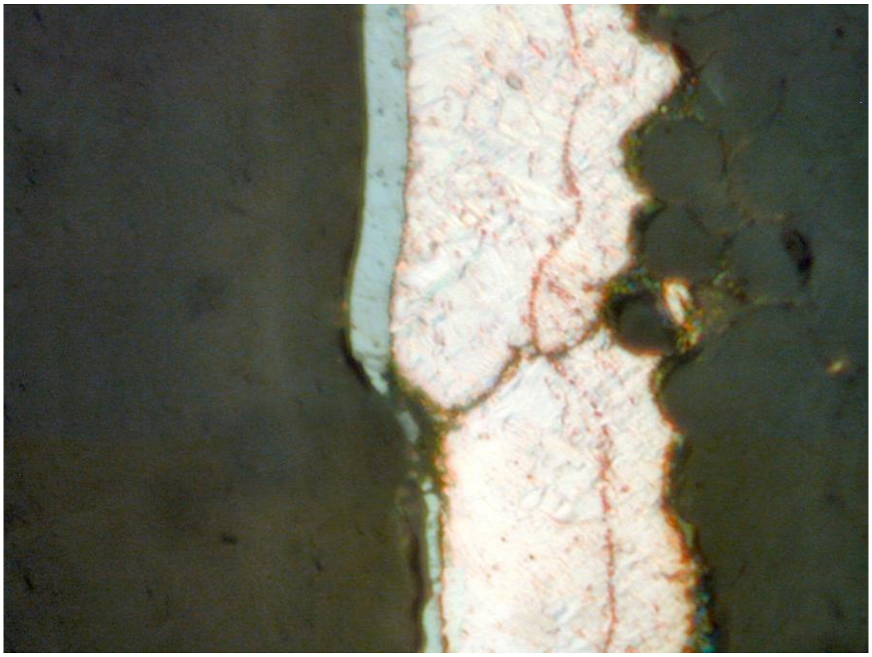


Figure 3 - Nickel Acceleration – Cracks Induced by Nickel Defect

If the goal of the investigation was to determine which of three materials is most robust then the presence of nickel would extend testing time and possibly confound the data. The subtle effects of roughly equivalent materials may well be masked by the presence of nickel in the surface finish.

Another influence that should be addressed prior to the selection of a test vehicle is design. Design may influence thermal testing in a number of ways. Grid size plays an important role in materials testing in that materials tend to delaminate most readily at 0.8 mm (0.032”) spacing but are more prone to crazing with PTH drilled at a 0.5 mm to 0.6 mm (0.020” to 0.024”) pitch.

Smaller holes, 0.4 mm (0.016”) or less tend to accumulate damage in the barrel of the PTH. Larger holes sizes tend to fail at internal interconnections. So testing the robustness of electrolytic plating would best be served with holes less than 0.4 mm

(0.016”). Testing the reliability of interconnections, for example testing the robustness of different electroless coppers, would best be served with a 0.4m (0.016”) or greater hole on a large grid.

All variables including design, construction, holes size, etc. should be considered when establishing effective reliability testing. For example, electroless copper and direct metalization chemistries may be effectively tested and ranked with a test vehicle that has large holes 0.4 mm (0.016”) on a 2.5 mm (0.100”) grid, with a nickel finish to strengthen the PTH and prevent the influence of barrel crack failures.

Once representative coupons have been fabricated they should be subjected to inspection including measuring the resistance of all test circuits. For the purpose of this report this incoming inspection and measurement will be referred to as prescreening. Commonly circuits are checked for opens and shorts, and resistances are measured and recorded. The data is then subjected to a statistical evaluation. If the test method selected has the capability, capacitance measurements are made as a baseline against which material damage can be determined.

In well designed circuits variations in resistance may reflect an inverse relation to copper thickness. Circuits designed to test plated through holes should be sensitive to variations in copper thickness and distribution, Circuits designed to test interconnect robustness are more likely to be sensitive to hole preparation, registration and variations in etching. By calculating the mean, standard deviation at the one sigma limit, minimum and maximum values, range and coefficient of variation (defined below) one is able to rank coupons and sort coupons into appropriate test groups.

If it is determined that the resistance of a circuit is sensitive to copper thickness in the barrel of the hole, low resistance would indicate thick copper plating. Conversely higher resistance is a reflection of thin copper plating in the barrel of the PTH. If the mean resistance is a reflection of copper thickness, variation from the mean is a reflection of variations in copper thickness. A large standard deviation in resistance reflects variable plating. Experience has demonstrated a coefficient of variation (described below) of greater than 10% may reflect unacceptable copper thickness variation and requires a review to understand if the variation is due to an attribute that is critical to the test goal. If, for example, materials are being compared, it would be counterproductive to establish a ranking of materials where one group of coupons is under plated. Such a test, confounded by variations in copper, would produce ranking based on copper thickness that could unknowingly be attributed to the influences of the tested materials.

Armed with the range in resistances one can intelligently select samples that better support the testing goal. If compliance, acceptance or survivability testing is being performed high, midrange and low resistance coupons best represent a reliability sample group that includes the extremes and midrange of copper plating thicknesses. Evaluations to rank or rate variables, such as different material types, are best served by selecting the most common resistance range across the test groups. Using the most common rang between groups will minimize the effects of copper thickness variations in the sample set allowing the effect of the variable of interest to be better expressed in the test data.

If capacitance circuits are available in the test vehicle then the capacitances between layers can be measured and two different coupons compared. Variations in construction are easily observed and variant coupons may be removed from the test group. Figure four demonstrates how the subtle differences in layup of two six layer coupons are demonstrated as changes in capacitance. Measuring the picofarads reading between the planes on each layer allows one to confirm or refute that two coupons have the same construction. Variation in the number of ply and glass styles each produce different construction profiles, based on capacitance measurements. If two dielectrics were being ranked for robustness, and variations in construction were found, then there would be concern that the test vehicles may not be equivalent and test data may be skewed.

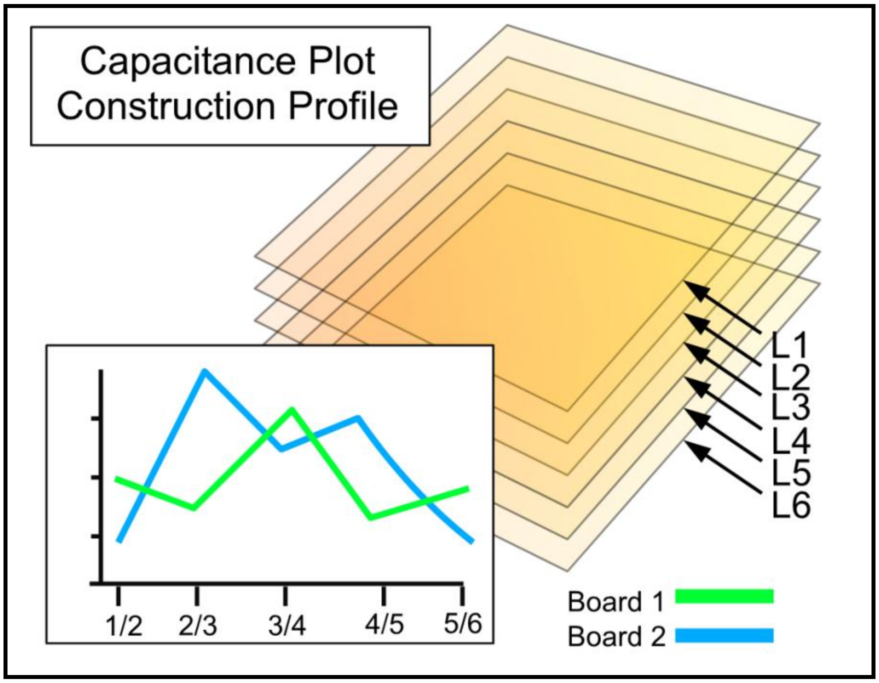


Figure 4 - Construction Profile

In prescreening, the resistance and capacitance measurements allow an intelligent selection of coupons which in turn increases the acuity and accuracy of the reliability test. The initial resistances and capacitance measurements set the baseline against which subsequent measurements are compared. Significant changes in resistance and capacitance are considered to be a reflection of copper or material damage.

The simulation of the thermal excursions associated with assembly and rework will, for the purposes of this article, be referred to as preconditioning. Preconditioning coupons allows a better evaluation of the degradation in reliability that is to be expected in assembly and rework. As a standard three thermal excursions are considered representative of two passes through a reflow oven and one pass over a solder wave. Two sided surface mount PCBs with a PTH connector would likely have three thermal excursions during assembly. Rework is thought to be represented with an additional three thermal excursions; possibly a BGA removal and replacement and one solder touch-up.

Preconditioning to simulate assembly is typically three thermal excursions, while assembly and rework is six thermal excursions. The reliability of the product can adequately be established by comparing cycles to failure of coupons tested “as received”, against the cycles to failure of coupons preconditioned three times (3X) and six times (6X). The “as received” coupons are the control group and the 3X and 6X preconditioned coupons the comparative test groups. One expects the “as received” coupons to survive the longest, followed by 3X coupons and the 6X preconditioned coupons. If the “as received coupons produce lower cycles to failure than the 3X or 6X coupons then one suspects that material damage is artificially extending the cycles to failure data, confounding the results.

Acceptance and compliance testing often uses 5X preconditioning as a standard by convention. DOE and comparative tests usually have testing “as received”, 3X and 6X. Survivability testing is basically preconditioning to failure and therefore no preconditioning is required before survivability testing.

Typically preconditioning is performed at 230°C for tin lead applications. Preconditioning to simulate lead-free applications is usually preformed at 245°C for low temperature lead-free assembly or 260°C for high temperature lead-free assembly. Preconditioning may be performed in a reflow oven, on the test equipment (for example IST) or by other means as agreed to by the user and supplier (AABUS). There is a great variability in reflow oven capabilities, assembly methods, and reflow profiles. Variations in assembly are observed between companies or even within companies.

Coupons have inherently different physical parameters than printed circuit boards that are loaded with paste and components, and setting ovens to produce the equivalent condition on coupons is problematic. The difference in mass between PCBs and coupons present the major challenge as the coupons do not have components or solder pastes and are a much smaller size. Sending a raft of coupons down the reflow oven setup to run boards may over stress coupons producing failures that are not observed in the boards.

Running coupons through oven setup to simulate the thermal profile of the PWBs requires significant time commitment due to cool down requirements between each run. For the best results preconditioning must be well controlled and repeatable.

It is important to measure the resistances and capacitance if available, before and after preconditioning to determine if there is interconnect or material damage attributed to the assembly and rework simulation. One way to capture this damage is to start reliability testing to establish the resistance baseline, remove the coupons, perform preconditioning, measure capacitance changes, and then resume the test. This allows the damage associated with assembly to be captured in the reliability test data. Both interconnection and material damage may be incurred in preconditioning with the temperatures associated with lead/free assembly. If the material is significantly damaged the reliability testing may be suspended due to the probability of having stress-relieved the coupons and likelihood of having the cycle to failure data confounded. It is a common error in reliability testing, not to capture the damage associated with preconditioning by starting reliability testing only after the assembly and rework simulation.

Various testing protocols require a different number of cycles to failure. Compliance and acceptance testing typically stops when the minimum cycles to failure are completed. DOE and reliability are typically set to 500, 1000 cycles or continue until a 50% failure rate is achieved. With HATS™ and IST testing a 10% increase in resistance is considered a failure while thermal cycling ovens typically have an event detector that continues cycling the coupon until the circuit being tested has an open. By stopping testing exactly at 10% one reviews the failure, (by means of microscopic examination) as it is developing, rather than after the failure site is destroyed by extra thermal cycles.

Testing temperatures vary based on equipment. Thermal cycling ovens allow negative temperature testing to -60°C or lower but are limited at the high end to approximately 140°C. HATS™ testing range is typically -60°C to 150°C. IST testing is limited to ambient 22°C to a practicle limit of 300°C.

Strain is defined as the change in length divided by the initial length (in this case at ambient). The strain associated with z-axis expansion due to thermal excursion is the force that induces stress in the PWB causing damage of the interconnection and material. The strain associated with negative temperatures, for example, between -60°C and ambient, ~22°C, is the same strain associated between 22°C and 104°C; the former in compression while the later is in tension. It appears the majority of damage in PWBs is associated with the higher temperature excursions near or above Tg. PWBs appears to tolerate the negative temperature without significant influence in reliability. It should be noted that solder joints, however, may be susceptible to thermal excursions to negative temperatures. The high end temperatures achieved in reliability testing have been increasing over the last few years, particular in response to lead-free assembly. A number of companies have performed studies and established standards based on tests at or above 150°C.

Thermal cycling ovens are generally limited to upper temperatures of about 120°C to 140°C. If the test method selected is capable, DOE, reliability and compliance testing is preformed at ~150°C. Many companies are specifying microvia testing at 190°C and polyimide materials (flex and rigid) testing at 210°C. Survivability testing is preformed at 220°C to 260°C. Acceleration testing is typically preformed at 150°C, 160°C and 170°C. If higher temperature testing is not available then test cycles must be extended to prevent false positive results and to capture enough failures to insure the data is statistically meaningful.

At the end of testing the cycles to failure are recorded. Standard statistical analysis is applied including mean, standard deviation, minimum, maximum, range and coefficient of variation. The mean allows proof of compliance for compliance testing. In DOE and reliability testing the mean establishes ranking of variables while the coefficient of variation suggests if there is more than one influence expressed in the results. A coefficient of variation (see below) in cycles to failure data of greater than 65% should be investigated.

An in depth review of statistical methods is beyond the scope of this article but there are a few point of interest offered for consideration. Typically common statistical methods are applied to resistance and cycle to failure data. This includes mean, standard deviation and range but a useful calculation to include is coefficient of variation. This is the standard deviation divided by the mean (formula 1). For ease of use this number is often expressed as a percentage. A coefficient of variation below 1% or greater than 100% is considered meaningless.

$$c_v = \frac{\sigma}{\mu}$$

Formula 1 - Where: c_v = coefficient of variation, σ= standard deviation, μ = mean

The mean cycles to failure are the most used calculation for ranking and comparing results. The coefficient of variation (C_v) is useful as an indicator of process variation and possibility of multiple failure modes. The coefficient of variations of resistance measurements in the as received condition can be relevant to copper plating and distribution variation in circuits that are sensitive to copper thickness.

Common statistical analysis methods have the advantage of being universally understood, and they are easily calculated. Limits include they assume the distribution of the data is Gaussian or normal (figure 6) express as a bell curve and the method does not take end of test into account. The end of test result is, by convention, calculated as a failure.

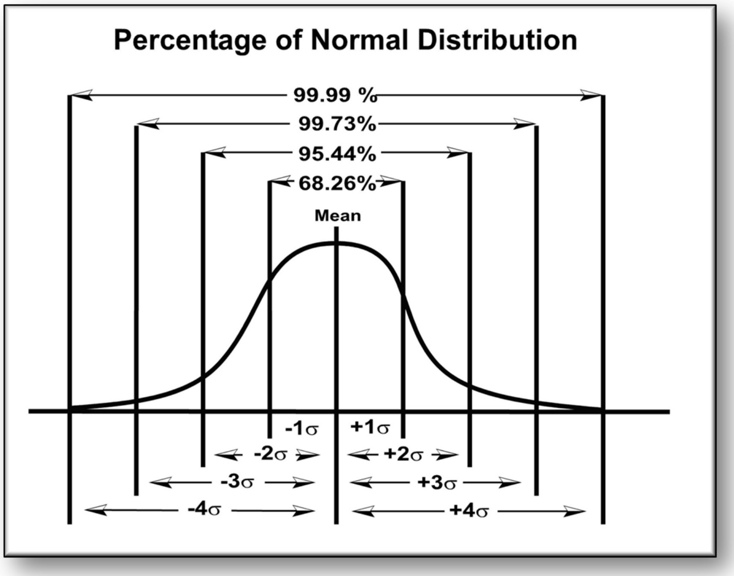


Figure 6 - Standard Distribution – Bell Curve

Weibull statistical analysis of cycles to failure produces a Weibull mean, beta (shape of distribution) and eta (mean time to failure). Although a thorough review of Weibull analysis is beyond the scope of this paper it should be noted that Weibull accepts right censored data. Beta is a useful number in failure analysis. A beta of less than 2 suggests that there may be more than one influence expressed in the cycle to failure data. A beta of greater than 15 suggests that the test temperature may be too high reducing the acuity of the results. Failures near 500 cycles usually produce good acuity and at the same time are practical from a time/cost point of view.

The two main advantages of Weibull analysis is that the shape of the curve accommodates the distribution better than standard deviation and it accepts right censored data. Instead of assuming the end of test results are a failure as is the convention with the mean, the end of test data is entered with the label suspended. Weibull analysis, to a limited degree, accommodates and adjusts data when the testing is stopped before failure. In essence, extra value is given to suspended data and the Weibull mean may be higher than the standard statistical mean.

In reliability testing the distribution is rarely bell shaped and therefore the data may be skewed. Weibull analysis incorporates the shape number beta (β). A beta of 1 is exponential, 2 emulate a Rayleigh distribution, 3.6 is normal and 5 is peaked normal (figure 7). When β is below 2.5 one should suspect that two or more failure modes with significantly different influence on reliability are present. If β is greater than 15, one may suspect that the test temperature may be too aggressive and a lower temperature may allow wider distribution, giving the test greater acuity to discern subtle variations.

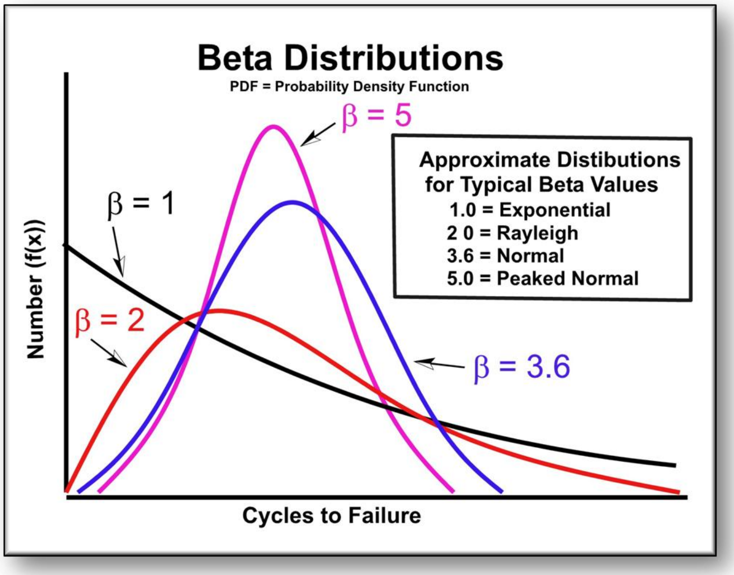


Figure 7 - Weibull Probability Density Function Curves

After testing is complete and if resistances at peak temperature have been recorded by the test method used, resistance graphs may be plotted. Resistance graphs (figure 8) are a plot of the change in resistance per thermal cycle. Resistance may be considered analogous to damage, typically due to cracks in the copper of interconnections. Resistance graphs give insight to the onset of damage and rate of damage accumulation. Resistance changes plotted against thermal cycles will show the onset and then acceleration of failure. Robust coupons fail slowly over time; usually thousands of cycles. Coupons that are weak will fail catastrophically in a few cycles. Coupons with material damage may present an accelerating damage accumulation, and then a flat or nearly flat plot reflecting the onset of the stress relieving effect of material damage. If the test is measuring resistance of more that one circuit at the same time in the coupon, then the effects of the two circuits may be compared to each other. Frequently one circuit will dominate damage accumulation, while other circuits are stress relieved or not influenced. Resistance graphs reflect the damage accumulation of the expressed and latent failure modes.

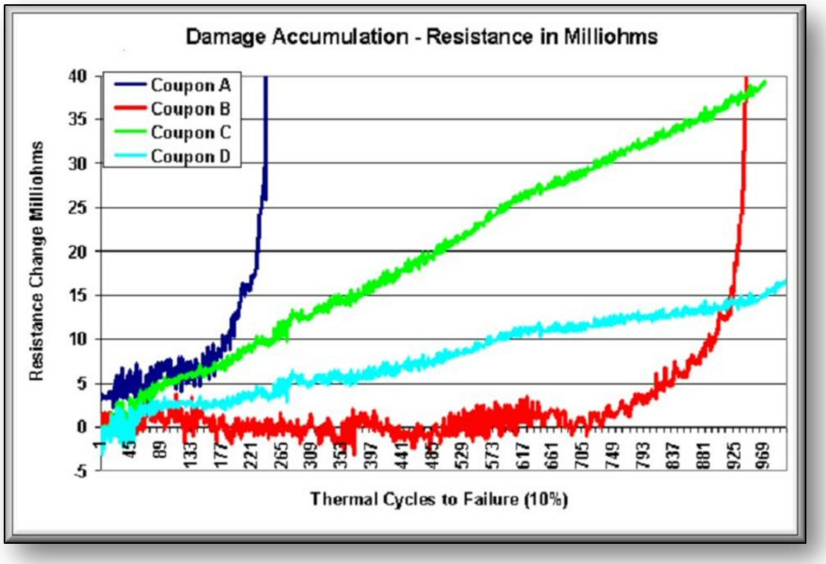


Figure 8 - Resistance Graph – Damage Accumulation

One of the most powerful tools in understanding the influences on reliability is failure site location in a failing circuit, by means of a low current and a thermal imaging camera. If testing is stopped promptly at a 10% increase in resistance, the failing circuit will still be conductive and a small current may be applied to the offended circuit while the coupon is being viewed with a thermal imaging camera. The most damaged interconnection will have the highest resistance and heat up to a higher temperature than other, less damaged, interconnections, and is readily observed with thermal imaging (figure 9). This technique is usually applied to the first failed coupon in a group, the one that achieved the fewest cycles to failure. The single most damage interconnection out of hundreds may be located in this manor and a microsection processed of that specific interconnection. This allows a direct view of a failure that is developing, before it becomes catastrophically damaged to the point where meaningful failure analysis is impossible. With a microsection of the failed interconnection, one can view the dominate failure mode in the identified interconnect and latent failure modes in adjacent interconnections. Frequently the failure site is associated to conditions that violate the minimum standards, such at copper thickness, as defined in IPC-6012 and other applicable IPC documents.

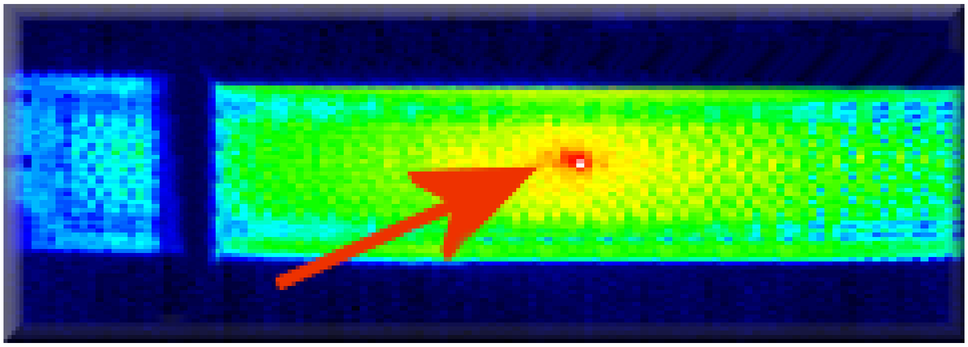


Figure 9 - Failure Location with Thermal Imaging Camera – Failing Microvia

Armed with the exact location of the most damaged interconnection, microsections may be processed and failure modes reviewed. The three most common tin/lead failure modes are barrel cracks due to metal fatigue, interconnect separation and corner cracks that progress through the electrolytic copper at the knee of the hole, at 45° angle. For the purposes of this article we will step outside of conventional definitions in that metal fatigue barrel cracks are differentiated from barrel cracks, interconnect separation is differentiated from post separation and 45° corner cracks are differentiated from horizontal corner cracks. The rationale for these distinctions is in ranking failure modes by the severity of damage, and the difference in how the failure modes are expressed in resistance graphs, and cycles to failure data.

It should be noted that all six interconnection failure modes (metal fatigue/barrel cracks interconnect separation/post separation, and 45° corner cracks/horizontal corner cracks) presented in this paper may be present in coupons that have been exposed to either tin/lead preconditioning (230°C) or lead/free preconditioning (245°C, 260°C) and are not exclusive to given preconditioning temperature. There is a trend however that has been noted. Tin/lead preconditioned coupons frequently express failure modes that are less severe and less numerous than coupons that were preconditioned to lead/free temperatures. The failure modes reviewed here are a reflection of PTH failures. Other types of interconnections including buried vias, capped buried vias, blind vias, microvias and interconnections with three point contact express other failure modes that are not reviewed in this paper.

Barrel Cracks due to Metal Fatigue: Metal fatigue barrel cracks (figure 10) are a wear out mechanism. The crack usually develops over time and traverses the copper of the barrel of the PTH at a 20° to 50° angle from horizontal. A metal fatigue crack will typically propagate between copper crystals. These cracks are frequently closed at ambient. This type of failure mode is consistent with slowly accumulating resistance that does not accelerate during the life of the test. Robust coupons which survive thousands of thermal cycles will present this failure mode.

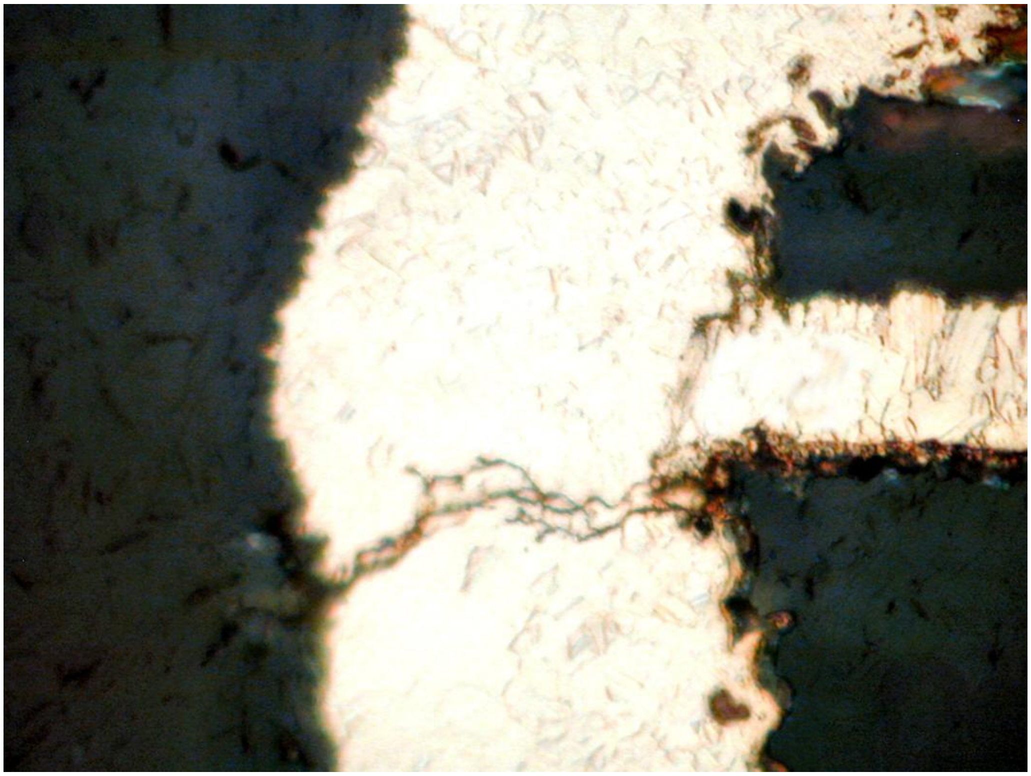


Figure 10 - Metal Fatigue Barrel Crack

Interconnect Separation**:** Interconnect separation (figure 11) is defined as a small crack at the internal interconnection. This failure mode is exemplified with small cracks between the copper of the PTH and the internal foil. The connection is frequently not displaced out of plane of the original interconnection site. There is a small gap between the foil and copper of the PTH barrel at ambient. This type of failure produces a constant increase in resistance over the life of the test.

Figure 11 - Interconnect Separation

Corner Crack - 45°: Corner cracks (figure 12) are a result of pad rotation due to Z-axis expansion. The expansion of the dielectric material puts strain on the corner of the PTH producing a fracture line the proceeds up the face of the surface foil and then across the plated copper at a 45° angle. Relatively small cracks can cause a 10% increase in resistance. Corner crack failures can be "wear-out" type failures where the copper at the corner is fatigued over time due to pad rotation as a result of repeated z-axis expansion associated with thermal cycling.

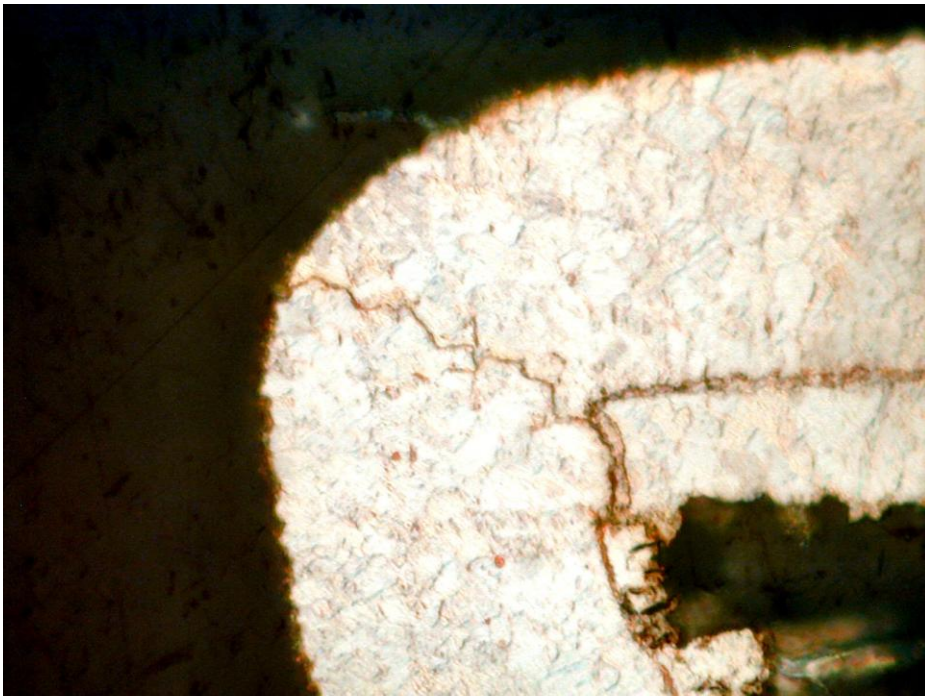


Figure 12 - Corner Crack at a 45° angle.

Generally the damage associated with coupons that have been subjected to lead-free assembly and rework is a more severe form of the traditional tin-lead failure modes described above.

Barrel Cracks**:** Barrel cracks (figure 13) are expressed as a more severe type of PTH failure. In this failure mode the crack traverses the PTH at right angles frequently propagating through copper crystals. Because the crack is open at ambient plastic deformation of the dielectric is inferred. This suggests that there is material damage associated with a barrel crack type failure. This type of barrel crack usually transverses the copper at a 90-degree angle. This failure mode frequently presents a quickly accumulating resistance, after onset that accelerates to failure over a few thermal cycles.

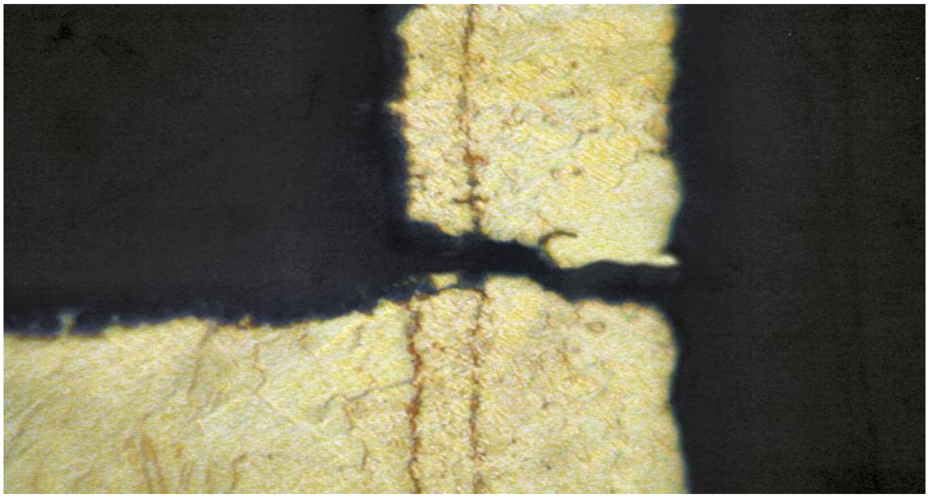


Figure 13 - Barrel Crack - Open at Ambient

Post Separation**:** Post separation (figure 14) is a failure of the connection between the internal foil and the barrel of the plated through hole. This failure mode is exemplified by large separations between the copper in the PTH and the internal foil. The connection is frequently displaced out of plane from the original interconnection site. There is a large gap between the barrel and the foil and frequently the foil end is rounded. This type of failure is catastrophic with resistance graphs showing acceleration after onset

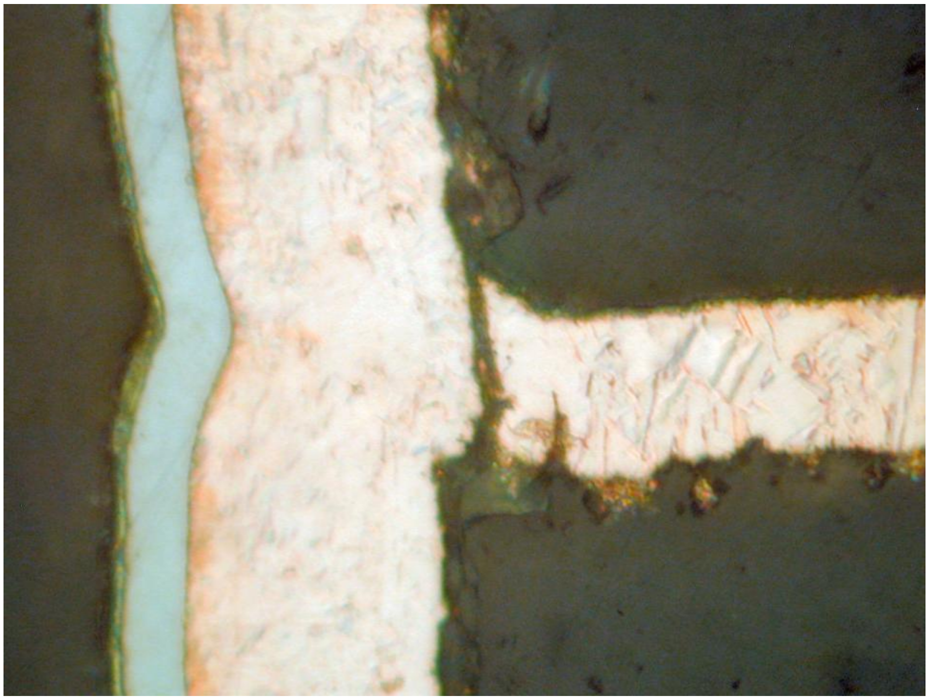


Figure 14 - Post Separation

Knee Crack- Horizontal: It appears that there is a tendency, after exposure to lead/free preconditioning, for corner crack type failures to be expressed as a horizontal crack (figure 15) occurring just below the knee of the hole. This failure usually presents with accelerating damage, after onset, failing in a few thermal cycles.

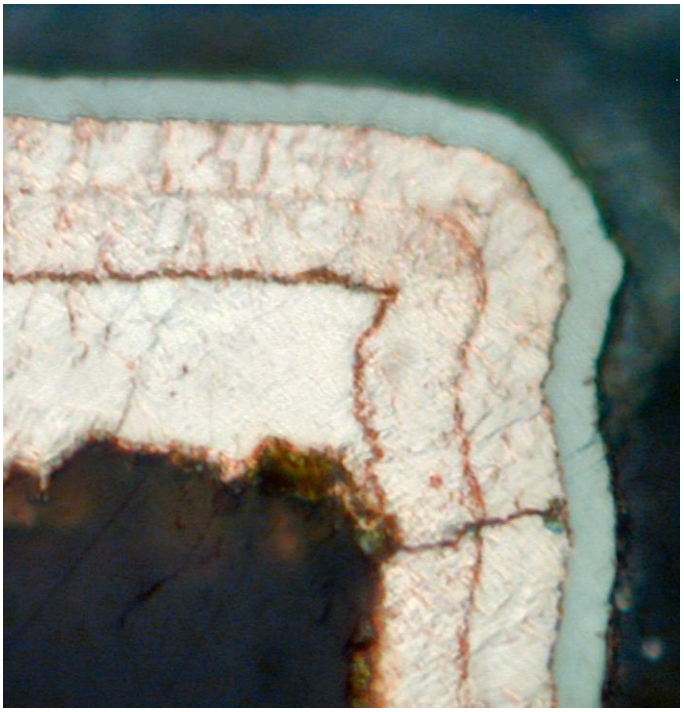


Figure 15 - Corner Crack - Horizontal

There are two trends that have been observed associated with lead-free assembly and rework. There is greater propensity for corner crack and these cracks are more frequently horizontal (figure 16).

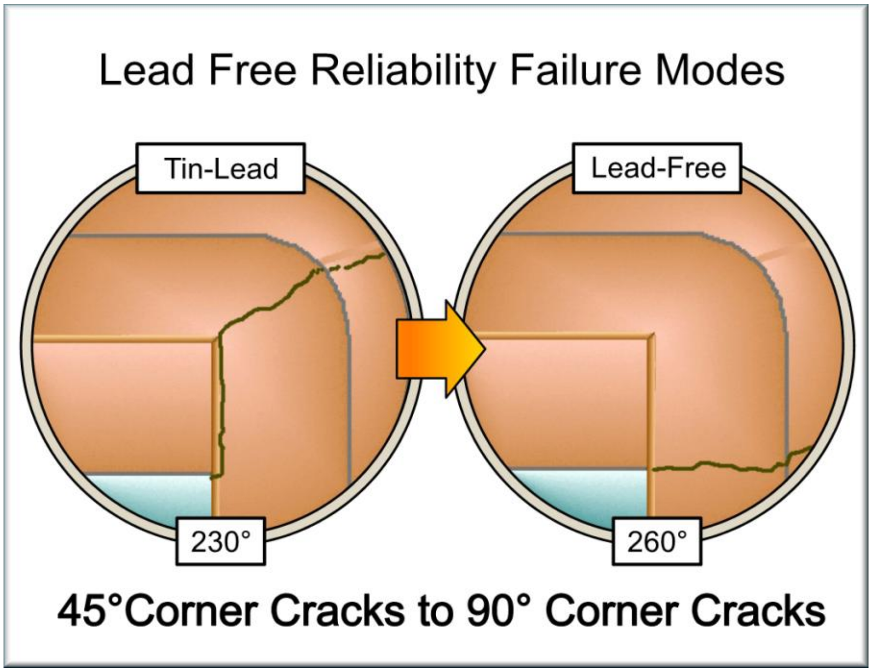


Figure 16 – Lead-Free induced corner cracks

Materials' testing in support of reliability, was traditionally limited to various thermal analyses. Only four types of test equipment are mentioned. Thermal mechanical analysis (TMA) measures the coefficient of thermal expansion (CTE) and glass transition temperatures (Tg). TMA is also used to measure time to delamination at various temperatures (T260, T288, and T300). A new method, informally called cyclic TMA (cTMA), incorporates the preconditioning cycles prior to time to delamination (cT260, cT288 and cT300) in an attempt to quantify the effect of assembly on dielectric materials. Dynamic mechanical analysis measures the viscoelastic properties of materials including Young's and loss moduli and tan delta Tgs. Thermal gravimetric analysis (TGA) establishes time to decomposition.

It appears the preconditioning at 260°C is at the limit of most FR4 based dielectric systems. As a result of the degradation of material induced by lead-free assembly, the dielectric material has a significant influence in reliability. The standard thermal analysis testing was not able to anticipate the robustness of materials in a given application. A practical method was developed to find material damage in coupons.

Assembly and rework at 260°C appears to be at the limit of most FR4 based dielectric system's temperature range, if PWB reliability is the standard. To that end, some test coupon designs (IST) are now incorporating capacitance planes on the layers that are ground planes in the PWB. These layers allow the measurement of capacitance, typically in picoFarads (fP) between planes. Subtle changes in the dielectric can be measured with this method. Material damages in to form of delamination, cohesive failure, crazing, material decomposition may be sensed. Other influences that can be sensed include changes in dielectric constant (i.e. curing) and moisture content. Measurements are taken and recorded in the "as received" coupon, after preconditioning and at end of test. Compared to baseline measurement a change in capacitance may reflect material damage (figure 17).

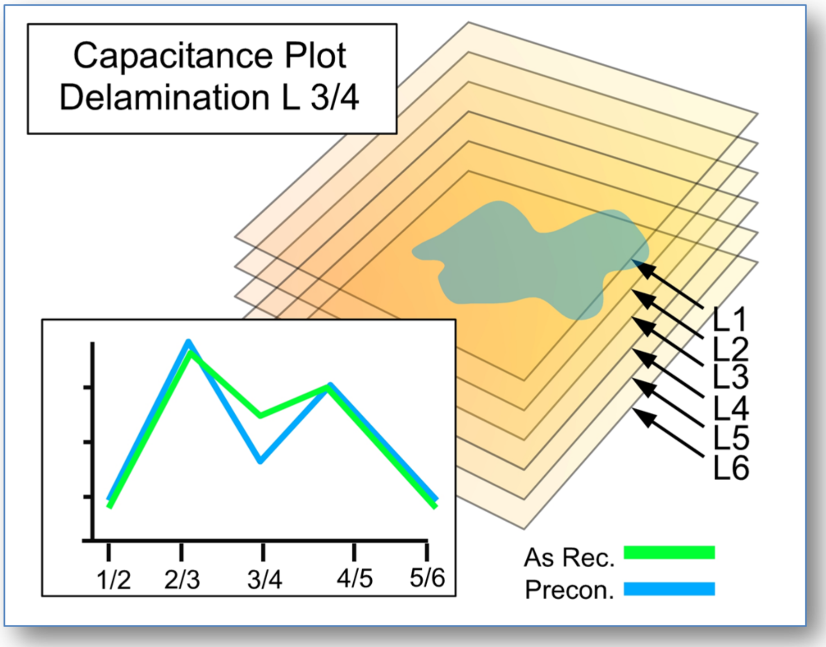


Figure 17 - Capacitance Layer with Delamination

Microsections are used to confirm material damage on the coupons with the greatest changes in capacitance. Although there is no practicle method to find the precise location of where the coupon may be delaminated, microsections in the middle zone of the coupon appear adequate to confirm or refute material damage.

Based on morphology and failure modes, four types of material damage have been identified and are referred to, for the purposes of this paper, as: adhesive delamination, cohesive failure, crazing and material decomposition (figure 18). It appears that a fifth material condition often referred to as cratering is an associated failure mode but, cratering has not been expressed as an influence in thermal cycles to failure test PWBs and is not sensed by established capacitance measurements. Coupons with lifted (rotated) pads, that have dielectric attached to the pad, and associated cracks in the dielectric, may anticipate cratering in assembly.

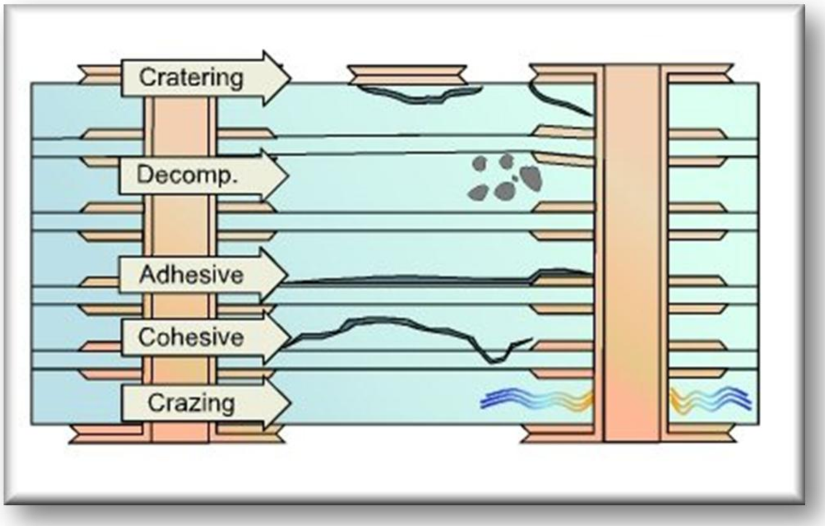


Figure 18 – Overview of Types of Dielectric Damage

It has become obvious that reliability evaluations must include testing the copper interconnections and the dielectric material in order to demonstrate robustness in lead/free applications. Material damage frequently artificially extends thermal cycles to failure by stress relieving interconnect structures. False positive test results are a consequence of material failure that goes undetected. It should be noted that material damage provides a path for conductive anodic filament (CAF) growth.

Adhesive Delamination: Adhesive delamination (figure 19) is a break between physical planes within the coupon. The most common is between the b-stage epoxy layer and c-stage or copper layers. On occasion the delamination will be between the epoxy and glass bundles but this is not to be confused with crazing where the crack is between epoxy and individual glass fibers. This type of delamination appears as round blisters or crosses and squares that are associated with warp and weft of the glass weave. Viewed in cross section cracks appear long and between laminated planes with pointed ends. It is thought that this failure may be a result of mechanical force being applied to the material like out gassing of volatiles or a failure of oxide coatings on internal copper traces or planes.

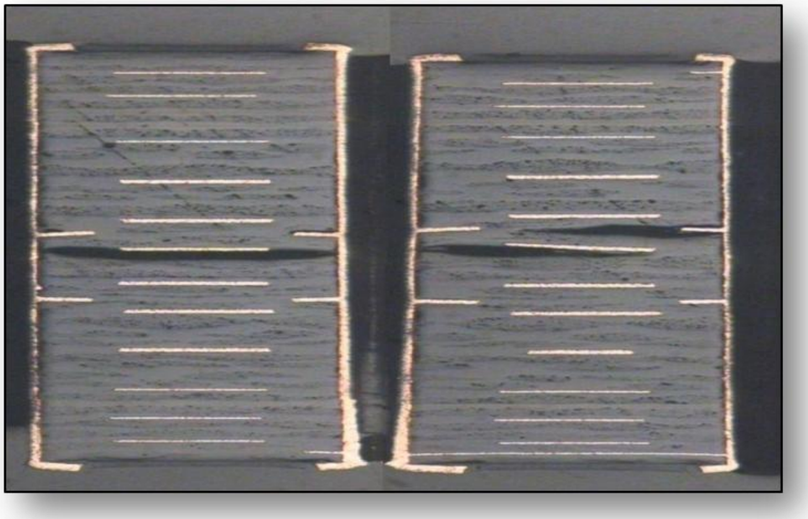


Figure 19 – Adhesive Delamination

Cohesive Failure**:** Cohesive failure (figure 20) appears to be a failure of the epoxy system. The failure appears to be closely associated with a chemical degradation of the material and less a mechanical force induced failure. On cross section the cracks are not limited to a physical plane and may cross between b-stage and c-stage boundaries. The cracks are present as angular sections sometimes bifurcating into two arms.

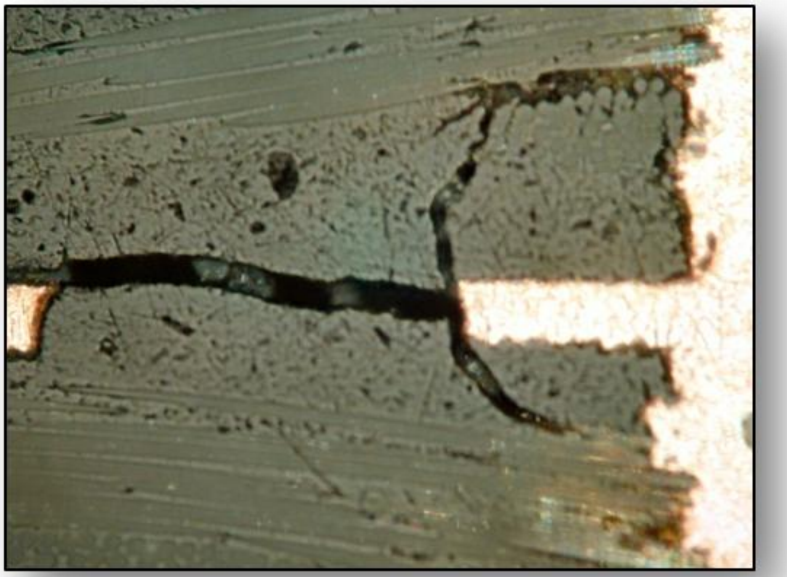


Figure 20 - Adhesive Delamination

Crazing: Crazing (figure 21) may be defined as a separation between the epoxy and individual glass fibers in the dielectric material. The defect appears at the edge of a drilled hole and proceeds down the length of the glass bundle. On cross section the condition appears to refract light and can bridge between holes and adjacent interconnections. Crazing does not connect directly to internal traces as there is usually a butter coat of pure epoxy above and below internal traces and glass bundles. Crazing may connect directly to the adjacent PTHs and frequently copper is observed penetrating down the glass bundles (wicking) for a short distance. The sizes of the cracks along the glass fiber are such as they are most likely conducive to capillary action of liquids. This is the common path for CAF.

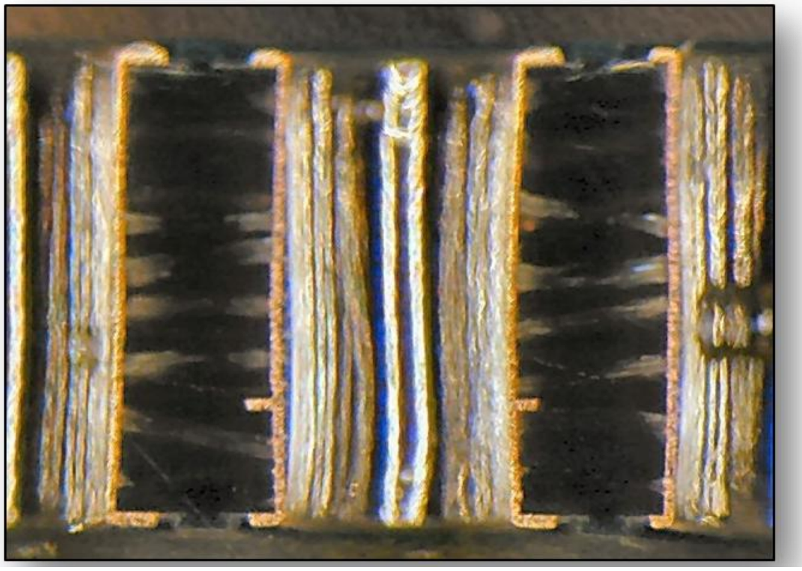


Figure 21 - Crazing along Glass Fibers – Longitudinal view between PTHs

Material Decomposition: Material decomposition (figure 22) is infrequently observed. On occasion low performance materials are tested in lead-free applications with the result of carbonizing the dielectric material. On cross section decomposed materials present severe pad rotation with bubbles in a blackened epoxy. Decomposed material is frequently observed "oozing" out beside PTHs. It is obvious that decomposed material has boiled and burned.

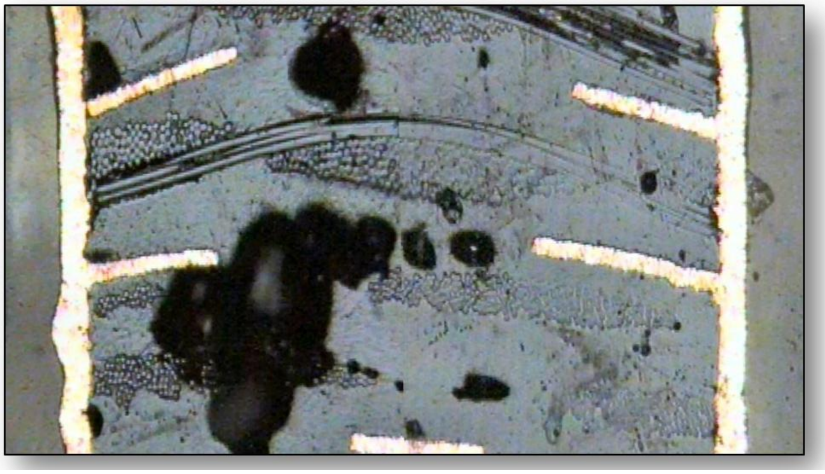
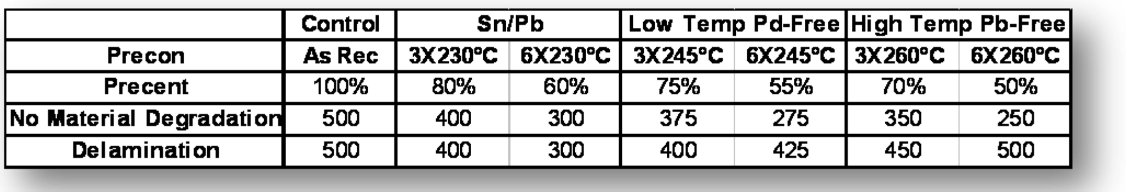


Figure 22 - Material Decomposition

If one were to take the mean cycles to failure result of a coupon tested "as received" as the reliability entitlement, then compare that number to cycles to failure of coupons preconditioned to tin/lead and lead/free temperatures, a reasonable reliability expectation could be inferred. One would expect cycles to failure to be reduced to a greater degree as the preconditioning temperature and number of cycles is increased. The data in table one has been normalized to 500 cycles for the "as received" tested coupons. The typical degradation due to various levels of preconditioning is shown. On well made coupons without material damage a 50% reduction in reliability is common after assembly and rework simulation.

Reduction in Reliability Based on Preconditioning

Table 1



	Control	Sn/Pb		Low Temp Pd-Free		High Temp Pb-Free	
Precon	As Rec	3X230°C	6X230°C	3X245°C	6X245°C	3X260°C	6X260°C
Precent	100%	80%	60%	75%	55%	70%	50%
No Material Degradation	500	400	300	375	275	350	250
Delamination	500	400	300	400	425	450	500

When material damage was present, the thermal cycles to failure increased. Crazing, adhesive delamination, cohesive failure and material decomposition, all can have the net effect of stress relieving the copper interconnections, protecting the copper from accumulating damage, and artificially extending cycle to failure data. It has become apparent that material damage can confound thermal cycle to failure data and give false positive results. Both the material and copper interconnections must be evaluated in concert in order to achieve an accurate reliability evaluation of representative coupons.

In summary, the best way to realize the most from reliability testing of PWBs is to assure the test method and coupon design will support the testing goal, by confirming compliance or discriminating between test variables. Reliability testing can be broken down into three testing approaches; compliance or acceptance testing, design of experiment or testing in order to rank and compare variables, and survivability or accelerated testing at high temperatures. Compliance testing requires a coupon that has the important attributes of the product. DOE and comparative testing may be confounded by surface finishes particularly nickel finish and the process temperatures inherent in HASL finishes. Survivability testing may induce atypical failure modes but does not change of order of failure; weak coupons fail earlier than robust coupons tested at any temperature. Preconditioning to simulate assembly and rework is used to stress coupons and evaluate the impact of assembly and rework on overall reliability. Typically testing effective reliability is performed to 150°C. Higher test temperatures are becoming more popular by expanding the testing capability to find weaknesses in otherwise robust interconnections and reduce test times. Acceleration testing to predict field life is typically done at 150°, 160° and 170°C. Microvias are tested at 190°C, polyimide circuits at 210°C and survivability testing is done at 220°C to 260°C. By stopping testing promptly at a 10% increase in resistance, a circuit will not be open allowing a small current to be applied to the failing circuit. This allows precise failure location by means of a thermal imaging camera of the interconnection that has accumulated the most damage. Microscopic evaluation of the developing failure allows insight into the expressed and latent failure modes. Failure modes are shifting due to lead free assembly; metal fatigue tends to be present as barrel cracks that are open at ambient, interconnect separation is present as larger post separation with displaced copper foil and corner cracks are changing from a 45° crack to a horizontal crack. Standard and Weibull analysis can be applied in novel ways to enhance both coupon selection and data evaluation. It is imperative to include evaluation of both copper interconnections and materials for lead-free applications. Changes in capacitance been used successfully to enunciate material damage in specifically designed test vehicles. Damage to material includes adhesive delamination, cohesive failure, crazing and material decomposition. Material damage, if undetected my give false positive results by stress relieving copper interconnections. A well made PWB, fabricated with high reliability material and conservative designs can expect a 50% reduction in reliability due to the temperature associated with lead-free processing.

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Mike has 34 years experience in the electronics industry with the majority of that experience in pcb fabrication. He started his electronics career working as a Cable TV Technician (aka Cable Boy). From there he moved into the pcb fabrication industry working at captive pcb fabrication facilities for major OEM's. Since then he has worked at independent pcb fabricators, in the semiconductor packaging industry, in semiconductor substrate fabrication, and in a couple of high technology start-ups in jobs ranging from co-founder, product and process development, Engineering Management, Manufacturing Management, and Technical Marketing.

Mike has a BS in Mathematics and Chemistry from the University of Wisconsin and a MBA from the University of Minnesota. He currently works at Sun Microsystems, Inc. as an Interconnect Specialist supporting Sun's high end Enterprise Server Group. Mike has been awarded eight patents in the area of packaging and signal integrity and has a number of patents pending.

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Paul Reid's' career in printed circuit board fabrication and reliability testing spans 31 years. Paul received a Bachelor in Science degree in 1975 and a Master in Science in 1980 from Rivier College, Nashua, New Hampshire. Paul has worked in Quality and Engineering in Managerial roles in New England and Canada. He is active in IPC on a number of committees. Articles and papers have been published in industry periodical and he has offered presentations for a number of technical organizations supporting the electronics industry. He has created technical animations of PCB fabrication, and failure modes induced by thermal excursions in support of reliability testing. His animations have been used for education, technical reports and promotions internationally. Paul is a Program Coordinator at PWB Interconnect Solutions Inc., Ottawa, where his duties include reliability testing, failure analysis and material analysis. He is currently investigating the effect of lead-free (RoHS) assembly on PCB reliability.

Acknowledgements

Appreciation is extended to Bill Birch and Jason Furlong at PWB Interconnect Solutions for the on going support and development of methods and release of information in support of this overview approach for effective reliability testing. Metallurgical specimens were processed with the support of Flavio Brutesco.

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