Status and Outlooks of Flip Chip Technology

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Abstract
Status of flip chip technology such as wafer bumping, package substrate, flip chip assembly, and underfill will be presented in this study. Emphasis is placed on the latest developments of these areas in the past few years. Their future trends will also be recommended. Finally, the competition on flip chip technology will be briefly mentioned.

Introduction
The flip chip technology was introduced by IBM in the early 1960s for their solid logic technology, which became the logical foundation of the IBM System/360 computer line [1]. Figure 1(a) shows the first IBM flip chip with three terminal transistors, which are Ni/Au plated Cu balls embedded in a Sn–Pb solder bump on the three I/O pads of transistor. A Cr–Cu–Au adhesion/seed layer is deposited between the Al–Si contact pads on the Si chip and the solder bump. Figure 1(b) shows the first IBM flip chip assembly (three chips) on a ceramic substrate.

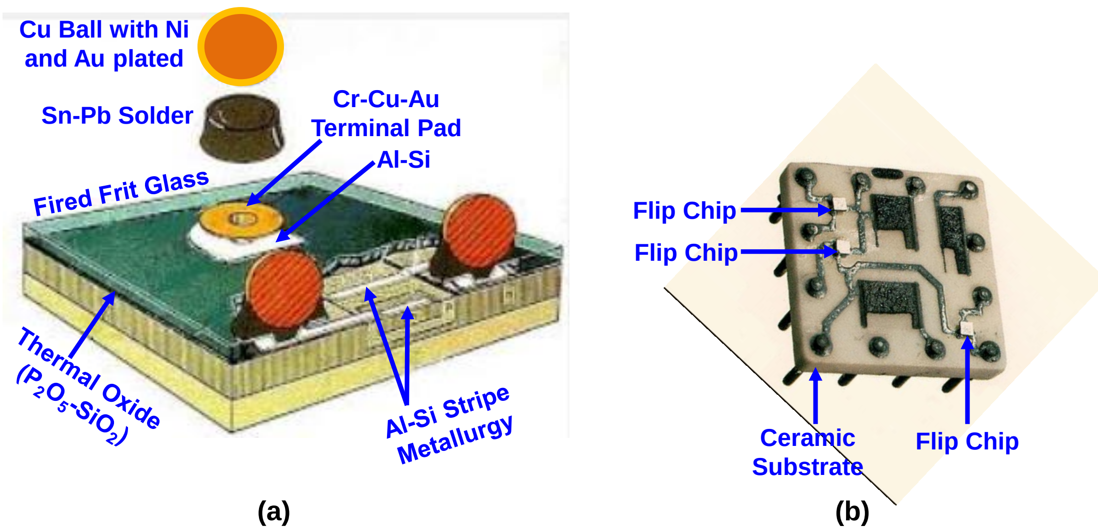

Figure 1 - (a) IBM's first flip chip component with 3 terminal transistors. (b) IBM's first flip chip assembly (3 chips) on a ceramic substrate

As the I/Os increase, the Cu ball is replaced by solder bump. The so-called C4 (controlled-collapse chip connection) technology [2] utilizes high-lead solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and all solder joints are made simultaneously by reflowing the solder.

Today, the applications of flip chip technology have been extended to [3, 4, 5] chip-to-chip, face-to-face, and face-to-back. Figure 2(a) shows Amkor's Double-POSSUM™ package [6]. It can be seen that the package is actually defined by two levels of nesting die. The three daughter dies are flip-chip attached to the larger mother die which is then attached to the largest grandma die. The grandma die is then flip-chip attached to the package substrate. The bumps between the daughter dies and the mother die are microbumps (Cu-pillar with solder cap). C4 bumps are used between the mother die and grandma die, and between the grandma die and package substrate. Figure 2(b) shows Samsung's 3D IC integration technology for the DDR4 (double data rate type 4) DRAM (dynamic random access memory) of their 128GB RDIMM (registered dual inline memory module). It can be seen that the DRAMs are bonded (stacked) with microbumps and NCF (non-conductive film).

Flip chip technologies have been used extensively for the processors of mainframe computers, servers, personal computers, notebooks, smartphones, tablets, games, etc., the application specific integrated circuits (ASICs) of networking, telecommunications, etc., and the memories of data storage devices, etc. Most of the flip chip assemblies are mass reflowed. Recently, because of the requirements of higher functionalities of the chips and shrinking the chips' area, the number of pin-outs of the processors, ASICs, and memories increases and their pitch (or the spacing between the pin-out pads) decreases.

Also, because of the trends of smaller form factors for mobile (e.g., smartphones and tablets) and portable (e.g., notebooks) products, the thickness of the chips and package substrates must be as thin as possible. Higher pin counts, tighter pitches, thinner chips, and thinner package substrates lead to the necessity of the thermocompression bonding (TCB) method for flip-chip assemblies. In this study, besides mass reflow, various TCB techniques are mentioned.

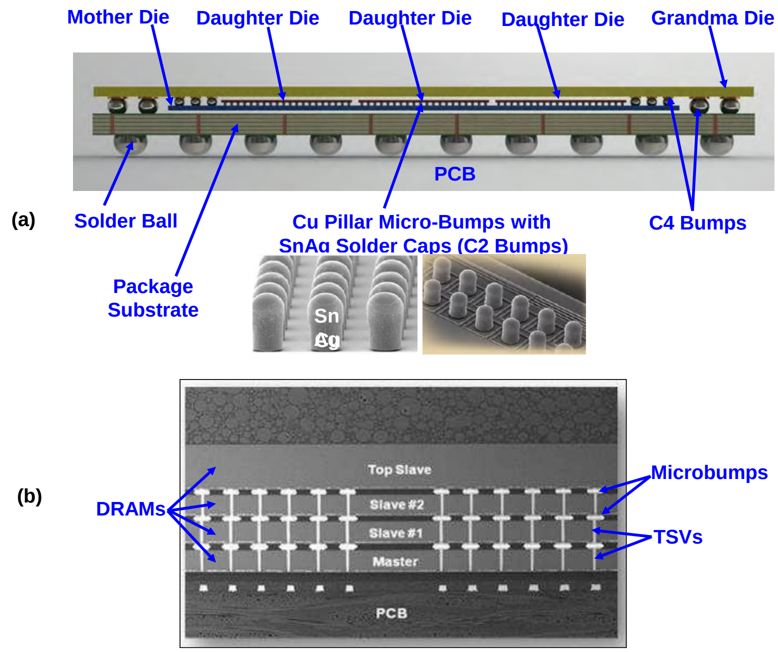

Figure 2 - (a) 3D IC packaging and (b) 3D IC integration

Recent advances in high-density and low-cost package substrates have promoted more flip chip applications. In this study, the organic build-up substrate, through-silicon via (TSV)-interposer, TSV-less interposer, coreless substrate, bump-on-lead (BOL), and embedded-trace-substrate (ETS) will be discussed.

In order to enhance the solder joint reliability of flip chip assemblies, underfill is a must, especially for organic package substrate. In this study, the pre-assembly underfill such as the no-flow underfill (NUF), nonconductive paste (NCP), and nonconductive film (NCF) will be discussed. Also, the post-assembly underfill such as the capillary underfill (CUF) and molded underfill (MUF) will be examined. Since wafer bumping is the mother of flip chip technology, it will be briefly mentioned first.

Wafer Bumping

There are many ways to perform the wafer bumping (at least 12 are shown in [7]), and the most common method is by electrochemical deposition (ECD) or electroplating [8]. Stencil printing method [9, 10] is also used for wafer bumping but it will not be presented herein.

C4 Bumps. Usually the pad size is equal to 100µm and the target bump height is equal to 100µm. After redefining the passivation opening (usually it is not required), either Ti or TiW (0.1–0.2µm) are sputtered over the entire surface of the wafer first, followed by 0.3–0.8µm of Cu. Ti–Cu and TiW–Cu are called under bump metallurgy (UBM). In order to obtain 100µm bump height, a 40µm layer of resist is then overlaid on the Ti–Cu or TiW–Cu and a solder bump mask is used to define (ultraviolet exposure) the bump pattern as shown in steps #1–4 in Figure 3. The opening in the resist is 7–10µm wider than the pad opening in the passivation layer. A 5µm layer of Cu is then plated over the UBM, followed by electroplating the solder. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve the target (100µm), the solder is plated over the resist coating by about 15µm to form a mushroom shape. The resist is then stripped off and the Ti–Cu or TiW–Cu is removed with a hydrogen peroxide or plasma etching. The wafer is then reflowed with flux, which creates smooth truncated spherical solder C4 bumps, due to surface tension as shown in steps #5–8 on the upper right-hand side of Figure 3 [7, 8].

C2 (Cu-Pillar with Solder Cap) Bumps. Because of higher pin-count and tighter pitch (smaller spacing between pads), there is a possibility of shorting the adjacent solder C4 bumps. Wire interconnects [11] and Cu-pillar with solder cap [12, 13] can be a solution. The fabrication process is basically the same as that of the C4 bumps except electroplating the Cu instead of solder as shown in step #5 on the lower right-hand side of Figure 3. It is followed by electroplating the solder cap and then reflowing the solder with flux. Because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the self-alignment of the Cu pillar with the solder cap bump and therefore, it is sometimes called a C2 (chip connection) bump. Besides being able to handle finer pitch, C2 bumps also provide better thermal and electrical performances than C4 bumps. This is because the thermal conductivity (W/m K) and electrical resistivity (μΩm) of Cu (400 and 0.0172) are superior than those (55–60 and 0.12–0.14) of solder.

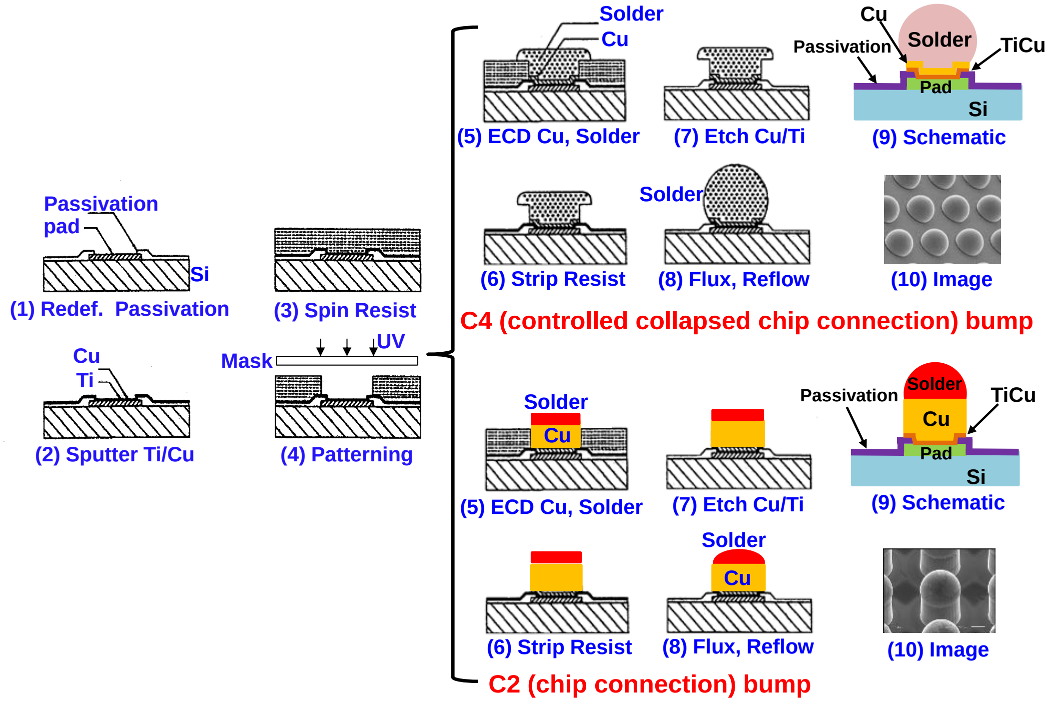

Figure 3 - Wafer bumping by ECD or electroplating method for C4 and C2 bumps

Flip Chip Package Substrate

In the past few years, tremendous efforts have been devoted to enhance/advance the capabilities of the conventional low-cost build-up organic package substrates by increasing the number of build-up layers, fabricating thin-film layers on top of the build-up layer, shrinking the dimensions of the metal line width and spacing, reducing the pad size and pitch, eliminating the core, making the BOL, and laminating the ETS. For silicon substrates, first come with the TSV-interposer and the future trend is for TSV-less interposer. Ceramic substrate will not be discussed herein.

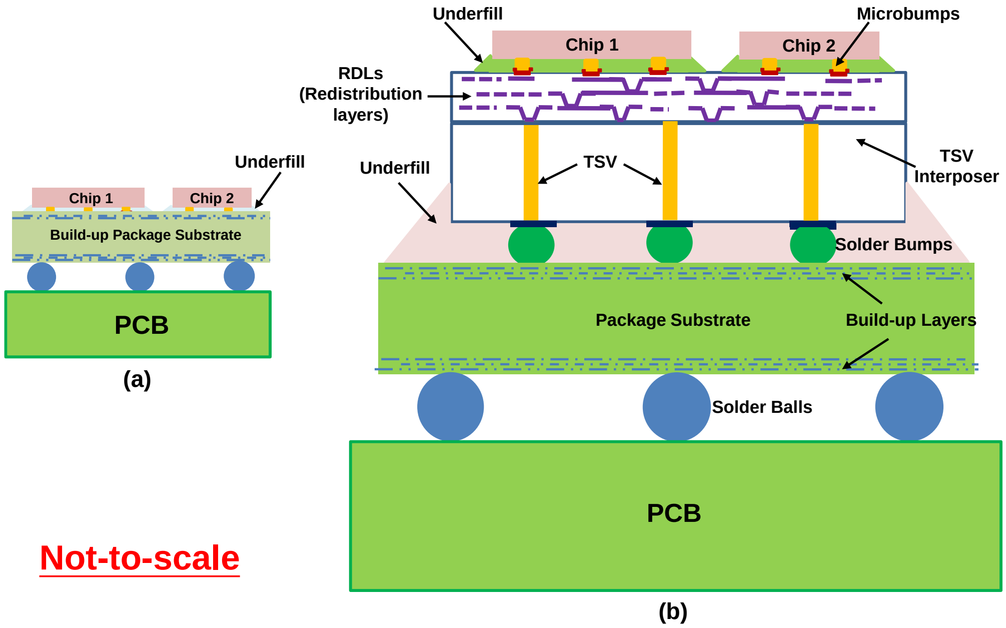

Figure 4 - (a) Build-up package substrate for flip chips. (b) Build-up substrate with TSV-interposer for flip chips

Surface Laminar Circuit (SLC) Technology. Almost 25 years ago, IBM in Japan at Yasu invented the SLC technology [14, 15], which formed the basis of today's very popular low-cost organic package substrates, Figure 4(a), with build-up layers vertically connected through microvias [16] to support flip chips. There are two parts of the SLC technology: one is the core substrate and the other is the SLC for the signal wiring. The core substrate is made by the ordinary glass epoxy panel. However, the SLC layers are sequentially built up with the dielectric layers made of photo sensitive epoxy and the conductor plane of copper plating (semi-additive technique). In general, a package substrate with twelve layers (e.g., two core-layers and ten build-up layers (5-2-5)) and 10µm-linewidth and spacing is more than adequate to support most of the chips.

TSV-Interposers. In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced field programmable gate array (FPGA), even a twelve build-up layers (6-2-6) package substrate is not enough to support the chips and a TSV interposer, Figure 4(b), is needed [17, 18]. For example, the left-hand side of Figure 5 shows the Xilinx/TSMC's sliced FPBG chip on wafer on substrate (CoWoS). It can be seen that the TSV interposer has four top RDLs (redistribution layers): three Cu damascene layers and one aluminum layer. The 10,000+ of lateral interconnections between FPGA chips are connected mainly by the RDLs of the interposer.

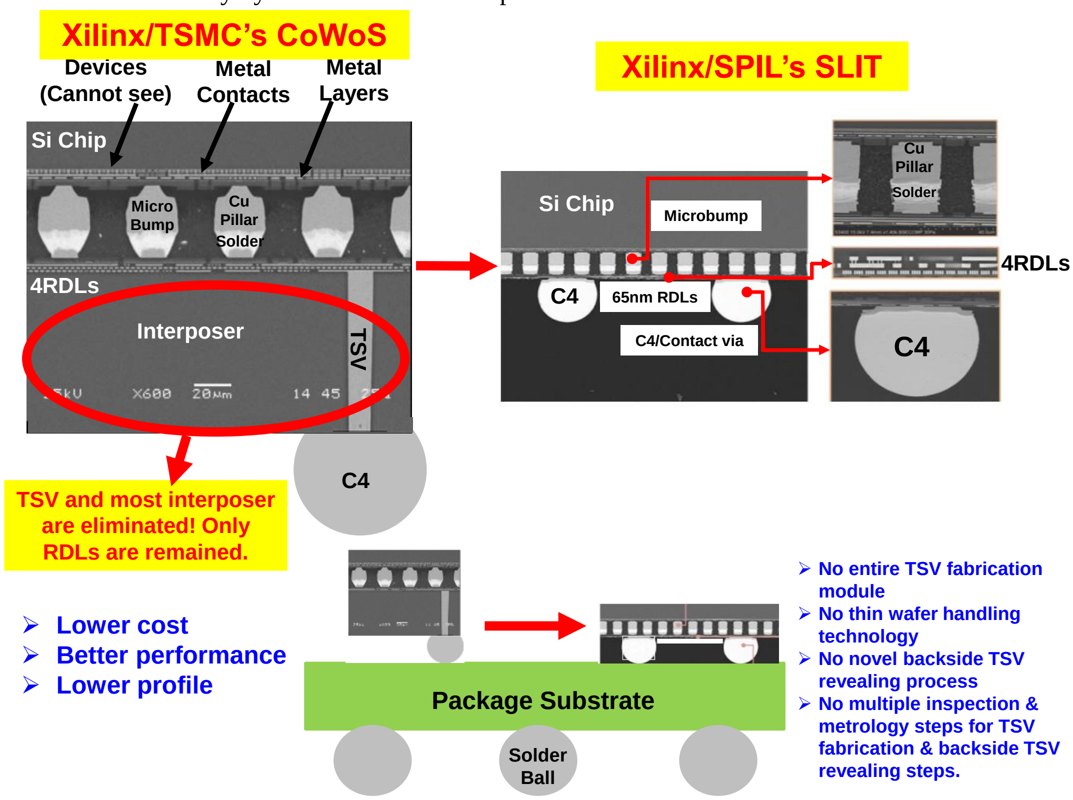

Figure 5 – Xilinx/TSMC's CoWoS (left) and Xilinx/SPIL's SLIT (right)

TSV-Less Interposer: Xilinx/SPIL's Silicon-Less Interconnect Technology (SLIT). So far, TSV-interposer is very expensive [3-5]. In order to lower the cost, enhance the electrical performance, and reduce the package profile, in 2014 Xilinx/SPIL proposed a TSV-less interposer for the sliced FPGA chips called SLIT [19]. The right-hand corner of Figure 5 shows the new packaging structure. It can be seen that the TSVs and most of the interposer are eliminated and only those four RDLs are kept to perform, mainly, the lateral communication of the sliced FPGA chips. Depending on the linewidth/spacing of RDLs' conductive wiring, the fabrication method of RDLs can be either by using a polymer for the dielectric layer and ECD Cu for the conductive wring (linewidth/spacing ~5µm), or by using plasma enhance chemical vapor deposition to make the SiO_2 dielectric layer and Cu damascene + chemical–mechanical polishing (CMP) to make the conductive wring (linewidth/spacing <5µm). Figure 6 schematically shows the cross section of Xilinx/SPIL's SLIT.

TSV-Less Interposer: SPIL/Xilinx's Non-TSV Interposer (NTI). In 2016, SPIL/Xilinx published a similar paper [20] with more characterization results such as warpage data and called it non-TSV interposer (NTI).

TSV-Less Interposer: Amkor's Silicon Interposer-Less Integrated Module (SLIM). In 2015, Amkor announced a very similar technology to SLIT and is called SLIM [21].

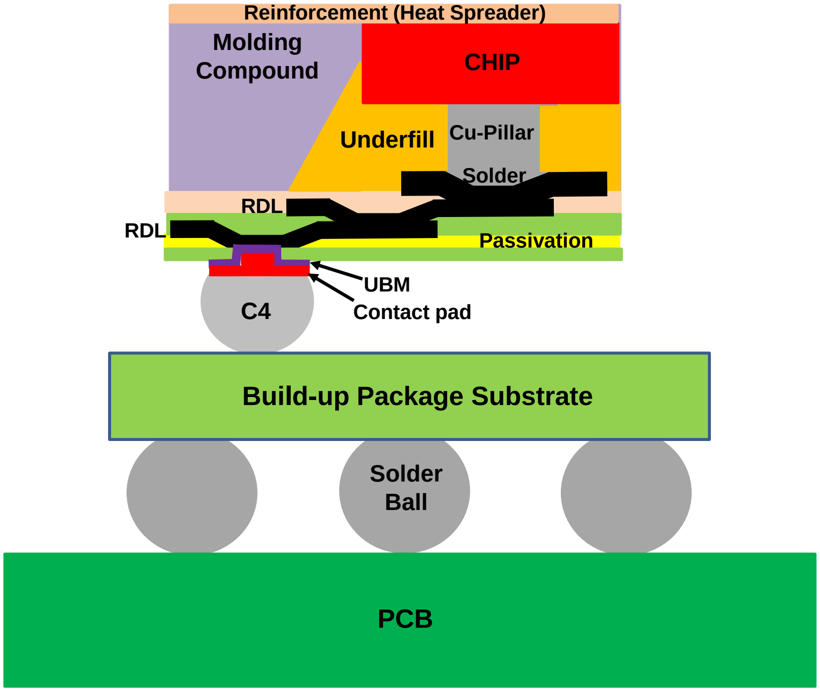

Figure 6 - Xilinx/SPIL's SLIT

TSV-Less Interposer: Intel's Embedded Multidie Interconnect Bridge (EMIB). In September 2014, Intel proposed an EMIB [22] to replace the TSV-interposer. The lateral communication between the chips will be taken care of by the silicon embedded bridge and the power/ground and some signals will go through the vias of the organic package substrate to the PCB as shown in Figure 7 [23]. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB and the other is to make the substrate with EMIB. For making the EMIB, first build the RDLs (including the contact pads) on a Si-wafer by either polymer + ECD or Cu damascene + CMP methods. Then, thin down the wafer to <100µm. Finally, attach the non-RDL side of the Si-wafer to a die-attach film and then singulate the Si-wafer.

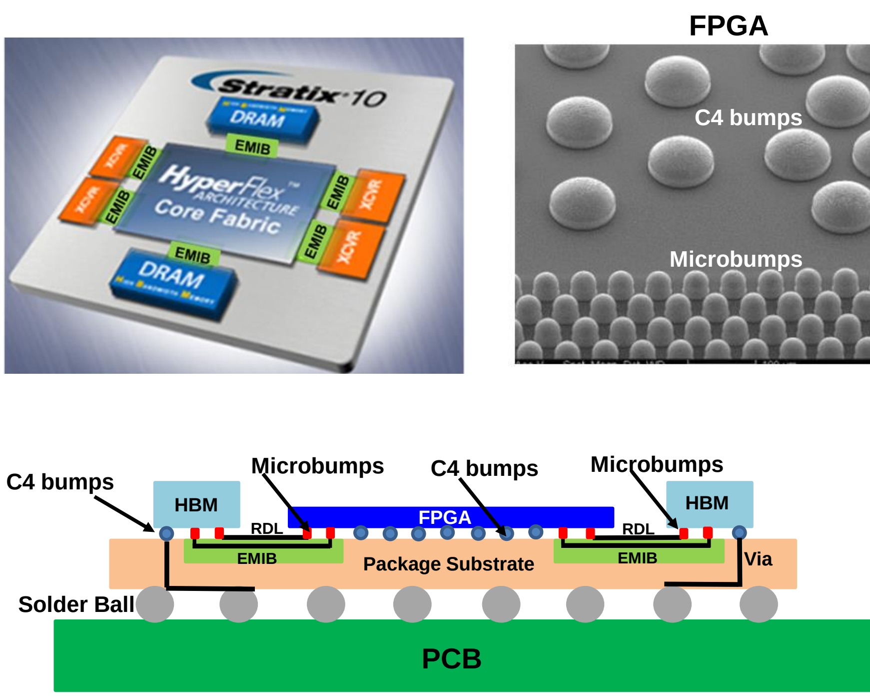

Figure 7 - Intel/Altera's high bandwidth communications between the FPBA and HBMs by EMIB

For making the substrate with EMIB, first place the singulated EMIB with the die-attached film on top of the Cu foil in the cavity of the substrate, Figure 8(a). It is followed by laminating a dielectric film on the whole organic package substrate. Then, drilling (on the dielectric film) and Cu plating to fill the holes (vias) are done to make connections to the contact pads

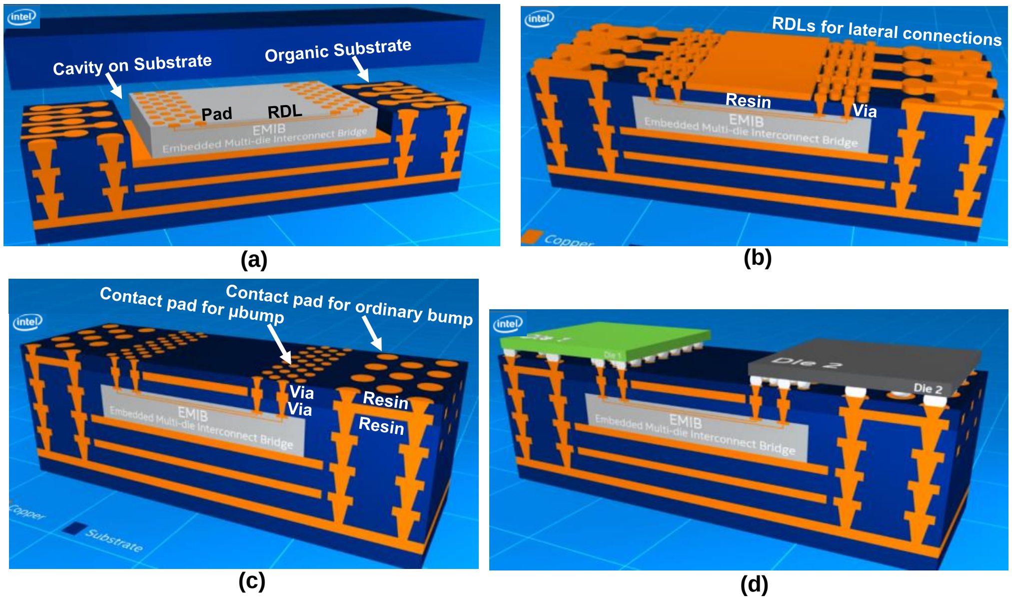

Figure 8 - Simple process flow of the Intel EMIB technology

of the EMIB. Continue Cu plating to make lateral connections of the substrate as shown Figure 8(b). Then, it is followed by laminating another dielectric film on the whole substrate and drilling (on the film) and Cu plating to fill the holes and make contact pads, Figure 8(c). (Smaller pads on finer pitch are for microbumps while larger pads on gross pitch are for ordinary C4 bumps.) The organic package substrate with EMIB is ready for bonding of the chips as shown in Figure 8(d).

On November 9, 2015, Altera/Intel announced [24] the industry's first heterogeneous system-in-package (SiP) devices that integrate stacked HBM (high bandwidth memory) from SK Hynix with high-performance Stratix® 10 FPGAs and SoCs (system-on-chip) as shown in Figure 7. It can be seen that the lateral communications between the chips and the HBMs are taken care of by the EMIB and a TSV interposer is not needed.

TSV-less Interposer: Cisco/eSilicon's Organic Interposer. Figure 9 shows a 3D SiP with a large organic interposer (instead of a TSV interposer) designed and manufactured by Cisco/eSilicon [25]. The organic interposer has a size of 38mm x 30mm x 0.4mm. The linewidth, spacing, and thickness of the front-side and back-side of the organic interposer are the same and are, respectively, 6µm, 6µm, and 10µm. A high-performance application-specific IC (ASIC) die measured at 19.1mm x 24mm x 0.75mm is attached on top of the organic interposer along with four HBM DRAM die stacks. The 3D HBM die stack with a size of 5.5mm x 7.7mm x 0.48mm includes one base buffer die and four DRAM core dice which are interconnected with TSVs and fine-pitch micro-pillars.

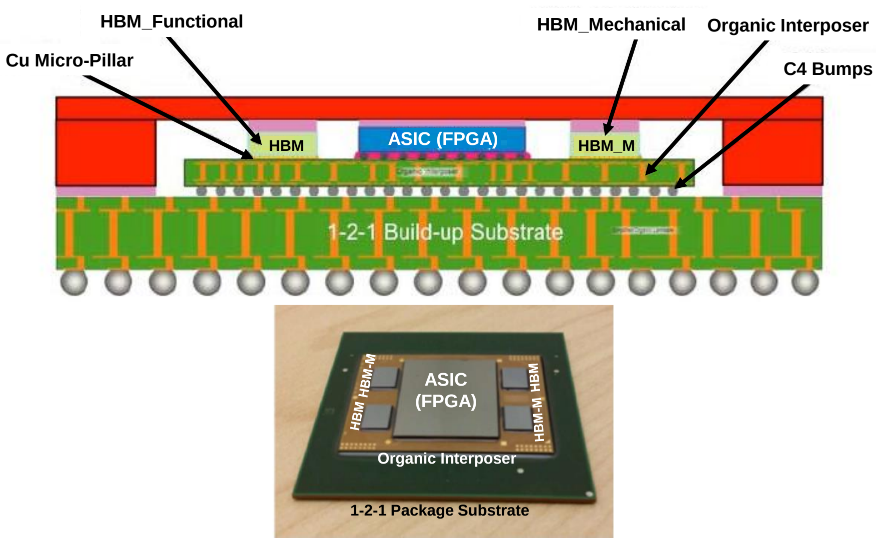

Figure 9 – Cisco/eSilicon's SiP with organic interposer

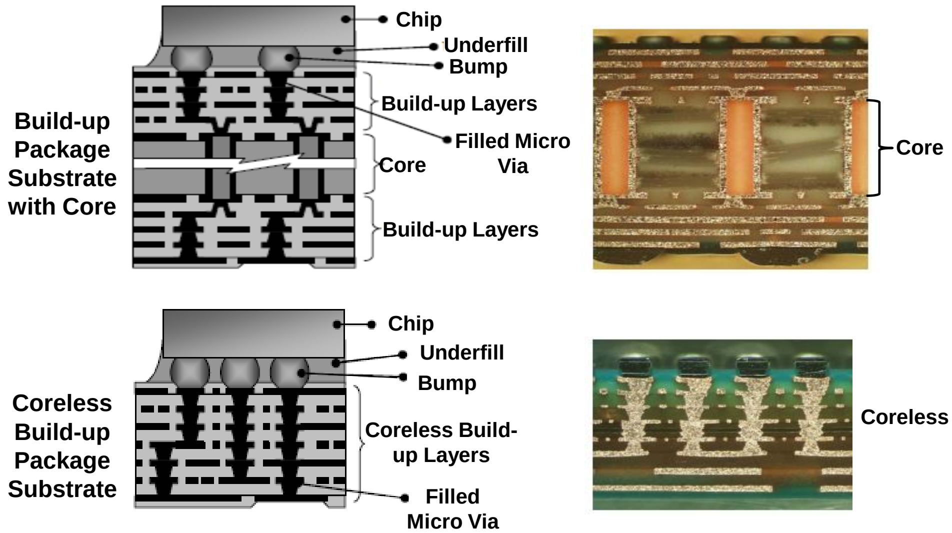

Figure 10 - (Top) flip chip on conventional build-up package substrate. (Bottom) flip chip on coreless substrate

Coreless Substrate. Coreless substrate was first proposed by Fujitsu [26] in 2006. Figure 10 shows the comparison between the conventional organic package substrate with build-up layers and the organic coreless package substrate. It can be seen that the biggest difference is that there is not a core in the coreless package substrate and all the layers of the coreless package substrate are the build-up layers. The advantages of the coreless package substrate are: (a) because of eliminating the core, the cost of the coreless substrate is lower; (b) by eliminating the core, higher wiring ability can be achieved; (c) better electrical performance because of good high-speed transmission characteristic; and (d) definitely smaller form factor. On the other hand, the disadvantages are: (a) because of eliminating the core, the warpage of the coreless substrate is larger; (b) easier to have laminate chipping; (c) poor solder joint yield because of less substrate rigidity; and (d) new manufacturing infrastructure is necessary. In 2010, Sony manufactured the first coreless package substrate for the cell processor of their PlayStation 3 [27]. Even though coreless substrates have many advantages, they are not popular because of the warpage control issue. One of the key factors affecting the warpage is the coefficient of thermal expansion mismatch of substrate materials. Thus, a proper control of this factor will help reduce the warpage issue of coreless substrates. Another factor affecting the warpage is the package assembly. Thus, a proper package assembly warpage correction control (with vacuum and pressure) will help improve the warpage problem of coreless substrate.

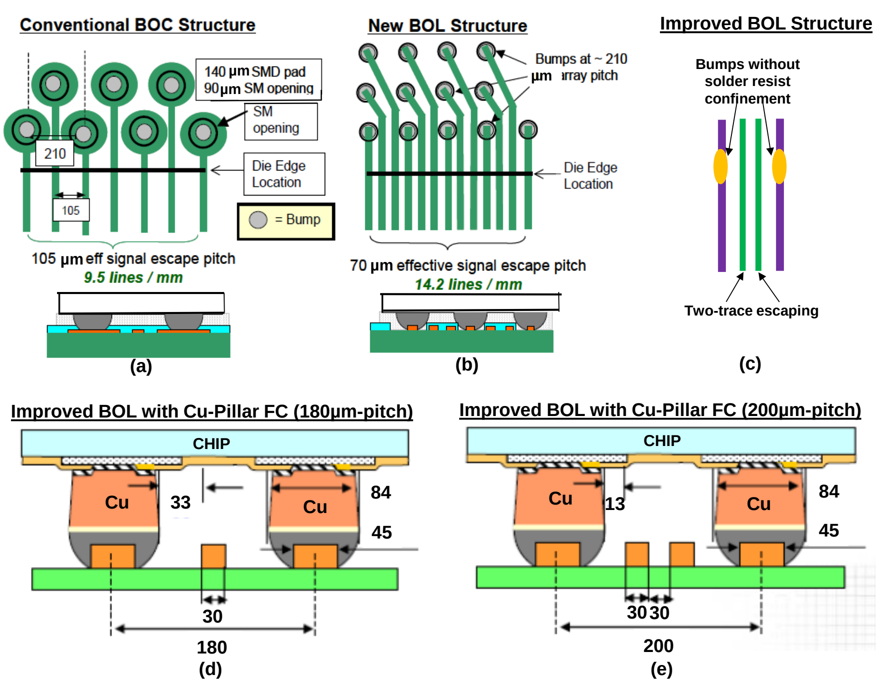

Figure 11 - BOL (a) conventional BOP, (b) new BOL, (c) improved BOL, (d) improved BOL with Cu-pillar flip chip (180µm-pitch), and (e) improved BOL with Cu-pillar flip chip (200µm-pitch)

BOL. BOL was first proposed by STATSChipPac [28] and was used by Qualcomm [29] and others [30]. A conventional bump-on-capture pad (BOC) or simply bump-on-pad (BOP) flip chip organic substrate layout is shown in Figure 11(a). It can be seen that the flip chip pads are on a 210µm area array pitch in an solder mask (SR) defined configuration with one signal escape between bump pads resulting in an effective escape pitch of 105µm. The BOL methodology is shown in Figure 11(b); here, the landing pad on the substrate is merely the trace (lead) itself, or a slightly widened version of the trace which results in freeing up of enough routing space to allow routing an additional trace between bumps thereby resulting in an effective escape pitch of 70µm without changing the design rules (trace width and space) of the substrate. The improved BOL structure is shown in Figure 11(c). It can be seen that the bump pads are without any solder resist confinement, i.e., open SR [29]. The test vehicles, Cu-column on BOL, used in [29] are shown in Figures 11(d) and 11(e). It can be seen that one trace between the 180µm bump pitch and up to two traces with the 200µm bump pitch can be comfortably routed. Typical cross sections of the perpendicular-to-BOL and longitudinal-to-BOL are shown in the upper portion of Figure 12. A 3D slide finite element model showing the BOL, BOC (or BOP), and solder joint is shown in the middle of Figure 12. The creep strain contours of the BOL solder joint are shown in the lower portion of Figure 12 [31] and are too small to create solder joint reliability problem under most conditions.

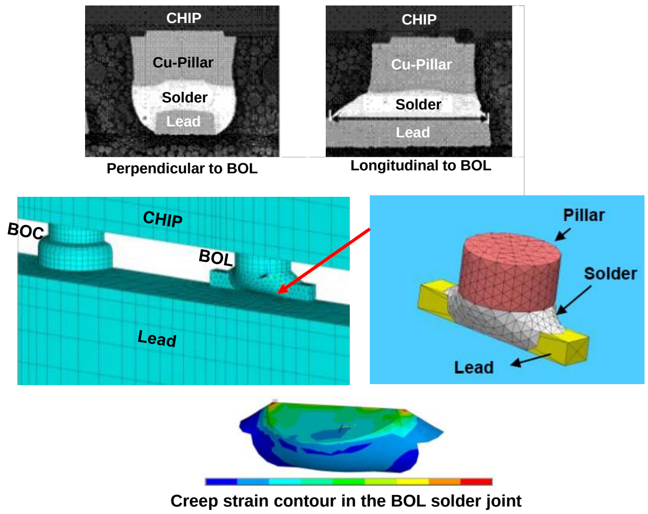

Figure 12 - Images of the perpendicular-to-BOL and longitudinal-to-BOL. Finite element models and creep strain contours in the BOL solder joint

ETS. ETS is one of the coreless substrates with fine linewidth/spacing embedding the top metal trace pattern into prepreg layer [32, 33]. The process flow of ETS is shown in Figure 13(a). It starts from a carrier board with a removable Cu foil. It is followed by using a typical electrolytic copper plating method to form the first layer of copper pattern. Then, laminate a

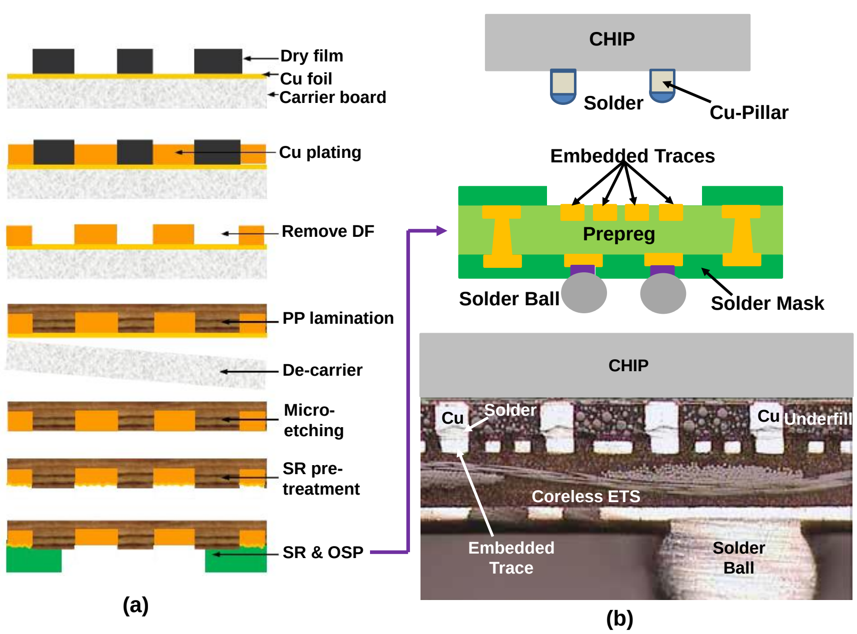

Figure 13 - (a) Process flow for fabricating the ETS and (b) flip chip with C2 bumps on ETS assembly

prepreg on the copper pattern. It is followed by laser via drilling, electroless copper coating, dry film laminating, exposing and developing, second layer copper pattern plating, stripping, and micro etching. Once all the copper pattern layers have been completed, the carrier board will be removed. Since the Cu foil is connected to the first copper pattern, micro etching is necessary before SR coating. After the SR opening process, it is completed by metal finishes treatment, e.g., organic solderability preservatives (OSPs). Figure 13(b) shows a cross section of a Cu-pillar flip chip on ETS assembly by SPIL [33]. The linewidth/spacing of ETS in use today is 15µm/15µm. However, 13µm/13µm is in production by Simmtech [34].

Flip Chip Assembly

Basically, there are two groups of flip chip assemblies: one is with an intermediate layer between the bonding pads/traces, and the other is not, i.e., nothing! Flip-chip assembly with intermediate layers such as solder for mass reflow and Cu-pillar with solder cap by TCB are called indirect bonding, which is the focus of this paper. Cu-to-Cu diffusion bonding, which does not have anything between the bonding pads/traces on the chip/wafer, is therefore, called direct bonding, which is out of the scope of the present study.

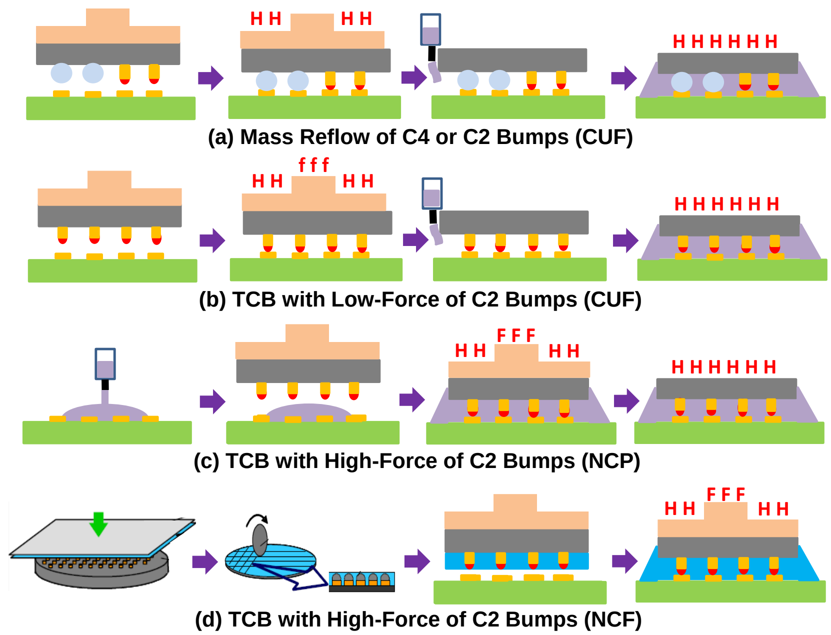

Figure - 14 Flip chip assembly: (a) mass reflow of chips with C4 or C2 bumps with CUF, (b) TCB with low-force of chips with C2 bumps with CUF, (c) TCB with high-force of chips with C2 bumps with NCP, and (d) TCB with high-force of chips with C2 bumps with NCF

C4 Solder Mass Reflow. Solder mass reflow has been used for flip-chip assembly for almost 50 years. Most of the solder C4 bumps are mass reflowed on either silicon, ceramic, or organic substrates. The assembly process is very simple, Figure 14 (a): (i) use a lookup and look-down camera to identify the location of the bumps on the chip and the pads on the substrate; (ii)

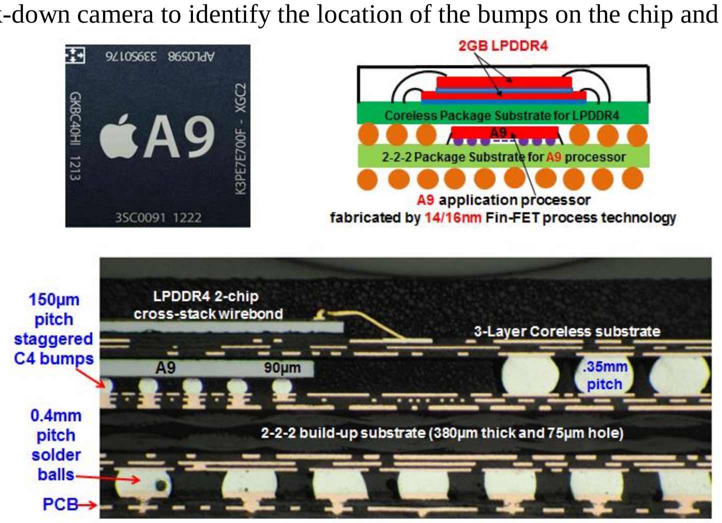

Figure - 15 PoP in Apple's iPhone 6/6+. In the bottom package, the C4 solder bumped (A9 AP) flip chip is mass reflowed on a 2-2-2 package substrate with a underfill, and then BGA to the PCB

apply flux on either the C4 bumps, or the substrate, or both; and (iii) pick and place the C4 bumped chips on the substrate, then mass reflow with temperature H. Because of the surface tension of the solder bumps during reflow, the process is very robust (self-alignment). Figure 15 shows the cross section of iPhone 6 Plus. It can be seen that the A9 application processor (AP) is housed in a PoP format (bottom package) and the solder bumped flip chip is mass reflowed on a 2-2-2 organic package substrate with underfill. In general, the spacing between the bumps on the solder mass reflow of C4 bumped chips can be as small as 50µm.

C2 Solder Mass Reflow. In the past few years, solder mass reflow of C2 (Cu-pillar with solder cap) bumped chips on either silicon, ceramic, or organic package substrates has been tried for high pin-count and fine-pitch flip-chip assemblies. The assembly process, Figure 14(a), is exactly the same as that of the C4 bumps, but the self-alignment characteristic is nowhere near the same, and thus, it is seldom being used. In general, the spacing between the pillars on the solder mass reflow of C2 bumped chips can be as small as 25µm.

C2 TCB. In the past few years, TCB of chips with an intermediate layer such as C2 (Cu-pillar with solder cap) bumps on silicon, ceramic, or organic package substrates, has been attracting attention for high-density and ultrafine pitch flip chip assemblies. Basically, there are two methods, one is with low-bonding force and the other is with a high-bonding force.

C2 TCB with Low-Bonding Force. For the one with low bonding force, the assembly process is simple, Figure 14(b): (i) first, use the look-up and look-down camera to locate the position of the C2 bumps on the chip and their corresponding pads on the substrate; (ii) apply flux on the solder cap or on the substrate or both; and (iii) pick-and-place the chip on the substrate and then apply temperature (H) to melt the solder and a low force (f) to hold the chip at a certain distance from the substrate. The above procedure is done one chip at a time and therefore, the throughput is low in comparison with the C2 solder mass reflow process. Figure 16 shows a typical cross section of a flip chip assembly with TCB with low force on C2 bumps [35]. In general, the spacing between the pillars on the C2 chip by TCB with a low-bonding force can be as small as 8µm.

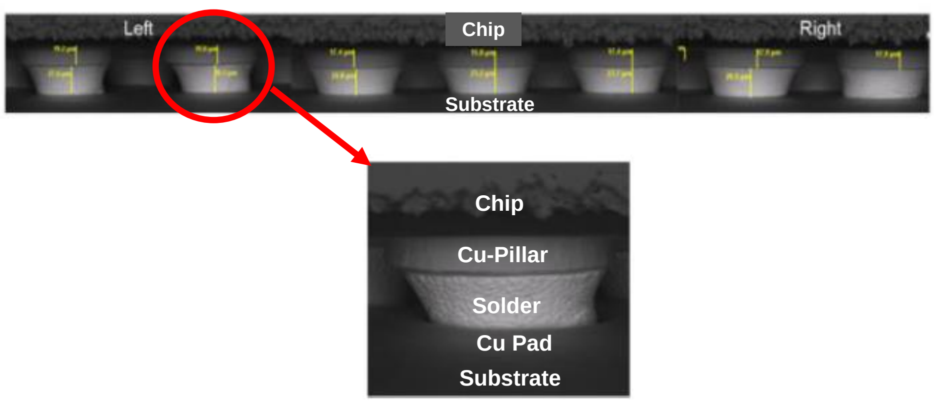

Figure 16 - Cross section of a C2 flip chip assembled on an organic package substrate by a TCB with low-force (CUF)

C2 TCB with High-Bonding Force. For TCB with a high-bonding force on the C2 chip, the assembly process must be combined with the NCP or NCF underfill, which will be discussed in the next section.

Underfill/Reliability

The reliability of flip chip solder joints is enhanced by the application of underfill [7], especially on organic substrate. Most underfills consist of low-expansion fillers such as fused silica (SiO_2) and a liquid prepolymer such as thermosetting resin (adhesive) that can be cured to a solid composite. In 1987, Hitachi showed that with underfill, the thermal fatigue life of the flip chip solder joints on ceramic substrate increased [36]. In 1992, IBM at Yasu proposed the use of the low-cost organic substrate instead of the high-cost ceramic substrate for flip chip assemblies [14, 15]. They showed that with underfill, the large thermal expansion mismatch between the silicon chip ($2.5x10^{-6}/^oC$) and the organic substrate ($15\text{-}18x10^{-6}/^oC$) is reduced substantially and the solder joints are reliable for most applications. This opened up the doors for today's very popular solder bumped flip chip on low-cost organic substrate packages used, e.g., in the processors of personal computers, notebooks, smartphones, tablets, etc. Basically, there are two different procedures to apply the underfill, namely pre-assembly underfill and post-assembly underfill.

Post-assembly Underfill. For post-assembly underfill, the application of underfill is after the flip chip assembly, i.e., the flip chip is already on the substrate and the solder joints are already mass reflowed (either with C2 or C4 bumps) or low-force TCB with C2 bumps. For post-assembly underfill, there are basically two methods, namely CUF [37] and MUF [38-43]. CUF is the first method that went into volume production. For CUF, the underfill is dispensed by a needle or jet w/o vacuum assisted on one (or two) sides of the flip chip on substrate assembly. Because of capillary action, this underfill completely fills the space between the chips, solder joints, and substrates. The chip and the substrate are then firmly bonded by curing the underfill. CUF is performed one chip assembly at a time, thus, throughput is an issue.

Molded underfill was first proposed by Cookson Electronics [38] in 2000 and later by, e.g., Dexter [39], Intel [40], Amkor [41], STATSChipPAC [42], and LETI/STMicroelectronics [43]. For MUF, the modified epoxy mold compound (EMC) is transferred molding the chip and filling the gap between the chip, solder joints, and the substrate of the flip chip assembly. The encapsulant of the chip and the underfill are formed at the same time, which will increase the throughputs. However, the challenges of MUF are: (a) the flow of MUF between the chip and the substrate is usually assisted by vacuum, (b) the size of the silica filler of the EMC must be very small for flowability, (c) the cost of the modified EMC for MUF is much higher than that for package molding, (d) package warpage is an issue due to the thermal expansion mismatch between the EMC, chip, and substrate, (e) the molding temperature is limited by the melting point of the solder joints, and (f) the standoff-height and pitch of the solder joints cannot be too small. In order to increase the throughput of CUF and avoid the drawbacks of MUF, a method of post-assembly underfill has been proposed in [44], where a stencil is designed for printing the underfill material for flip chips on organic-panel and Si-wafer assemblies.

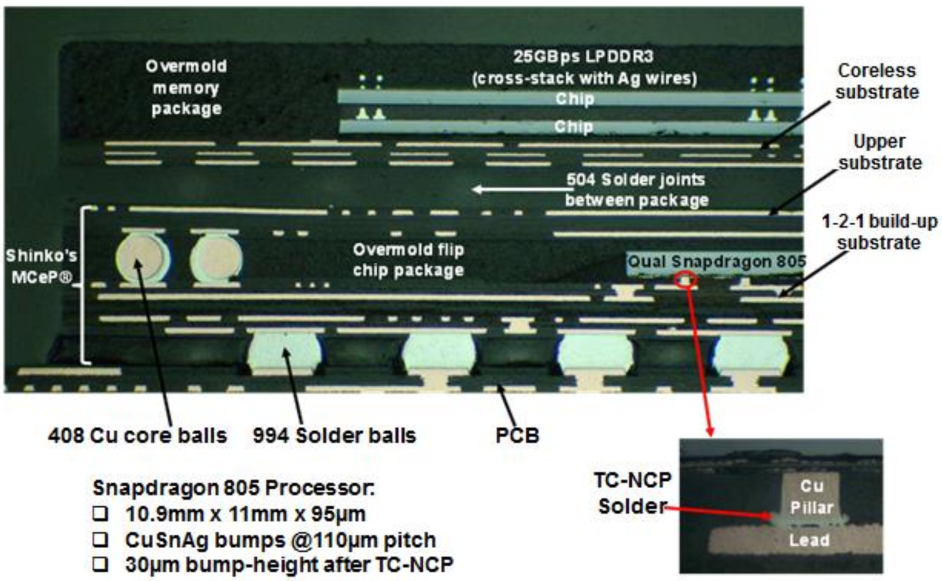

Figure 17 - PoP in Samsung's smartphone. The C2 flip chip is TCB with high-force on a package substrate (TC-NCP)

Pre-Assembly Underfill. For pre-assembly underfill, the application of underfill is either on the substrate or wafer and is before the flip-chip assembly. Solder reflow of the C4 bumps with underfill on substrates was first proposed by GIT [45] and is called NUF. High-bonding force TCB of the C2 bumps with nonconductive paste (TC-NCP) underfill on the substrate,

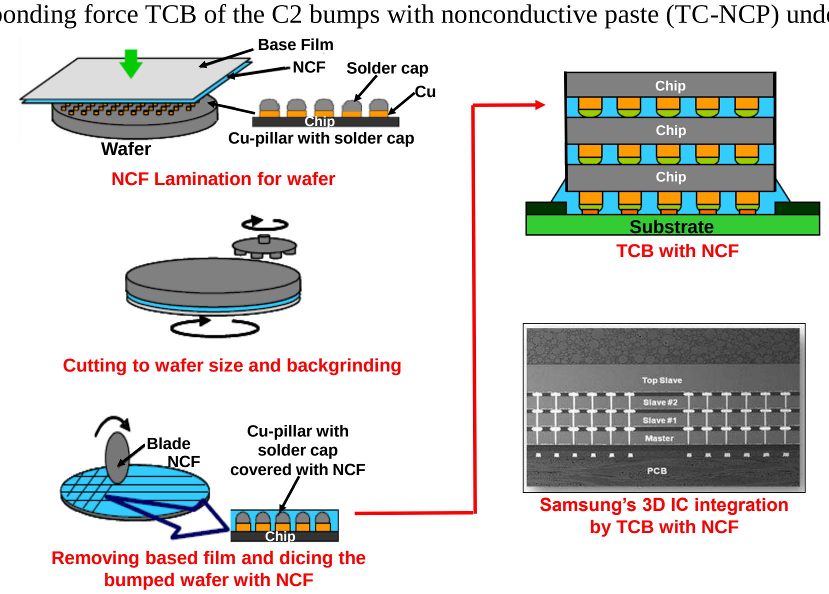

Figure - 18 Lamination of NCF on a C2 bumped wafer, dicing, and TCB of NCF flip chips (one by one)

Figure 14(c), was first studied by Amkor [46] and has been used to assemble Qualcomm's SNAPDRAGON application processor for Samsung's Galaxy smartphone as shown in Figure 17. The NUF and NCP underfills can be spun on, dispensed by a needle, or vacuum assisted.

By learning from the chip-on-glass technology, high-bonding force TCB of C2 bumps with nonconductive film underfill on wafers have been studied by, e.g., Sanyo [47], Hitachi [48, 49], Tohoku [50, 51], DOW [52], Hynix [53], KAIST/Samsung [54, 55], Amkor/Qualcomm [56], and Toray [57-59] for 3D IC integration. Figure 18 shows the lamination of NCF on the Cu-pillar with a solder cap bumped wafer. High-bonding force TCB of the C2 chips with NCF (after singulation from the laminated wafer) has been in production for 3D IC integration by Samsung on its TSV-based DDR4 DRAM, Figure 18. This 3D memory cube is stacked one chip at a time and each chip takes ~ 10s for the underfill film to gel, the solder to melt and solidify, and the film to cure. Throughput is a problem!

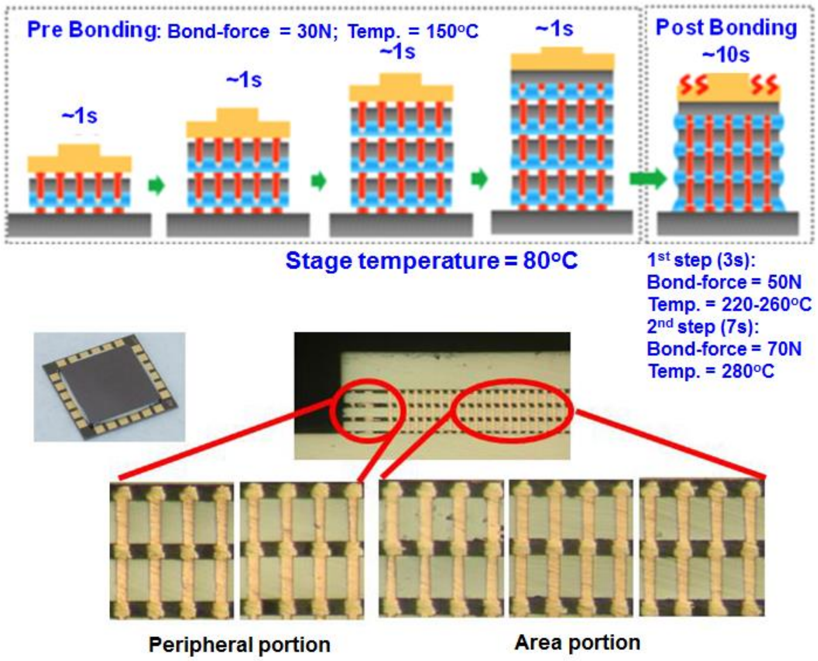

Figure 19 - Toray's collective TCB with high-force with NCF flip chips

In order to resolve this problem, Toray [58, 59] proposed a collective bonding method which is shown in Figure 19. It can be seen that the C2 chip with NCF is prebond (bond force = 30N, temperature = 150ºC, and time <1s) on a stage with temperature = 80ºC. For postbond (first step (3s): bond-force = 50N, temperature = 220–260ºC, second step (7s): bond-force = 70N, temperature = 280ºC) on a stage temperature = 80ºC. Thus, instead of using 40s in stacking up four chips by the conventional method, it only takes less than 14s by the collective TCB method. Some images of the cross section of the proposed collective bonding method are shown in Figure 19. Reasonable good joints are achieved with optimized conditions. In general, the spacing between the pillars on the C2 chip with either NCP or NCF by TCB with high bonding force can be as small as 10μm.

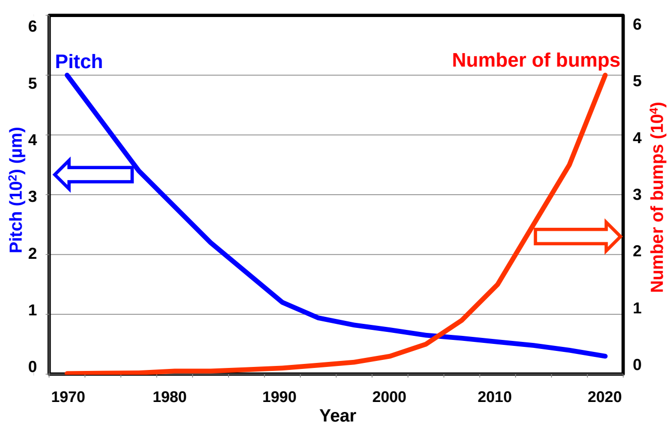

Figure 20 - Trend in flip chip bump and pitch

Summary and Recommendations

Wafer bumping, package substrate, assembly, and underfill for flip-chip technology have been investigated in this study. Some important results and recommendations are as follows:

- Flip chip technology came from a long way. From the three-bump flip chip to 10,000-bump flip chip, and could be 50,000-bump flip chip by the year of 2020. Also, by that time, the flip-chip pitch could be as small as 30µm as shown in Figure 20.
- C2 bumps have better thermal and electrical performance and can go down to finer pitch (smaller spacing between pads) than C4 bumps.
- The self-alignment characteristic (one of the most unique features of flip chip technology) of the C2 bumps is nowhere near the C4 bumps. Thus, mass reflow is usually applied to C4 bumped chips.
- C2 bumped chips are usually assembled by TCB with high-force, while low-force is sometime used.
- The advantages of TCB are for higher pin-count, finer pitch, thinner chips, higher-density, and thinner package substrates, and controlling warpage and die tilt. One of the drawbacks of TCB is throughput (compared with mass reflow).
- A package substrate with ten build-up layer (5-2-5) and 10µm linewidth and spacing is more than adequate to support most of the flip chips. In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced FPGA, even a 12 build-up layer (6-2-6) package substrate is not enough to support the chips and a TSV interposer is needed.
- As of today, TSV-interposer is very expensive. In order to lower the cost, enhance the electrical performance, and reduce the package profile, TSV-less interposers such as the Xilinx/SPIL's SLIT, Amkor's SLIM, SPIL/Xilinx's NTI, Intel's EMIB, and Cisco/eSilicon's organic interposer have been developed. This will be the trend in package substrate for high-density and performance flip chip applications.
- More research and development works should be done on innovative and low-cost ETS and coreless substrates for portable, mobile, wearable, and IoTs applications. More research and development works should be done to effectively use the BOL technique to increase routing density, and thus, lower the cost and reduce the size of organic package substrate.
- For the post-assembly underfill approach, the CUF or MUF is usually applied to flip-chip assemblies with mass reflow and TCB with low-bonding force methods.
- For the pre-assembly underfill approach, the NUF, NCP, or NCF is usually applied before flip-chip assemblies; NUF is with mass reflow and NCP or NCF is with high-force TCB. In general, the NUF and NCP are applied on the substrate and the NCF is laminated onto the C2 bumped wafer and then diced into individual chips.
- Toray's collective TCB with high-force method can be a potential high-throughput process for stacking C2 chips with laminated NCF.

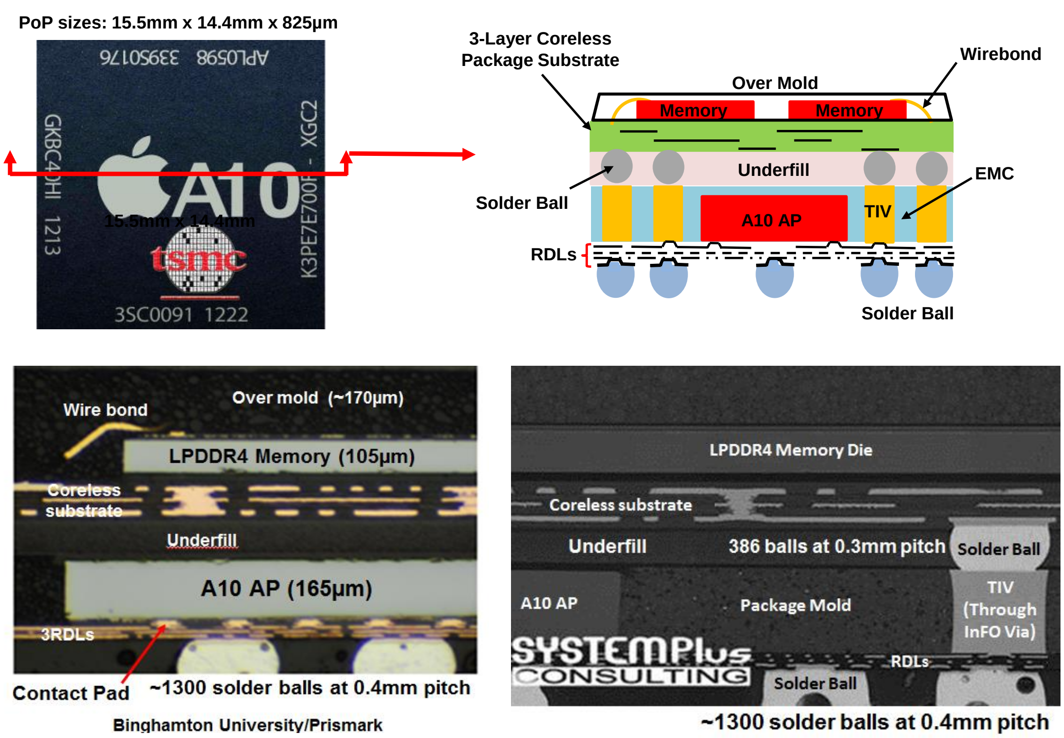

Figure 21 - PoP in Apple's iPhone 7/7+. In the bottom package, the A10 AP is embedded in the EMC and its circuitry is fanned out through the RDLs to the PCB

- Flip chip technology is facing stiff competition. Some of its market share will be taken away by the fan-out wafer/panel-level packaging (FOW/PLP or simply FOWLP) technology [60, 61, 62]. Figure 21 shows the schematic and SEM (scanning electron microscope) images of the cross section of the PoP which houses the Apple A10 AP and mobile DRAMs of the iPhone 7/7+. This PoP is fabricated by TSMC with their InFO (integrated fan-out) WLP technology [62]. It can be seen from the bottom package that the wafer bumping, fluxing, flip chip assembly, cleaning, underfill dispensing and curing, and build-up package substrate (of the A9 AP shown in Figure 15) have been eliminated and are replaced by the EMC and RDLs (for the A10 AP as shown in Figure 21). This results into a lower cost, higher performance, and lower profile package. This is very significant, since Apple and TSMC are the "sheep leaders". Once they used it, then many others will follow. Also, this means that FOWLP is not just only for packaging baseband, RF (radio frequency) switch/transceiver, PMIC (power management integrated circuit), audio codec, MCU (micro control unit), RF radar, connectivity ICs, etc., it can also be used for packaging high-performance and large (>120mm^2) SoC such as APs.
- With the popularity of SiP, fan-out (which can handle multiple dies and discrete component) will be used more because the flip-chip WLCSP (wafer-level chip scale package) can only handle single die.

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