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SOLDER JOINT RELIABILITY ANALYSIS AND TESTING OF A DUAL ROW QFN PACKAGE

Luke England and Yong Liu
Fairchild Semiconductor
South Portland, ME, USA
luke.england@fairchildsemi.com, yong.liu@fairchildsemi.com

Richard Qian[1] and Ji-Hwan Kim[2]
Fairchild Semiconductor
Suzhou, China[1] and Bucheon, Korea[2]
richard.qian@fairchildsemi.com, jihwan.kim@fairchildsemi.com

ABSTRACT
QFN packages have become mainstream designs for mobile applications. As more applications adopt the QFN style packages, I/O count requirements are increasing. The typical method for increasing pin count in a QFN package is to increase the body size to accommodate the additional lead fingers. This is undesirable though, as mobile device users are pushing for smaller package sizes. By using a dual row design, more lead fingers can be added in the same overall body size. This increases the overall performance to package size ratio.

Previous studies published on dual row QFN packages focus mainly on design considerations for manufacturing. [1-3] Since the current design uses standard lead frame processing techniques, no additional processing strategies are needed compared to single row QFN production.

This study focused on the board level solder joint reliability of a 28 lead dual row QFN package. Prior to manufacturing, a mechanical modeling DOE was performed for various dual row QFN footprints to estimate the solder joint lifetime through temperature cycle testing. The modeling was followed by prototype manufacturing of daisy chain units. The daisy chain devices were subjected to temperature cycle testing according to JEDEC specifications. Testing was continued until the complete lifetime estimation curve could be obtained. It was determined that a dual row design can actually improve solder joint reliability performance when compared to a single row design of similar body size. Since there are no lead fingers in the immediate corners of the package for the dual row design, which is typically the highest stress area of the package during testing, the overall solder joint lifetime can be increased. Although the typical failed lead fingers on the dual row package were still the farthest distance away from the package center, these lead fingers are not located in the package corners. Final results show that the dual row QFN package has good performance through temperature cycle testing, with a performance increase over standard single row QFN packages.

Key words: QFN, dual row, mechanical modeling, thermal cycle

INTRODUCTION

As mobile electronic devices become smaller, the shrinking of packages for these devices is a necessity. QFN style package have become mainstream technology in mobile applications throughout the industry. Their leadframe based technology makes them ideal for ease of manufacturing at a low cost, and also provide excellent thermal performance for high power devices. As I/O counts increase, many suppliers are moving toward substrate based packages such as BGA to avoid increasing the package area while increasing the number of interconnects. These package types are higher cost, however, due to the more expensive substrates.

Dual row QFN designs help to bridge the gap between conventional single row QFN packages and BGA style packages. They enable a higher I/O count per area of single row QFN packages, and they also maintain similar costing due to the leadframe based technology. This makes them attractive over substrate based packages in many cases.

Within the dual row QFN family, there are multiple options for design. The inner row of leadfingers must be supported during manufacturing using tie bars that can be connected to the center die attach pad (DAP), if available, or to the same connecting bar that the outer row of leadfingers is attached to. [2] The later is preferred because connecting the inner row of leadfingers to the DAP requires an extra sawing process to electrically separate the leadfingers from the DAP. Connecting the inner row of leadfingers to the same connecting bar as the outer row allows all leadfingers to become electrically isolated during one saw pass.

The option also exists for inline or staggered row configurations, which can both be used in either leadfinger tie bar connection method described previously. The staggered dual row configuration does have some advantages over the inline configuration, however. For one, a larger number of leadfingers can be designed into a

package of a specific x-y size. During solder paste printing for surface mounting of the devices, the staggered row configuration minimizes the chance for solder bridging since the closest points between two inter row pads is a corner rather than an entire side.

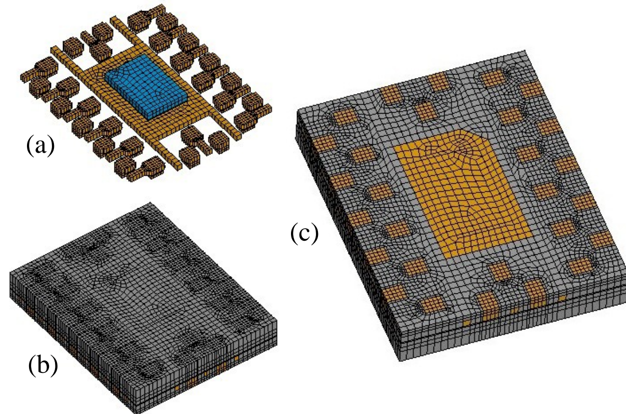


Figure 1: Drawings showing the design and finite element model of the staggered dual row package. (a) Leadframe (b) Top Package Surface (c) Bottom Package

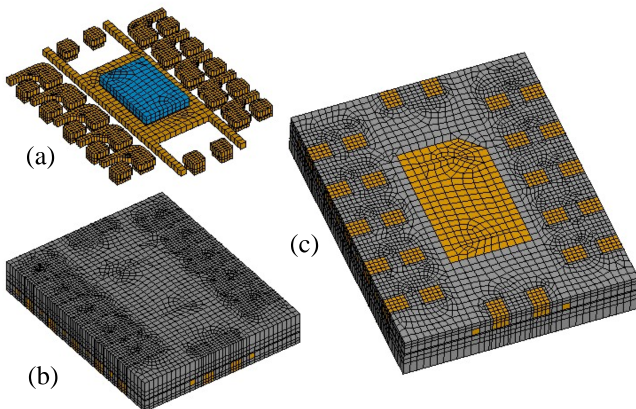


Figure 2: Drawings showing the design and finite element model of the inline dual row package. (a) Leadframe (b) Top Package Surface (c) Bottom Package

This study focused on the board level thermal cycle reliability of a 28L dual row QFN package. Specific package size requirements for a particular application were given, and both inline and staggered configurations were initially compared through designs and modeling activities. After the ideal configuration was selected, leadframes were procured, and daisy chain devices were created for board level thermal cycle testing. The final thermal cycle results were then compared to the mechanical modeling results for accuracy.

EXPERIMENTAL

Package Design

A target package size of 2.9x3.6mm with a 0.55mm thickness was given for a particular application. The goal was to fit as many I/O's into this package size as possible. Inline and staggered dual row configurations were designed using minimum leadframe design rules and dimensions. No JEDEC outline was followed (i.e. MO-267). Designs for each are shown in Figure 1 and 2. It can be seen that the staggered row design has 28 leads, but the inline configuration only allowed for 26 leads. This is essentially because the staggered design can have a smaller between row pitch than the inline design due to leadframe metal-to-metal feature and half etch design rules. The major features of the final package design are listed in Table 1.

Table 1: Dual row QFN package design features.

Design Feature	Value
Package Size	2.9x3.6mm
Package Thickness	0.55mm Max
Leadframe Thickness	6mil (Cu)
Lead Count	28
Lead Size	0.2x0.25mm
Within Row Pitch	0.60mm
Between Row Pitch	0.375mm
DAP Size	1.14x1.84mm

Mechanical Modeling

Finite element models were constructed initially to predict the best performing leadframe configuration. A three-dimensional non-linear finite element model was developed in ANSYS® for the numerical simulations. The finite element models used for the staggered and inline designs are shown in Figures 1 and 2. In order to simplify the calculations, wire bonding was ignored in the modeling. Solder was assumed to be SAC405 since accurate modeling parameters for this alloy were previously obtained. [4]

The thermal cycle testing board contained 32 packages mounted to a single board. The board is inserted into a socket for electrical resistance monitoring. Figure 3a shows the overall board layout for thermal cycle testing. To simplify calculations only one package and the board area immediately surrounding it were used in the modeling, which is illustrated in Figure 3b. Details of the test board design are further discussed in the following section.

Figure 4 shows the finite element model of the package and the portion of the thermal cycle testing board that was used in modeling. For the calculations, the two surfaces of the thermal cycle testing board were set to be symmetrical planes. Anand's constitutive model was used and the material properties were described as viscoplastic elements. The Anand constants of SAC405 solder that were used for modeling are listed in Table 2. For the calculations, the thermal load is considered to be uniform. Temperature is applied to all elements of the model (package, solder, and test board). The temperature range for modeling was -40C-

125°C with conditions that match those described in the following section.

In addition to stress modeling, the first failure and characteristic lifetime were also modeled using previous known numerical methods. [5]

Initial modeling was performed using a single layer element in the solder in order to reduce calculation time. This method was sufficient for a general comparison of the design configurations in order to predict the best performer. Following completion of thermal cycle testing, however, it was found that the modeling results did not agree well with the experimentally determine values. The model was subsequently adjusted to include five layer elements in the solder, which helped to improve the accuracy of the modeling results.

Daisy Chain Testing

Daisy chain packages were assembled using the final leadframe design. In order to form the continuous electrical path for resistance monitoring, leadfingers were wire bonded together as shown in Figure 5. The corresponding lands were connected in the test PCB.

The PCB test board design followed the IPC-9701 standard. It was a single board containing 32 test sites, and the overall board layout is shown in Figure 3a. The board contained 8 total layers (1+6+1), and was fabricated using standard build-up technology. Solder mask was NSMD

Table 2: Experimentally determined fitted Anand model constants for SAC405 solder alloy. [4]

Description	Symbol	Constant
Initial value of s	s_o	20 MPa
Activation energy	Q/R	10561 K
Pre-exponential factor	A	325/s
Stress multiplier	ζ	10
Strain rate sensitivity of stress	m	0.32
Hardening coefficient	h_o	8.0E5 MPa
Coefficient for deformation resistance saturation value	$\hat{s}$	42.1 MPa
Strain rate sensitivity of saturation value	n	0.02
Strain rate sensitivity of hardening coefficient	a	2.57

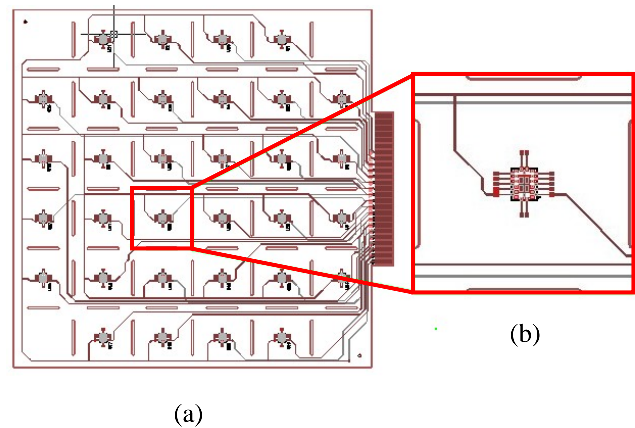


Figure 3: (a) Thermal cycle testing board drawing. (b) Part of thermal cycling board in modeling.

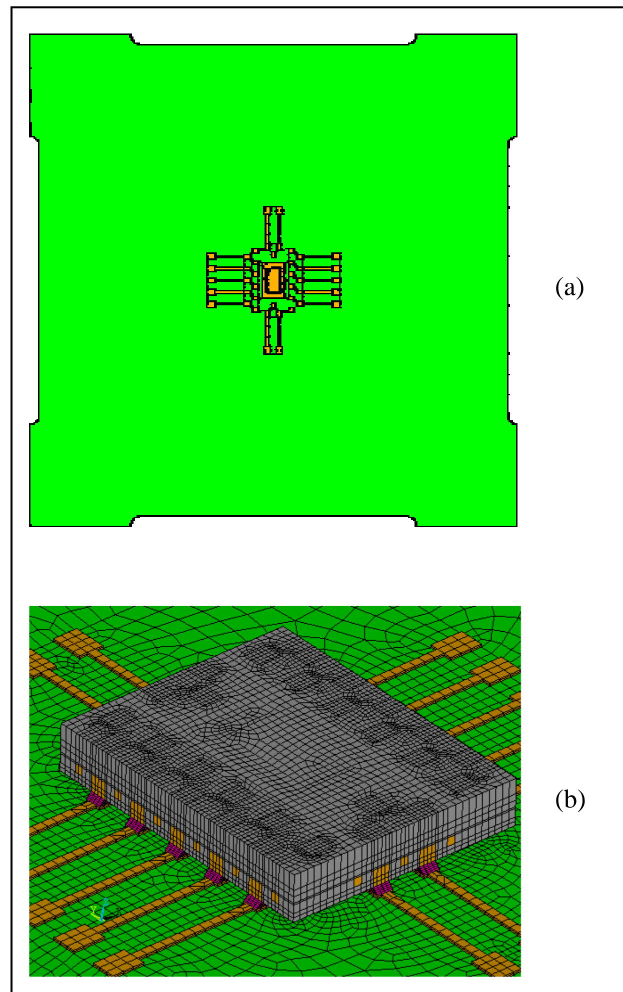


Figure 4: (a) Board model used for thermal cycle testing. (b) Finite element model of package mounted to test board. Although these show the inline design specifically, they are representative of the staggered design as well.

with Via-in-Pad land pads. Surface mounting also followed the IPC-9701 standard, and was done using stencil printing with SAC305 paste and component placement. Reflow was performed in a nitrogen atmosphere. There was some difficulty in getting good solder paste release out of the small apertures, but using a 2mil thick stencil minimized the issue. A 2mil thick stencil is not ideal for manufacturing, but time constraints prevented in depth surface mount studies using a more conventional 4mil thick stencil.

Thermal cycle testing was done according to IPC-9701 condition TC3. The temperature cycle range was from -40-125°C. Two cycles per hour were performed, and a 10min dwell time was used at each peak. Daisy chain resistance was continuously monitored using an event detector, and a fail was recorded if the resistance exceeded the set threshold of 1000Ω. Final data analyzed and a Weibull plot was generated using the two-parameter distribution function shown in the following equation:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right]$$

where *F(t)* is the cumulative density function, η is the scale parameter or characteristic lifetime, and β is the shape parameter or slope. [6]

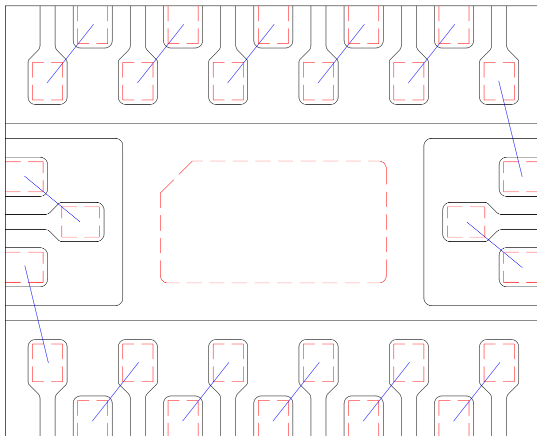
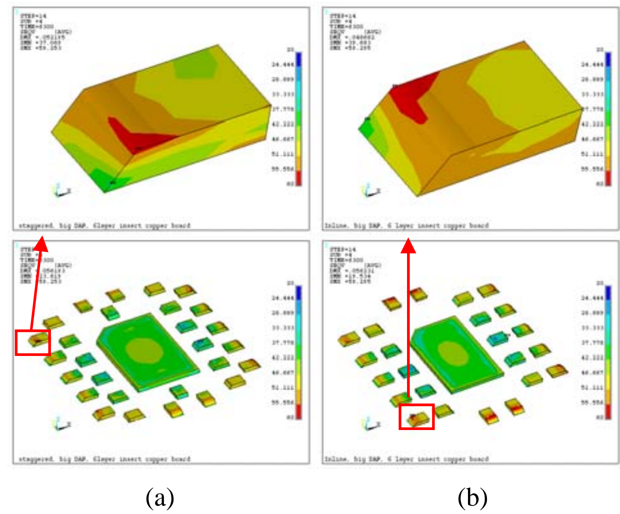


Figure 5: Package sketch showing the wire bond scheme for the daisy chain packages. The leadfingers were bonded together, and corresponding land pads on the PCB were connected to form the electrical resistance loop. A dummy die was present in the package for testing, but no wire bonds were made to it.

RESULTS AND DISCUSSION

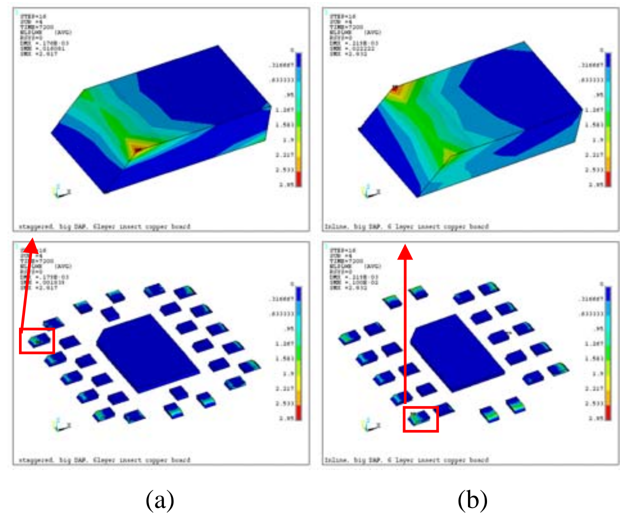
Modeling

Figure 6 shows the max Von-Mises stress and Figure 7 shows the viscoplastic energy density after the fourth temperature cycle. It can be seen that both the max Von-



(a) (b)

Figure 6: Resulting maximum Von-Mises stress of the solder joints. (a) Staggered: 59.25MPa (b) Inline: 59.3MPa



(a) (b)

Figure 7: Resulting maximum viscoplastic strain energy density of the solder joints. (a) Staggered = 2.82MPa (b) Inline = 2.83MPa

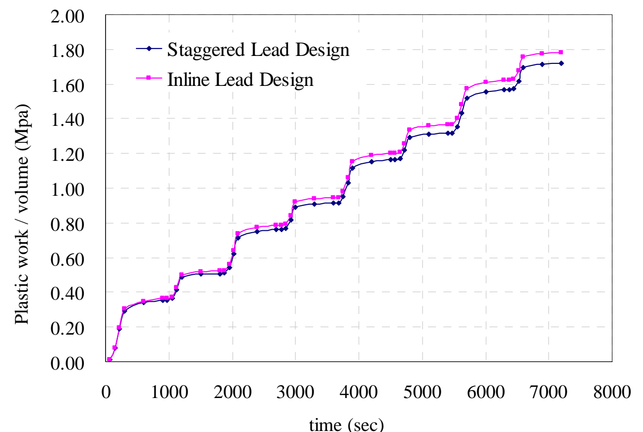


Figure 8: Plot showing a comparison of the viscoplastic strain energy densities for the staggered and inline designs.

Mises stress and viscoplastic strain energy density of the inline design are slightly higher than those of the staggered design. Within the solder joint, both the max Von-Mises stress and viscoplastic strain energy density are located at the point where the solder paste connects to the package leadfinger. This predicts that the failing solder crack during testing will appear near this interface. Figure 8 shows the viscoplastic strain energy density comparison through the first four temperature cycles. It can be seen that the viscoplastic strain energy density is rising at a greater rate for the inline design, which indicates that the staggered design is more robust through thermal cycling.

Once it was determined that the staggered configuration was the optimum configuration, the overall effects of the test board structure were also modeled. Two different board types were investigated. Table 3 shows the conditions of each group along with the results, while Figure 9 shows a cross sectional view of the model with and without the center Cu layers in the board.

Figure 10 shows the resulting maximum Von-Mises stresses and viscoplastic energy density for each group tested. A definite dependence upon internal Cu layer content can be seen in the Von-Mises stress and predicted lifetime values. The modeling results show that the better performance can be gained by using a board with the least amount of Cu layers possible. The plot of viscoplastic energy density for each group illustrates this. The reason is because the board will then be less stiff overall, which will result in less stress applied to the solder joints due to the material's CTE mismatch. Although this configuration was shown to be the best case, our actual thermal cycle testing was done using the board with multiple layers of Cu. The reason is that this follows the IPC-9701 specification for test board design. By testing this configuration, the worst case is essentially being verified.

Table 3: Modeling group details and their corresponding lifetime predictions. 2-Cu layer boards have only front and backside Cu layers, while 8-Cu layer boards contain 6 internal Cu layers (1+6+1 Configuration). Group B matches the experimental board design.

Group	Board Thickness	# of Cu Layers	Predicted First Failure	Character Cycle Failure
A	2.35mm	2	7,232	11,761
B*	2.35mm	8	6,016	9,784

Thermal Cycle Testing

Based on the modeling results described in the previous section, board level thermal cycle testing was performed on the staggered dual row configuration only. The package proved to be very robust as testing was stopped at 9,528 cycles with only a 53% failure rate.

The thermal cycle Weibull plot is shown in Figure 12 along with the two sided confidence bounds at a 90% confidence

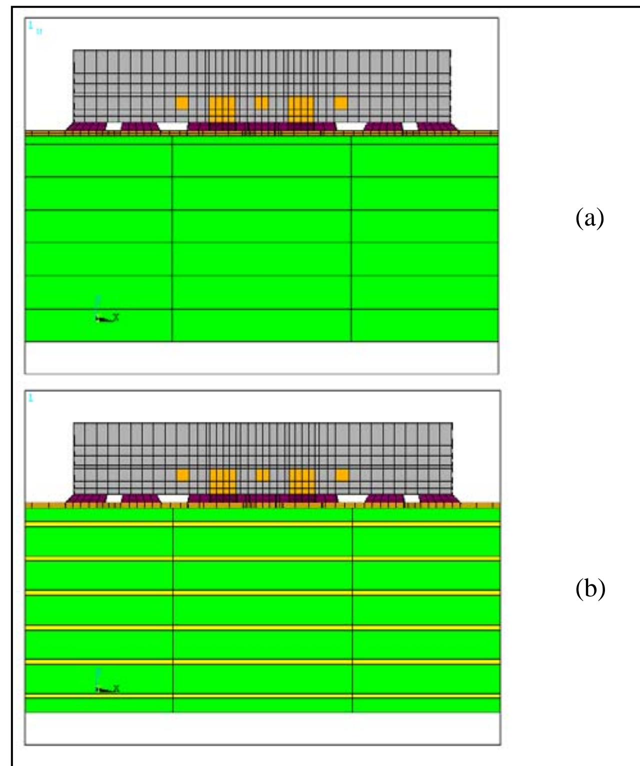


Figure 9: Cross section drawing of package/board model (a) without and (b) with center Cu layers.

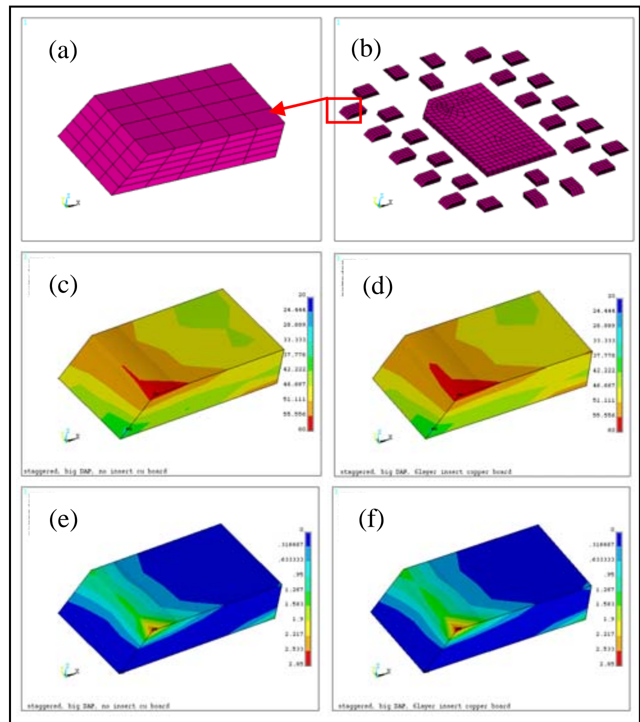


Figure 10: Resulting maximum Von-Mises stress and viscoplastic strain energy density for the two modeling conditions. (a-b) Location of results (c) Group A: 58.87MPa (d) Group B: 59.25MPa (e) Group A: 2.64MPa (f) Group B: 2.82MPa.

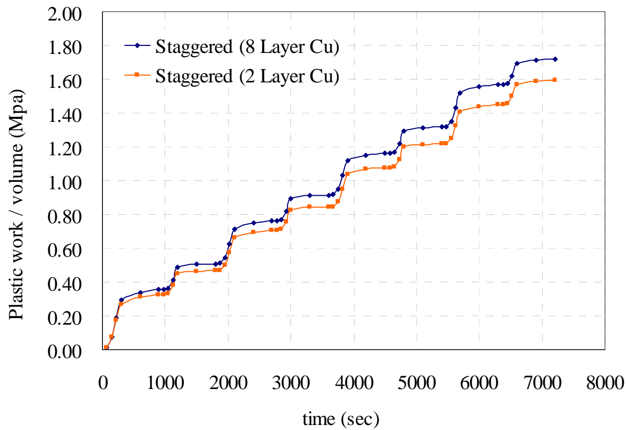


Figure 11: Plot showing a comparison of the viscoplastic strain energy densities for each test group listed in Table 3.

level. The failures can be grouped into two categories – failures less than 3,500 cycles and failures greater than 6,000 cycles. It is suspected that the early failures (< 3,500 cycles) are the result of the surface mounting issues that were encountered during board assembly, which are described further in Experimental section. When looking at the failures over 6,000 cycles a very tight Weibull distribution can be seen. This plot is shown in Figure 13. This suggests a first failure at approximately 5,500 cycles when consistent surface mounting can be achieved, with a 50% failure rate of almost 10,000 cycles. This data matches our modeling results very well (see Table 3). Since there is such good matching between modeling and experimental data, it supports the suspicion that the early failures were the result of surface mounting problems. Although the early failures appear to be in a separate grouping, they are still occurring after enough thermal cycles for sufficient reliability in mobile applications, which is the main target of this package type.

Failure analysis was performed on select daisy chain packages. Cross sections of Pin #26 and Pin #28 of the device that failed at 8,311 cycles are shown in Figure 14, along with a diagram showing the plane of cross sectioning. These pins are located in the package end position, which is one of the points of highest stress due to the large distance from the package centroid. Based on this it was expected that these pins would be the first to fail.

Unfortunately the board design contained all of the test samples, so failures were unable to be pulled for analysis immediately after an event was detected. Many of the devices, especially the early failures, saw extra thermal cycles after failure occurred. For instance, the first failure at 665 cycles was stressed all the way through 9,528 cycles when testing ended. This made it difficult to determine the root cause of failure. Based on this experience, it is recommended that multiple boards be used with fewer package sites per board to enable more accurate failure analysis.

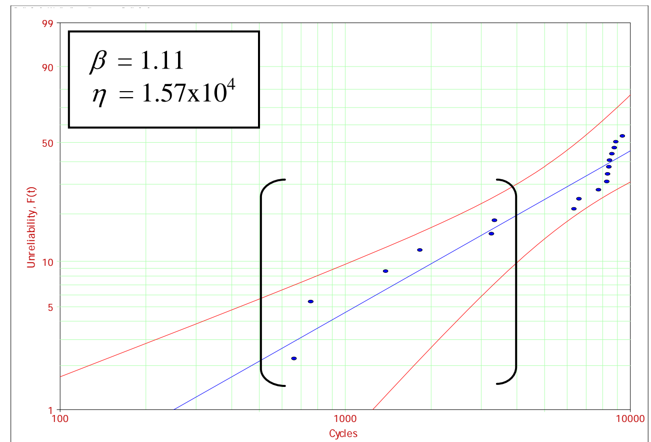


Figure 12: Weibull plot showing all thermal cycle failures. Early failures before 3,500 cycles (shown in brackets) are most likely surface mount related, coming from the difficulties encountered during board assembly. The 95% confidence bounds indicate marginal lifetime prediction.

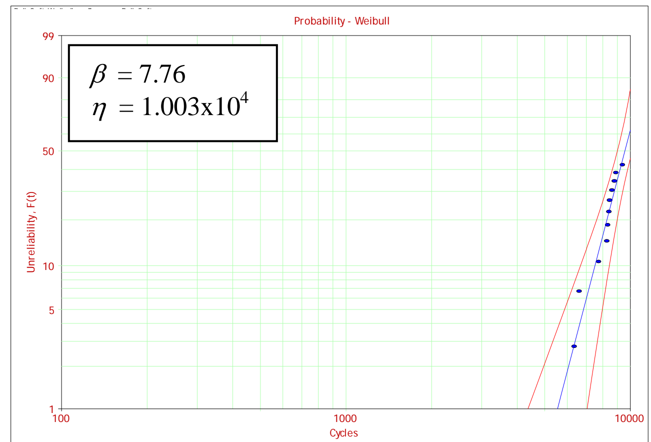


Figure 13a: Weibull plot showing failures over 6,000 cycles. The 95% confidence bounds are tight around the best fit line, which indicates very good lifetime prediction. Scale is the same as shown in Figure 12.

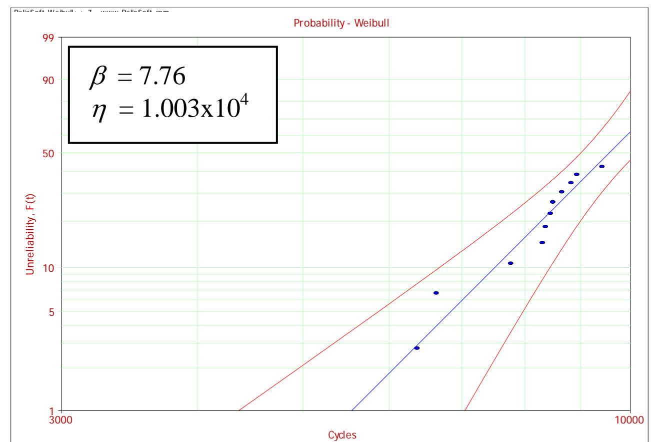


Figure 13b: Weibull plot repeating results of 13a, but at a higher scale (3,000-10,000 cycles) for better data viewing.

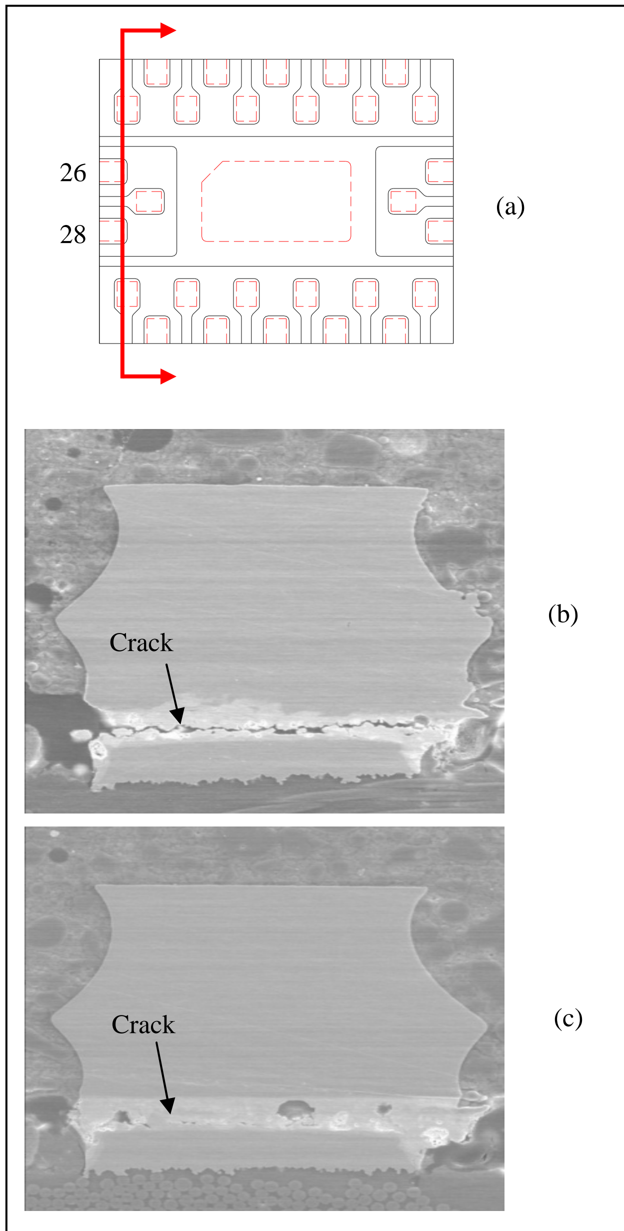


Figure 14: (a) Diagram showing cross section plane for failure analysis. (b) Pin 26 cross section. (c) Pin 28 cross section. Failure mode is solder cracking.

CONCLUSIONS

Mechanical modeling of two dual row QFN design configurations (staggered and inline) for a given x-y package size was performed. The staggered configuration was predicted to have better thermal cycle performance for two main reasons:

- The staggered configuration simply has more pins/leadfingers within the given package size.
- The inline configuration has only two leadfingers on each end, while the staggered configuration has three leadfingers on each end.

Both of these design differences help the staggered configuration to better resist the stresses applied during thermal cycling due to material CTE mismatches.

Leadframes were designed in the staggered configuration, and daisy chain packages were assembled for thermal cycle testing. The results revealed a very robust package, and testing was stopped after just over 9,500 cycles with only a 53% failure rate. Failures appear to be segregated into two groups. It is suspected, but not proven, that the group of early failures is stemming from the surface mounting issues encountered during test board assembly.

Initial modeling predictions did not provide a good match to the experimental data. Subsequent adjustments to the calculations greatly improved the predictions, and resulted in a good correlation between modeling and experimental data. For instance, initial modeling only utilized one layer element through the solder joint, and increasing to five layer elements provided more accurate calculations. In addition, the material properties used in the model greatly affect the outcome; therefore, it is critical to have accurate material property inputs in order to achieve good results.

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