SIR AND ECM TESTING OF SOLDERING MATERIALS
VS. SOLDERING PROCESSES

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ABSTRACT
Manufacturers of soldering materials have been asked by electronics device manufacturers and contract electronics
PWB assemblers for Surface Insulation Resistance (SIR) data of solder pastes and other soldering materials on IPC-
B-52 coupons. IPC-B-52 coupons were designed for evaluating the electrochemical reliability of the whole
soldering process, not just the materials, used by PWB
assemblers. The bare coupons should made by the same
board fabricator using the same materials and processes as
the boards used by the PWB assemblers. Additionally, the
test coupons should be assembled and soldered by the PWB
assemblers themselves. Having a soldering material
manufacturer or a commercial test laboratory assemble and
solder the coupons using an IPC-B-52 kit will not provide the
complete benefit of evaluating the whole soldering process,
i.e. all the materials and processes used by the
manufacturers. The completely assembled and soldered
coupons may then be tested for SIR to a standard test
method, such as IPC TM 650 Method 2.6.3.7., by the
assembler, a commercial laboratory or the material
manufacturer.

The present SIR and ElectroChemical Migration (ECM)
testing methods for soldering materials do not address the
electrochemical failure mechanism concerns of flux residues
trapped under component and the ever shrinking spacing
between solder joints. However, requiring the use of complex and expensive IPC-B-52 coupons for material
evaluation is a poor solution for this issue. New test
vehicles for soldering materials that include occluded flux
residue and tighter board spacing are needed.

INTRODUCTION
Some electronics original equipment manufacturers
(OEM’s) and contact manufacturers (CM’s) have asked
electronics materials suppliers to provide SIR data for
materials, such as solder paste and wave soldering flux, on
populated IPC-B-52 coupons. The IPC-B-52 was developed
to evaluate the electrochemical reliability of electronics
assembly processes [1,2], including:
- Bare board fabrication
- Soldering processes
  - Solder paste printing and reflow
  - Selective fountain and wave soldering
  - Rework hand soldering
- Cleaning processes
- Conformal coating

A materials manufacturer will likely purchase an IPC-B-52
kit, including test board and dummy components from one
of several test vehicle distributors. The test vehicles in these
kits are likely to be very clean and may not be representative
of the bare boards used by a particular electronics
assembler. If a materials supplier assembles IPC-B-52
coupons, care will be given to ensure minimal
contamination during assembly, and soldering conditions
may be chosen to give higher SIR values. The test vehicles
may even be pre-cleaned before assembly. Again, such
assembly in a material manufacturer’s laboratory will likely
not be representative of actual processes used in an
electronics assembly plant.

Finally, this can be an imposition for smaller materials
vendors that may have limited assembly and SIR testing
capability and can’t accommodate testing on multiple
patterns, up to thirteen channels, on ten coupons for this
type of evaluation. Larger materials suppliers may be
willing to test already assembled IPC-B-52 coupons to
accommodate a large customer, but question the wisdom of
assembling these test vehicles at their laboratory, as this
partly defeats the purpose of validating a new material,
process set up or piece of assembly equipment using this
coupon.

Unfortunately, SIR test vehicles, such as the IPC-B-24
coupon [3,4] and the IPC-B-25A [4,5] have not kept up with
the challenges of modern electronics assembly. Spacing
between leads on components is getting smaller with time,
and 0.5mm gaps are not tight enough to represent typical
hand held electronic devices. Many newer component
packages have signal or power connections close to large
ground connections, such as quad flat no-leads (QFN’s), see
Figure 1., or complex land grid array (LGA’s), see Figure
2. These large ground connections are needed to remove
heat produced by the component. These components also
have very small clearances between the bottom of the
component and the circuit board. In addition, a relatively
large amount of solder paste is needed to solder a large
ground connection to the circuit board, resulting in a lot of
flux residue being trapped between the central ground plane
and surrounding signal and power connections. This makes
a good environment for electrochemical migration and
dendrite growth, particularly in harsh service environments.
HOW TO ASSEMBLE IPC-B-52 COUPONS

Guidance on using the IPC-B-52 coupon for process evaluation is available in IPC 9202, Material and Process Characterization/Qualification Test Protocol for Assessing Electrochemical Performance, and IPC 9203, Users Guide to IPC-9202 and the IPC-B-52 Standard Test Vehicle. These are comprehensive documents compiled by several experts in using SIR and ECM testing to evaluate electronic assembly electrochemical reliability. Some brief and general guidance will be provided in this paper.

Use Your Own Circuit Board Fabricator

Off the shelf IPC-B-52 coupons are available from some vendors, but they may not represent actual unprocessed circuit boards from a particular fabricator. If there is a problem with the board fabricator, it is better to determine this during process evaluation than having field failures during service. The Gerber files for this test vehicle are available from IPC. If desired, the test vehicle design can be modified to include a problematic component specific to a particular assembly. If the assembly in question has a big QFN, include a similar dummy on the test vehicle.

The materials used by a fabricator can affect SIR values and the whether ECM is likely occur. These include:
- Laminate and prepeg,
- Copper foil,
- Solder mask,
- Metal finish

Certain metal finishes are more problematic than others; a poorly cleaned hot air solder leveled (HASL) surface will give poorer SIR than typical electroless nickel gold (ENIG) finishes. Solder masks may not be fully cured during board fabrication, this may allow various chemical to be absorbed into the mask and slowly released during SIR testing, or even in actual service in harsh environments.

Cleaning the circuit board between various processes can also be an issue with board quality. Etching chemicals need to be aggressive to remove the copper from the laminate, it's important to sufficiently clean the board before applying the solder mask. Boards should also be properly cleaned after any application of metal finishes.

Using the fabricator that makes an assembly plant’s bare boards with the materials usually specified will help determine whether the fabricator’s materials and processes are compatible with the soldering, cleaning and coating materials and processes used during circuit assembly.

Finally, use the test vehicles just as they come from the fabricator, don’t clean them. Incoming boards are not pre-cleaned before assembly.

Assemble the Coupons In Your Assembly Plant

Circuit board assembly operators never eat salty chips during a break and then forget to wash their hands or wear gloves. They never use unauthorized hand lotions. The water-washable touch-up flux in the squirt bottle is never used on no-clean assemblies because it makes the solder flow really well. It’s better to find out during process evaluation than before field failures occur.

Even if a plant’s operators are well trained and monitored, materials may not be compatible with each other or a reflow profile may not be optimized for a particular solder paste. A cleaning process may not be effective enough when a particular solder paste is used. Perhaps too much liquid flux is applied during selective soldering. A RTV silicone or poly urethane conformal coating may not work well with a certain solder paste. New equipment may also affect the assembly process. Process evaluation is when to determine whether these problems exist.

SIR Testing

If you have the ability and equipment, you may test the coupons yourself. Otherwise, there are many capable test laboratories that can perform this testing. Sometimes, solder paste or cleaning chemical suppliers will test the coupons for their most valuable customers. As long as the testing is done properly, it doesn’t matter who tests them.
Usually, IPC-B-52 coupons are tested to IPC-TM-650 Method 2.6.3.7., but another test method might be better for a particular circuit board’s application. It’s best to know what test is wanted before approaching a commercial test laboratory or a soldering material supplier. If a circuit is used at high temperatures, an SIR test at 85°C / 85% R.H. may be more appropriate.

**BETTER SIR COUPONS AND TEST CONDITIONS FOR MATERIAL EVALUATION**

**Conductor Spacing**
As discussed before, the IPC-B-24 and IPC-B-25A coupons do not address current and future spacing between connector pads. The effects of conductor spacing and electrical field was studied extensively in the past [6] by a European consortium. A pattern with traces 0.4 mm wide with 0.2 mm spacing was recommended to be more representative of actual electronic assemblies and better for finding issues with electrochemical migration. The wider traces facilitate printing and reflowing solder paste without shorting the comb pattern. Using relatively low field strength was also recommended.

What would be a small enough spacing for SIR qualification/classification of soldering materials, 0.2 mm, 0.15 mm? If the number of squares in the patterns is maintained at 1000, the pass/fail criteria of 100 Mohms can be kept. Wider conductors will facilitate hand printing of solder paste without bridging conductors. What about wave and selective soldering? It’s already difficult to wave-solder the current IPC-B-24 comb pattern without solder bridges, finer spaces between conductors will be more difficult. Wave soldering isn’t used for soldering closely space conductors.

**Trapped Flux Residue**
As the IPC-B-24 and IPC-B-25A test vehicles have uncovered comb patterns, they also don’t address the issue of occluded solder paste flux residue. The flux trapped under the component may absorb moisture from the air if it is hygroscopic enough and allow low SIR and electrochemical migration. With no applied bias, the formation of semi-conductive oxides at 85°C and 85% RH. is possible and can greatly reduced the insulation resistance under QFP’s [5], see Figure 3 for X-ray pictures of tin oxides formed under QFN packages.

At high temperatures, tin electrochemical migration between signal or power to ground has occurred for some unusual LGA’s at low humidity. This failure was reproduce by reflowing solder paste flux on SAC305 pre-soldered IPC-B-24 coupons covered with glass slides, then exposing the coupon to 105°C and 6V bias for 15 hours, see Figure 4.

Glass slides have been used before to approximate conditions under QFN’s, LGA’s and RF shields [8]. However, it’s uncertain whether glass slide covered comb patterns are a representative of conditions under QFN packages.

**Temperature and Humidity**
Finally, what are the best test conditions to exacerbate low SIR and ECM? Twenty years ago, it was discovered that low solids, organic acid activated liquid fluxes were more likely to fail ECM and SIR tests at lower temperatures than 85°C 85% R.H. conditions used at the time. This is because the organic acids volatilize faster at higher temperatures, and leave little hygroscopic residue to low SIR after a day or two at 85. For this reason, ECM testing is generally conducted at 65°C and SIR testing is done at 40°C. However, some experimental core solder fluxes and solder pastes have passed the currently specified IPC TM 650 Method 2.6.3.7 test at 40°C / 90% R.H., but have failed SIR testing at the previously specified Method 2.6.3.3 at 85°C / 85% R.H. For example, an experimental core flux passed the present 40°C / 90% R.H. test with all measured SIR...
values greater than 1 Gohm, but had values less than 30 Mohm when tested at 85°C / 85% R.H.

Should the 40°C / 90% R.H. and the 85°C / 85% R.H. both be required for SIR evaluation of soldering materials? Should a combination condition test similar to Wittmer’s Delphi SIR (40°C/90% R.H. followed by 65°C/90% R.H. followed 85°C/85% R.H.) be developed [10]?

CONCLUSIONS
This paper asks more questions than it answers. However:

- IPC-B-52 coupons were intended for entire electronics process evaluation, and are not appropriate for single soldering materials evaluation.
- SIR test vehicles for soldering materials evaluation need to have smaller conductor spacing than those presently specified.
- An SIR test vehicle needs to be developed that will evaluate the propensity of a material to allow ECM with occluded flux residue.
- SIR and ECM temperature and humidity conditions need to be reexamined as some materials have better SIR and less tendency for ECM at 40°C / 90% R.H. and other materials have better behavior at 85°C / 85% R.H.

REFERENCES
[10] P. Wittmer, unpublished work