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FROM THE SINGLE CHIP TO THE WAFER INTEGRATION

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ABSTRACT

System integration is clearly a driving force for innovation in packaging. The need for miniaturization has led to new System In Package (SiP) architectures, which combine a whole range of different technologies. In addition, due to the increasing complexity of systems, the introduction of new components like MEMS or RF components and the still growing pressure on size, performance and cost; a general trend is to put not one but several dies in a single package. However, cost is the critical issue in SiP Packaging as individual operations are currently necessary to complete each individual package. Taking into account all the developments that have been made to date on Wafer Level Packaging, it has been proposed to establish SiP at wafer level.

Companies that desire an "in-house solution" will prefer WLP because one of the benefits of the wafer level packaging is a simplified supply and value chain. Furthermore, for small companies (not IDM's), one of main consideration is to use generic technologies which can be applied on chips coming from different sources because they have no direct access to wafer manufacturing. To be compatible for chip multi-sourcing one of the most know examples on wafer level packaging is the fan-out wafer level structure This concept, proposed by major companies (Infineon, Freescale, ...), consists of rebuilding a wafer from heterogeneous Known Good Die (ASIC, sensor, memory, optic component etc.).

After having established the current state of the art, the objective of this paper is to identify the various technological concepts and to give a focus on Chip in Wafer in Silicon technology developed at CEA-LETI.

Key words: wafer level packaging, embedded components, rebuilt wafer, 3D integration

INTRODUCTION

Electronics components follow several tendencies related to the economic conjuncture of cost reduction and time to market, on miniaturization (smaller components, level of integration) and to functionality (increase in performances, more functions). To meet this need, a universal technique of packaging doesn't exist; for each product it is necessary to choose an adapted solution which takes account all the specifications. Thus, each technological solution must take into account the form factor, the performances to be reached, the final cost of the component but also the constraints related to the application. Several concepts from packaging coexist and make it possible to answer to integration levels (Figure 1). Each of these concepts presents specific advantages and drawbacks. For example, cost acts as a brake on SiP and further developments are necessary to reduce it.

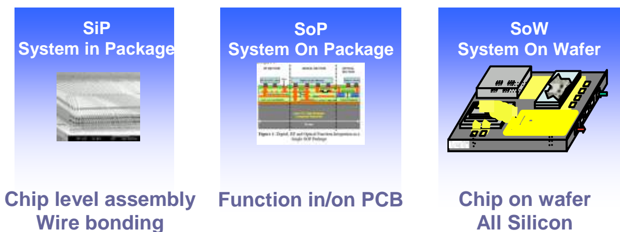


Figure 1. Packaging concepts (source LETI)

Wafer Level Packaging is one on the promising way to decrease cost and improve level of integration.

Among the emergent technological solution, 3D integration is probably one of the most promising way to improve integration level. This concept makes it possible to integrate in the vertical axis the whole of the components to be assembled which allows, for example, to decrease the size of the final assembly and to reduce the length of the interconnections. However, one of the disadvantages to this process is that it is often necessary to carry out vertical intra-connections (TSV) so that the chips can communicate between them. In general, TSV's need to be formed at somepoint before make dicing occurs.

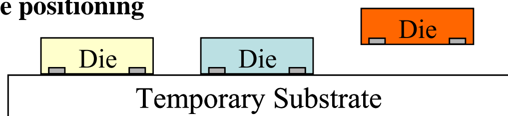
Finally, for small companies (not IDM's), one of main consideration is have access to a limited number of chips or wafers and to use generic technologies which can be applied on individual chips coming from different sources because they have no direct access to wafer manufacturing.

BACKGROUND ON RE BUILT WAFER: FROM THE CHIP TO THE WAFER

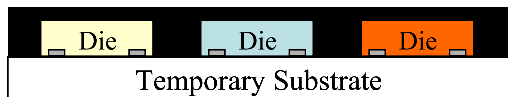
To take into account these previous considerations, one concept which emerged recently is to rebuild a wafer from heterogeneous Know Good Die (KGD). Typically, individual dice are positioned on a temporary substrate with an accurate and high speed handler. These dice are molded in organic substances. After a backside thinning and substrate debonding, a redistributive chip layer is

processed on the side to connect the pads. The main steps of process flow are explained on the next figure 2.

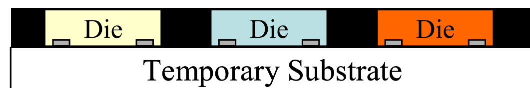
▪ **Die positioning**



▪**Molding**



▪**Back side thinning**



▪**Substrate de-bonding**

Figure 2. Rebuilt wafer process

This concept was introduced by General Electric 20 years ago. In 1994, a first version, called "Neostack", had been proposed by Irvine Sensor where neo-chips for 3D stacking was formed by embedding IC chips in epoxy [1]. In the "Neostack" concept, the KGD was bumped using gold wire bonding. Now, many companies have been developing various versions of the technology.

In 2005, 3DPlus and CEA-LETI [2] in European project (Walpack) showed a new concept based on rebuilt wafers for embedded chips (figure 3) and compatible with stacked module (WDoD).

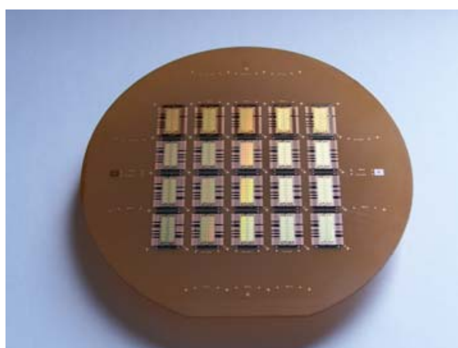


Figure 3. WDoD rebuilt wafer process (source LETI/3Plus)

The RCP (Redistributive Chip Package) has been developed by Freescale [3]. It is based on a bath process that features a build-up and metallization constructed on an embedded die. The application targets are DSP, processors, power management devices, etc…

Infineon proposes a fan out WLP structure with the embedded Wafer Level Ball grid array (eWLB) technology [4] and "Molded Reconfigured 200mm Wafer" [5]. This technology uses a combination of front and back end manufacturing techniques with parallel processing of all the chips on a wafer.

Recently concepts of wafer level technologies form major institutes and companies (EMWLP from ITRI and IME, EM-eSiP from NEPES) using conventional die placement, molding and RDL process has been publishing [6 to 8].

With the SMAFTI concept (SMArt chip connection with Feed Through Interposer) [9], NEC demonstrated in 2006 the feasibility of a new inter-chip connection structure semiconductor package for broadband data transfer and low latency electrical communication.

A NEW CONCEPT

Generally, this process enables coplanar chip active face and Wafer Level Packaging such as pad redistribution, bumping and testing. However the consistency of these rebuilt wafers is limited by the thermal properties of the embedded resin. Processes at temperatures higher than glass transition are hazardous. Wafer deformation is also a critical issue on a rebuilt wafer with polymer. This is due to the excess polymer left by potting or injection on die. A few tens of microns lead to a deformation of several millimeters. Simulation of a 700µm silicon wafer with 50µm of polymer (polymer CTE=20ppm) deposited on it and cured at 200°C leads to a wafer bow of approximately 600µm. To get round this difficulty, we propose to use a silicon wafer as a frame. Known Good Dies are fitted into through cavities and sealed with polymer, this is the CIWIS concept (<u>C</u>hip <u>I</u>n <u>W</u>afer for <u>I</u>ntegrated <u>S</u>ystem) [10] (figure 4)

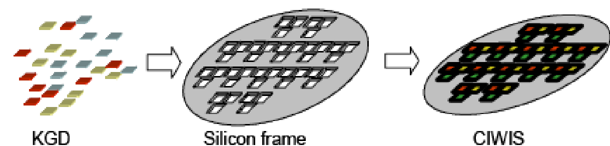


Figure 4. CIWIS concept

The CIWIS technology can be seen as an evolution of that concept : dice are inserted in a silicon or glass frame and polymer is used only to fill the gap between the frame and the dies. This configuration ensures a better mechanical behavior of the rebuilt wafer and allows the realization of higher temperature and higher resolution processes.

The process developed to make such a wafer test vehicle includes:

- ✓ Cavity etching in silicon wafer by laser
- ✓ Silicon wafer bonding on temporary substrate
- ✓ Die placement face down into through cavities
- ✓ Trench filling with polymer

- ✓ Polymer curing
- ✓ Temporary substrate de-bonding
- ✓ Back grinding

The next figure shows CIWIS process flow (figure 5)

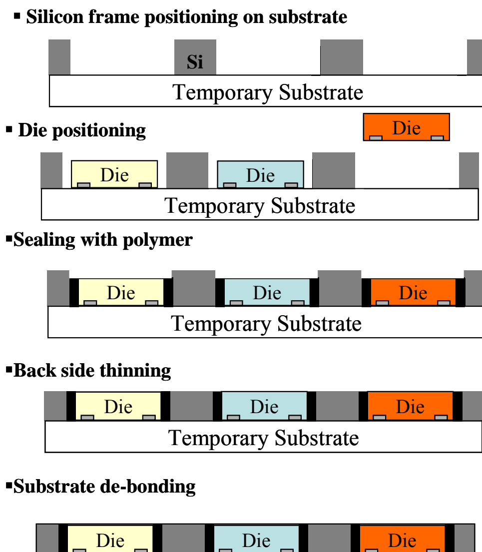


Figure 5. CIWIS process (**C**hip **I**n **W**afer for **I**ntegrated **S**ystem)

In the process, polymer is simply deposited inside the trenches. The test vehicle wafer consists of a 200mm silicon wafer with 82 dies. The die size is 8 x 8 mm², the pitch between dies is 15mm and the sealed cordon is 500µm wide. The figure 6 shows the test vehicle wafer.

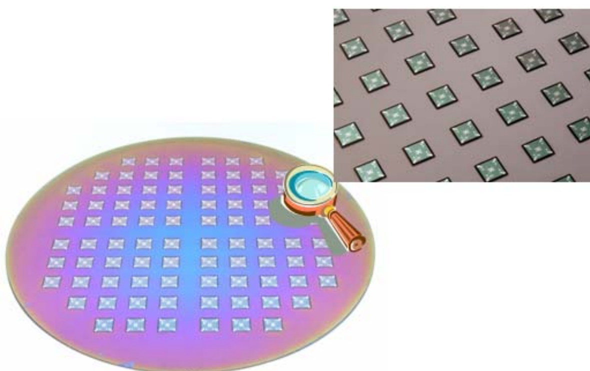


Figure 6. 200mm Ciwis wafer (82 silicon dies)

During trench filling, the wafer and dies are held on the temporary substrate by an adhesive tape. This step is crucial because at the end of the process the placement accuracy of the dies must be compatible with lithography on die pads. To control the relative positioning of the dies after polymer curing, a specific photoresist pattern was made on the wafer by photolithography. Gaps between these photoresist patterns and the die pattern were measured using a microscope. The polymer curing process induces a die displacement of less than 5µm inside the cavity. This value is compliant with pad redistribution of standard ASIC in which pads are 50x50µm².

Bows have been measured on 8 wafers and the average value is 23µm. This value is compared to the 12µm of a blank wafer. Thermal Deformation Measurement was performed to evaluate wafer deformation. The results are presented in the figure 7. It can be noted from this figure that wafer deformation has increased with temperature but is less after heat treatment than before. It is probably due to strength relaxing.

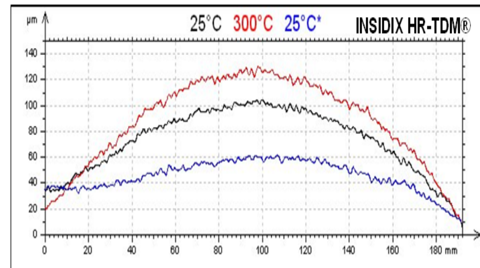


Figure 7. Thermal Deformation Measurement on CIWIS wafer

This process enables coplanar chip active face with the host silicon wafer. Chip co-planarity was observed by SEM observation (figure 8) and profilometer measurement. The typical gap between die face and wafer frame face is around 3µm which is a good value. Moreover the SEM photo shows a good continuity of polymer and silicon on the front side.

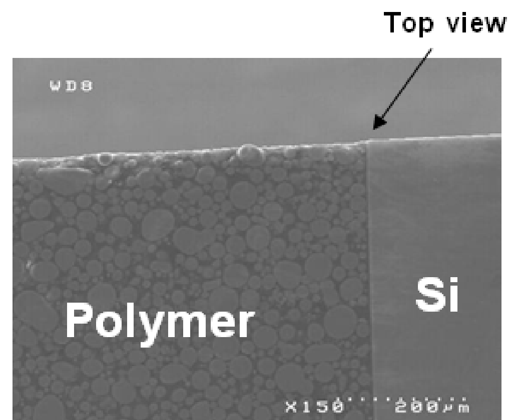


Figure 8. SEM observation on CIWIS

To make sure that the process to integrate chips in wafer does not damage the integrated circuit, a die with a CMOS was blended in a dedicated cavity of the test vehicle wafer. This die made by the CEA-LETI has CMOS with 80nm gate width. Id(Vd) was measured before and after the process. As shown in the graph (figure 9).

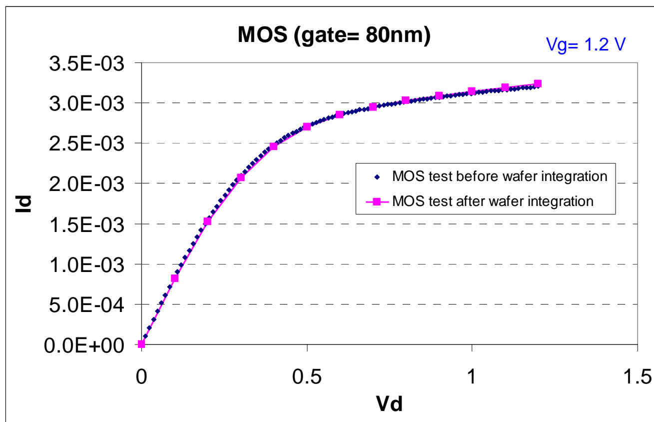


Figure 9. Id(Vd) measured before and after CIWIS process

Globally, the wafer characteristics are summarized below:

- ✓ Low warpage ~ 20 µm
- ✓ Chip placement ~ 5µm
- ✓ Good chip sealing in cavities
- ✓ Topology on wafer < 3µm

For evaluating if CIWIS technology has a potential to adopt as mass production, reliability test is necessary. There are currently in progress and further evaluation will be carried on the next months but the first results are encouraging.

Finally, the process flow is not complex and allows a short time to market. This approach can naturally address the market for all portable equipment (e.g. iPod, mobile phone, MP3, micro cards, hearing aids,…) which is extremely extensive. The CIWIS process is also compatible with other wafer frames such as glass wafer (figure 10)

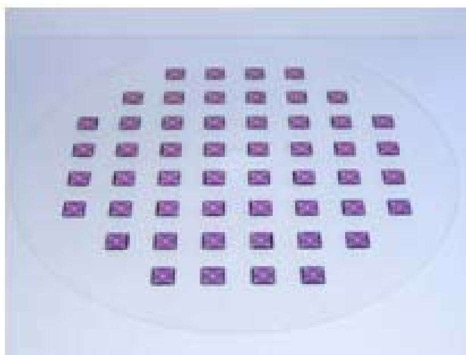


Figure 10. Ciwis on 200mm glass wafer

The next step is to work on implementation of an Above IC process on Chip In Wafer such as passive integration, rerouting, bumping and chip bonding (figure 11).

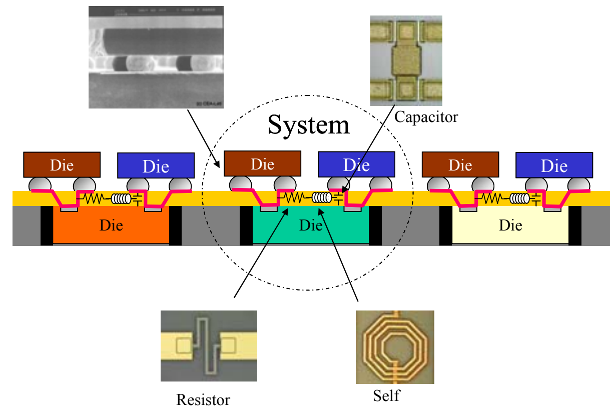


Figure 11. Embedded passive component on CIWIS

FROM THE WAFER LEVEL TO THE 3D INTEGRATION

In 2009 Sillon [11] from CEA LETI explains that we can distinguish two different approaches for Wafer Level 3D Integration, corresponding to two different business models. On one hand IDMs or their packaging subcontractors which have a direct access to design and can adapt front-end processes, will use the possibility to perform Through Silicon Vias (TSV) to achieve ultra compact /low cost assemblies. On the other hand, some end-users companies will look for generic technologies, which can be applied on heterogeneous chips coming from different sources. 3D stack will be in that case achieved thanks to vertical interconnections outside the silicon.

Using rebuilt wafers, it is now possible to process heterogeneous individual chips at the wafer level. Although these advanced technologies are competitive and, certainly improvable, it is difficult to process the embedded components to prepare the stacking or the 3D integration (particularly TSV).

HOW TO DO WITHOUT THE TSV ?

Consequently, a specific integration schemes allowing for chip stacking and chip-to-chip interconnectivity outside the die (without TSV) should be identified. The approach is based on embedding and contact redistribution of dice in film interconnect layers. Once embedded, these structures can be stacked using, e.g., solder microbump technology. This concept allows for the highest system level flexibility where thin dies with varying dimensions and shapes can be stacked and interconnected together with thin-film passive components. Different 3D architectures using plated Cu pillars have emerged on the past.

In 2002, Jung from Fraunhofer IZM [12] proposed an embedded chip in polymer. To connect the chip on the PCB, copper vias are made on thick BCB polymer and filled by electroless and electrodeposition processes. The same year, Fujitsu shows a similar approach with a chip scale module based on wafer thinning, chip stacking and

re distribution technologies. IMEC, in collaboration with CNRS and University of Barcelona proposes ultra-thin-chip stacking (UTCS) [13] to form 3D compact structures and using plated copper pillars. UTCS 3D was routing in thin film dielectric. Recently CEA-LETI proposed a concept called Via Belt Technology [14].

VIA BELT TECHNOLOGY

With the objective to reduce the packaging size without TSV, an original 3D architecture has been proposed to interconnect a base wafer with standard dice. Firstly, the dice are connected to the substrate face-down by low pitch interconnects (called µ-insert). In order to obtain a new surface, the wafer is embedded in a polymer and the mold-side is thinning by grinding, enabling copper pillars to be connected. A new rerouting and interconnection system enables a second die hybridization. The "Via belt" concept is presented on figure 12.

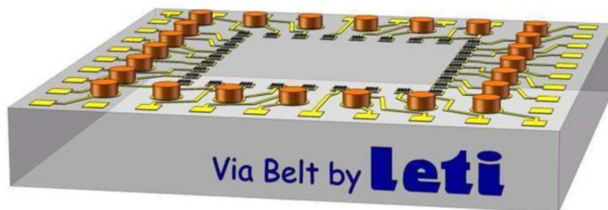


Figure 12. Via belt concept

The process starts on a base wafer (figure 13). This wafer can be just a blank wafer, an active wafer (for instance a memory wafer, memory being often the bigger die of an heterogeneous stack), or a rebuilt wafer, as described previously (CIWIS). The second step in our process is to perform flip chip, keeping the capability to integrate standard dice without any specific process on it.

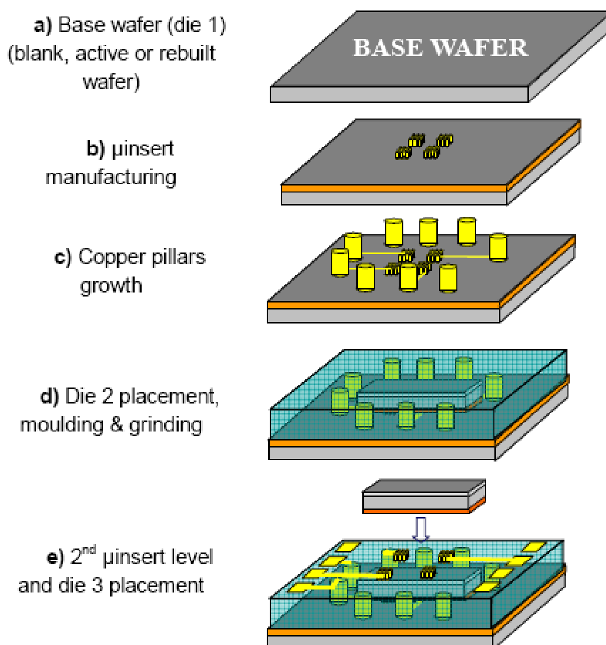


Figure 13 . Process flow for Via belt technology

The solution proposed by LETI is called µ-inserts interconnects (figure 13b). This process is based on nickel µbumps [15]. Several Ni pillars are electroplated on each pad. Each one has a diameter of 5 µm, for a thickness around 10 µm. Thanks to the pressure applied during flip-chip, Ni pillars are inserted in the aluminium pads of the top die, with no need for specific metallization (figure 14).

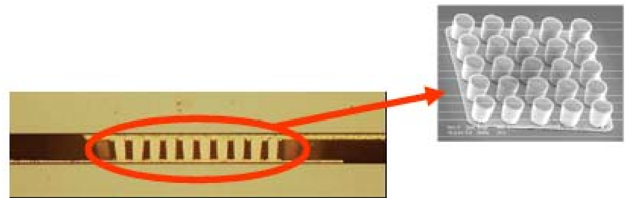


Figure 14. Cross section of a die hybridized face to down on a rerouting wafer – details on Ni µinserts (diameter 5µm)

In order to lift electrical contact to the 3rd level, a "belt" of copper pillars are grown around the footprint of die 2 as presented in figure 13c. A photo-pattern dry thick film is used for electroplating these pillars, which have a diameter of 100 µm for an initial thickness of 200 µm.

Die 2 (figure 13d) is then flip-chipped by thermo-compression on µinserts previously described, a specific polymer is spun to embed both dice and pillars, and then polymer is grinded until the copper pillars appear (figure 15).

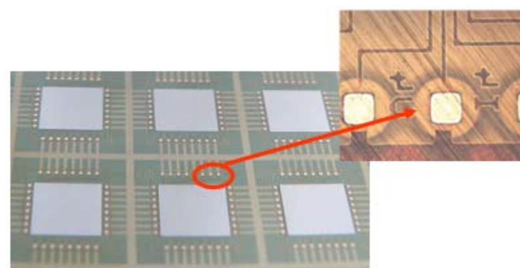


Figure 15. Top view after epoxy glue embedding and grinding

A second level of µinserts is patterned on the polymer layer and the third level of dice is placed face-down (figure 13e).

The figure 16 shows a cross section for a 3D stack on a demonstrator. The two levels of µinserts are clearly seen. The very thin interface is a good advantage when a thin stack is targeted. The thickness of mid die is 65µm after grinding.

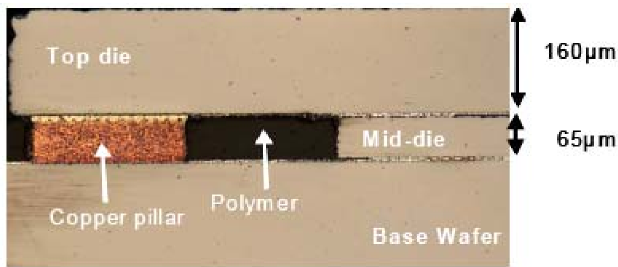


Figure 16 . Via belt cross section

Figure 17 shows a final assembly when the top die is placed face-down to be connected to the copper pillars.

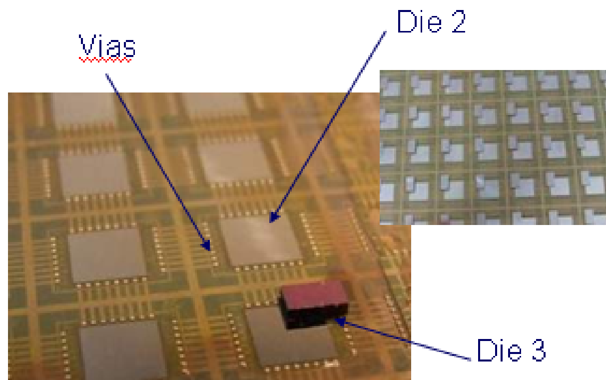


Figure 17. Via belt – final assembly

Electrical tests show an effective electrical contact between the three levels of dice. The first demonstrator has been achieved on a classical wafer base. However, rebuilt wafer coupled on via belt technology is an very interesting way to give access to wafer level technologies and 3D integration compatible with heterogeneous chips for end-users companies.

The CIWIS concept, previously presented, has been initially developed for fan out packaging or embedded wafer level packaging. Coupled to the Via Belt, we are able to propose a complete approach from a single chip to a 3D integration process including all the technical value chain.

CONCLUSION

As discussed initially, companies that want to develop "in-house" solutions prefer wafer level packaging because one of benefits is to simplify supply and value chain. Consequently with smaller companies, the main challenge is to process chips coming from different sources an without access to the wafer manufacturing

For niche markets which require only small quantities of chips or heterogeneous components of various manufacturers, wafer level technologies remain interesting but difficult to implement due to a limited wafer availability. The neo-wafer concept is really interesting because it makes it possible to select known good die, to integrate in a dedicated environment and to interconnect at a conventional redistributive chip level. One of the main drawbacks is the susceptibility to deformation due to thermo-mechanical constraints. The technical approach, proposed by CEA LETI, consisting in using a silicon matrix and a positioning of the chips in cavities makes it possible to solve this difficulty.

It is possible to consider a 3D integration starting from reconstituted substrates comprising of heterogeneous chips. In this case, the simplest solution consists of building the intra-connections outside the chips. The process via belt developed is particularly adapted.

All these developments in embedded wafer level packaging and 3D integration can be seen as an anticipation of future heterogeneous integration systems. Today, demand is increasing for a highly miniaturised system added to a low cost solution. The wafer level approach is probably one of the most promising solutions, the challenge is to be compatible with consumer market applications.

ACKNOWLEDGEMENTS

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REFERENCES

[1] US patent 5953588, September, 14, 1994 from Irvine Sensor

[2] G Poupon, JC Souriau, O Lignier, M Charrier, International Symposium on WLP , 1st IWLPC conference, San Jose, 2004

[3] B.Keser, C Amrine, T Duong, O Fay, S Hayes, G Leal, W Lytle, D Mitchell, R Wenzel, Proceedings of Electronic Components and Technology Conference, 2007, pp286

[4] M Brunnbauer, T Meyer, Proceedings of 3rd Annual Device Packaging Conference, IMAPS 2008

[5] E Furgut, G Beer, M Brunnbauer, T Meyer, Advanced Packaging Conference, SEMICON Europe 2006, Munich

[6] C Ko, S Chen, C.W Chiang, T.Y. Kuo, Y.C.Shih, Y.H.Chen, Proceedings of Electronic Components and Technology Conference, 2006, pp 322

[7] A Kumar, V Sekhar, S Lim, C Keng, G Sharma, S Vempati, V Kripesh, J Lau, D L Wong, , Proceedings of Electronic Components and Technology Conference, 2009, pp 1289

[8] I.S. Kang, G.J. Jung, B.Y. Jeon, Proceedings of 2009 International Symposium on Microelectronics, IMAPS, pp 482

[9] Y Kurita, K Soejima, K Kikuchi, M Takahashi, M Tago, M Koike, K Shibuya, S Yamamichi, M Kawano, Proceedings of Electronic Components and Technology Conference, 2006, pp 289

[10] JC Souriau, ME Faivre, N Sillon, , Proceedings of 11th Electronics Packaging Technology Conference, Singapour, 2009

[11] N Sillon, D Henry, JC Souriau, J Brun, H Boutry, S Cheramy, Proceedings of 2009 IEEE-IITC

[12] E Jung et al, IEEE / CPMT / SEMI annual international electronics manufacturing technology symposium No27, 2002 , pp. 46

[13] S Pinel et al IEEE Transaction CPMT, 2002, vol 25 , pp. 244

[14] J Brun, H Boutry, R Franiatte, T Hilt, N Sillon, Proceedings of Electronic Components and Technology Conference, 2009, pp 1670

[15] A Mathewson et al, Proceedings of Electronic System and Technology Conference, 2006