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Simulation of Embedded Components in PCB Environment and Verification of Board Reliability

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Abstract
Embedded components technology has launched its implementation in volume products demanding for highest miniaturization level. Small modules with embedded dies and passive components on the top side are mounted in hand held devices. Smart phones are the enablers for this new technology using the capabilities of embedded components. These modules have already shown a high level of reliability which has been a pre-requisite to get acceptance for volume products. Embedded dies are relative small with dimensions of about two by two millimeter and therefore all critical topics like the CTE mismatch of components and PCB materials, process die attachment are on a non-critical level. The roadmaps for the application development show a drastic increase of the complexity of the modules and in parallel increasing I/O numbers and die dimensions. Applications in the development pipeline show already die dimensions of seven by seven millimeter.
Based on this development roadmap a simulation project was started with the Material Center Leoben and Thales Global Services to evaluate the stress situation of embedded components and to build a thermo mechanical simulation model. The verification of this model was started by characterization of silicon dies and embedding of standardized components into PCB to get detailed stress parameters for these components. The next step of simulation deals with the simulation of embedding processes. Die assembly is the first process followed by the lamination process to form the embedded core. For the assembly process a DOE has been done to correlate the results with the simulation model.
All along the European funded FP7 HERMES*project huge efforts have been deployed in order to characterize the reliability of active and passive embedded chips, as well as packages assembled on the outer layers of the PCB . To achieve a high level of reliability of future complex modules using HERMES technology, work has been done to address different aspects like process optimization including different build-ups, best choice of base material, different size of active dice and design rules, knowledge of failure mode.

HERMES was successful closed in February 2012 and the final results of the HERMES embedding technology are shown in this paper. A dedicated test vehicle using a 4 (level of stacked µvia) +core +4 simulating a functional demonstrator have been manufactured and stressed under accelerated thermal cycling in the range -40°C/+125°C and under continuous monitoring.
This test vehicle includes embedded chips of different sizes, passive chips and BGA/QFN package assemblies on the external faces of the PCB. The design permits to isolate component (in daisy chain) and interconnections to facilitate the reliability and failure analysis. A detailed construction analysis of the manufactured boards has been done before to start the reliability test in order to have a reference.

Notes:

(*) HERMES: High density integration by Embedding chips for Reduced size Modules and Electronic Systems.

Introduction:
Chip embedding technology has become state-of-the-art during the last two years and industrial manufactured products are available. With this step to industrialization, the next applications are in the ramp-up phase. New applications with embedded sensors driven by miniaturization and optimized packages for the different demands for the sensors. Another logical trend for the embedded modules can be seen – increase of complexity by embedding of chips with one hundred interconnections and more. The size of the dies is growing fast. Looking at the first modules with die size in the range of two by two millimeter the actual module has doubled the die size. The size of silicon area to FR-4 area is increasing in a similar way which results in an increase of warpage in the chip and board area driven by the mismatch of the materials. Thermo mechanical simulation of these new packages becomes a very important tool to predict mechanical load and high stress areas in an embedded package.
The development of an embedded package will need special care for material selection, material data for every material type over a wide temperature range and detailed design data of the embedded modules. With this set of data the module in the first design stage the high stress zones become visible. The characterization of the die which will be embedded will be shown in this paper to get information on its mechanical properties. A four ball crack test for daisy chain dies delivered important data to get target values for the stress load. A simulation model on chip level war created using the layer build up and the design pattern to calculate the highest stress zones during embedding. In a next step the embedding process was simulated – lamination and the cool down to room temperature has been investigated.
Parallel to this activities test vehicles with different materials have been manufactured in the HERMES project to evaluate the reliability of the chip embedding technology. These test boards had embedded daisy-chain dies up to 10 x 10 mm and passive components. On the PCB surface, a variety of SMD components have been assembled to analyze the interaction between surface mounted and embedded components. Extended temperature cycle tests have been performed to evaluate the incidence of the PCB constitution and build-up (with or without embedded chips) on the solder joint reliability of BGA/QFN assemblies.

Simulation of the lamination process of embedded components

One of the key process steps of the embedding process flow (Figure 1) is the laminating process in the press, where the components are embedded into prepreg materials under high pressure and high temperature. The components have to withstand this stress environment, where pressure and temperature are increasing and decreasing due to the press profiles used and the behavior of resin flow of the prepreg materials.
In addition, the cooling of the PCB after curing of the resin can be even more important for the stress loading of the embedded components. Here, the different coefficients of thermal expansion of the involved materials as glass, resin, ceramic component, Si dies or GaAs dies are the key parameters that can introduce residual stresses in the system.

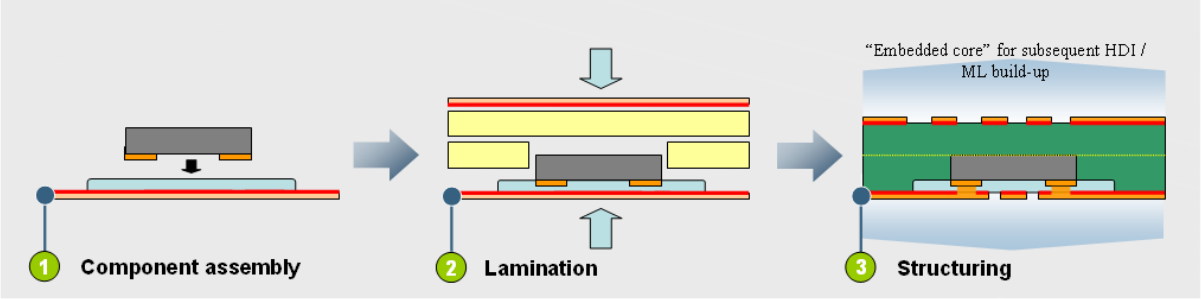


Figure 1 - Basic process flow for embedded components

In order to find the key parameters and possible stress hot spots during the lamination and curing of the press books, a simple analytical and numerical FE models was created. To use this model analysis of material parameters had to be done in order to get more knowledge about mechanical stress behavior of embedded devices like ceramic capacitors or Si dies.

Analysis of properties of embedded components

However, since PCBs with embedded components are produced by thermal pressing, a high mechanical reliability of components is generally required to survive the mechanical stresses during the process. The embedded devices like ceramic capacitors, silicon chips or GaAs chips are very brittle and their fracture force can be in the order of few Newton. Thermo-mechanical stresses may occur during operation of the board; hence the functionality of the entire package also relies on the mechanical strength of the components.

Semiconductor silicon chips are among the most commonly employed embedding components. The mechanical properties of such materials could be different depending on the crystallographic direction of the surface subjected to tensile stress. The degree of surface finishing or the presence of deposited metal contacts also plays a determinant role.

Hence, a different mechanical reliability of the board may be attained, depending on the side of the device that is exposed to tensile stresses.
The Si chips have two different sides, one constituted by mirror-polished pure silicon and the other side with deposited Cu-metal contacts and Al-interconnects, as shown in Figure2a and 2b. Therefore depending on which side tension will occur the behaviour of the dies is different.

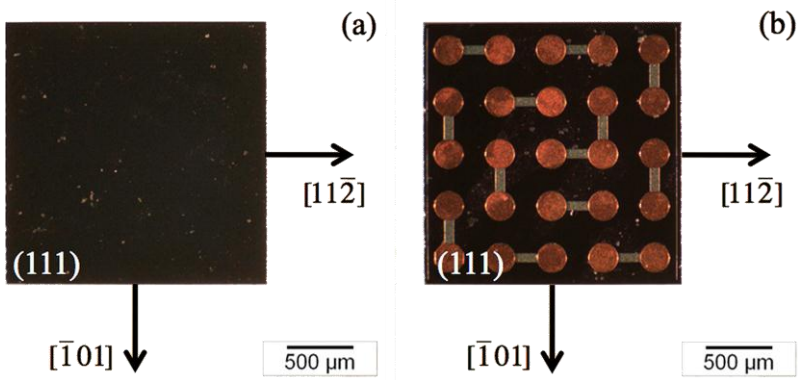


Figure 2: (a) Si-side and (b) metal-side with Cu-contacts (red) and Al-interconnects (white), crystallographic directions (as determined by EBSD) are explicitly indicated.

The strength of the Si-chips was determined using the B3B test (Figure 3). In this testing method, a rectangular plate (or a disc) is symmetrically supported by three balls on one side and loaded by a fourth ball in the centre of the opposite side which produces a very well defined biaxial stress field shown in figure 4. The load is increased until fracture occurs, and the fracture load can be used to calculate the maximum tensile biaxial stress in the specimen at the moment of fracture.

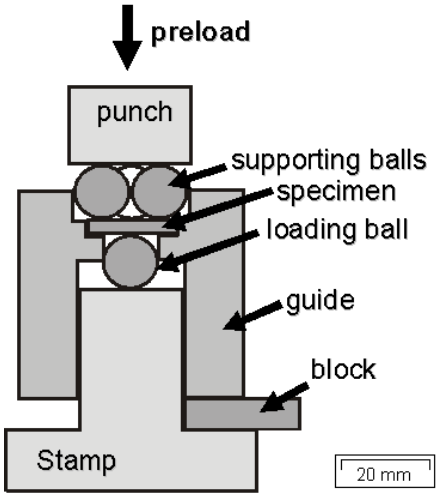


Figure 3: Schematic drawing of the B3B fixture

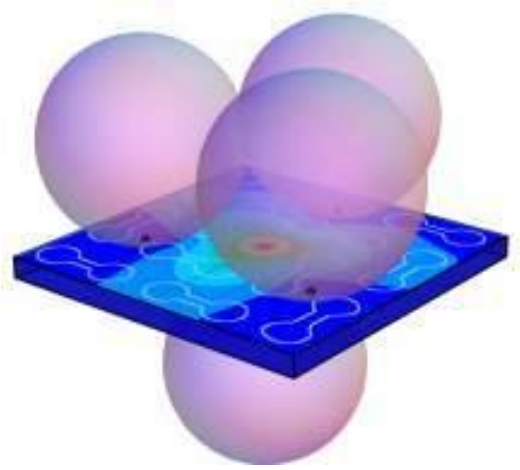
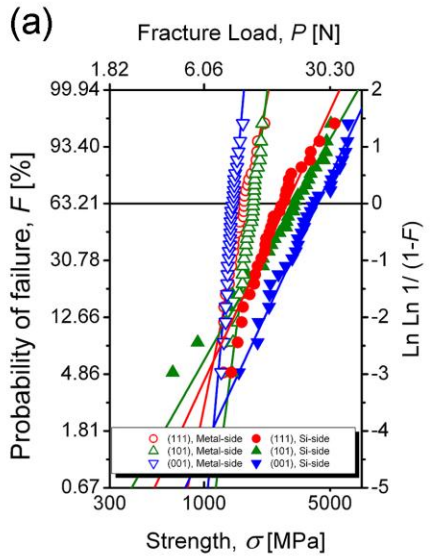


Figure 4: Stress field developed in the specimen during B3B testing, calculated with FEM.

Some results of the B3B-tests are shown in figure 5a. All tests have been done on both sides of the chip, on the Si-side and on the Metal-side of single-crystalline Si chips. The scale chosen in the graph allows representing Weibull–distributed data as a straight line. Each distribution was collected on a sample of ~30 specimens, which ensures statistical significance for the Weibull analysis.
Figure 5b reports the nominal characteristic strength σ_0 for a reference volume, and the corresponding Weibull moduli, *m*, for both Si-side and Metal-side testing configurations for each crystal orientation.



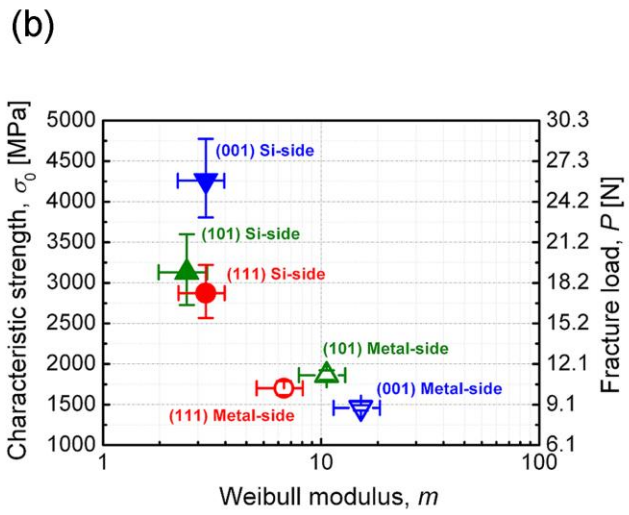


Figure 5a: B3B tests on Si-side and Metal-side Si chips

Figure 5b: Characteristic strength vs. Weibull modulus diagram for the tested specimens.

Strength results showed a clear statistical difference in the characteristic strength for both approaches, being in the Si-side more than 2 times larger (σ_0≈3500 MPa) than in the Metal-side (σ_0≈1700 MPa). The Weibull modulus in the Si-side is in agreement with common values for silicon wafers (*i.e.* m≈2.8), whereas for the Metal-side a very high value is obtained (*i.e.* m≈11). Fractographic analyses of broken specimens suggested that the lower strength of Metal-side specimens could be ascribed to the presence of a brittle silica layer and/or a stress concentration in the region where metal contacts are deposited on the silicon phase. The present findings where used to develop a finite element model for the lamination process for embedding components.

Modeling of the laminating process of embedded devices

The model for the laminating has to be described in two sub processes. First sub process is the heating and pressure sequence continued by the 2nd sub process curing under pressure. Therefore not only the lamination process but the cooling down from the curing temperature has to be considered in addition.
In laminates the misfit in the strains in the different materials causes nonuniform strains and thus stresses. The total deformation of a laminate with thermal loading can lead to bending and torsion. For cooling down, the layers of laminates that have small amount of thermal strains (like the embedded components) exhibit mainly compressive stresses. These compressive stresses would not limit the reliability of the PCB in the sense that brittle materials, like silicon or ceramics, have very high compressive strengths. Depending on the build-up of the laminate, thermal- and curing strains can cause different forms of stress- and deformation fields which may cause also tensile stresses in the components (very important for brittle materials).

In figure 6, three cases relevant for the PCB situation are shown, based on different sources of stresses that may occur during this process. In the first case, two thin layers with different thermal strains induce a bending of the laminate, as it is known in the case of a bimetal. Stresses in the layers are distributed uniformly over the whole length of the laminate. In the general case of more than two layers, bending also occurs. In special cases such as a symmetric build-up of the laminate or a certain material and thickness combination, no bending of the laminate should occur.
In the second case, the stresses occur near the interface of the two materials and at the surface of the laminate, as shown in figure 6. In the part that has the lower thermal strains, the resulting compressive stresses cause localized tensile stresses in the corners. These stresses are similar to stresses caused by clamping.

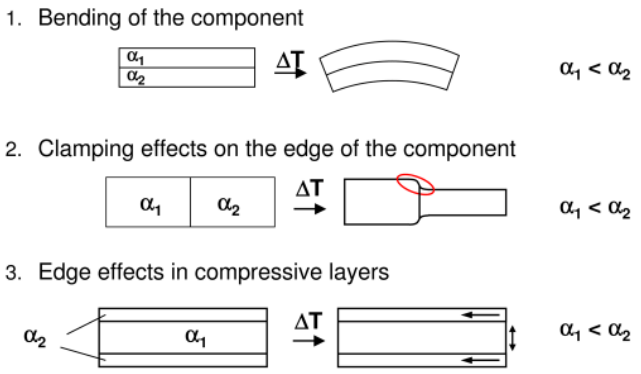


Figure 6: Cases of thermal stresses in a laminate

In scenario 3 a symmetric build-up of a laminate with biaxial compressive stresses in the middle layer parallel to the layer plane (i.e. in-plane stresses) is described. As investigated in multilayer ceramics with residual stresses, tensile (out of plane) stresses are generated at the edge surface of the compressive layers in the direction perpendicular to the layer plane. Their highest values arise in the center of the compressive layers and can lead to cracking of the material, thus being also relevant for design purposes.

For the calculation of the bending stresses and deflections, a simple analytical model can be used. The very simple bulid up of a printed circuit board is divided into segments that have a certain, uniform build-up. For these parts, a temperature loading can be calculated. Effects on the boundaries of those parts cannot be regarded with that simple model. The complex geometry of the prepregs like woven glass fibers with resin in between is simplified to a central glass layer and two resin layers on both sides of the glass layer. The thicknesses are chosen to obtain the glass content of the prepreg. The parts of a laminated core with an embedded component are shown in figure 7.

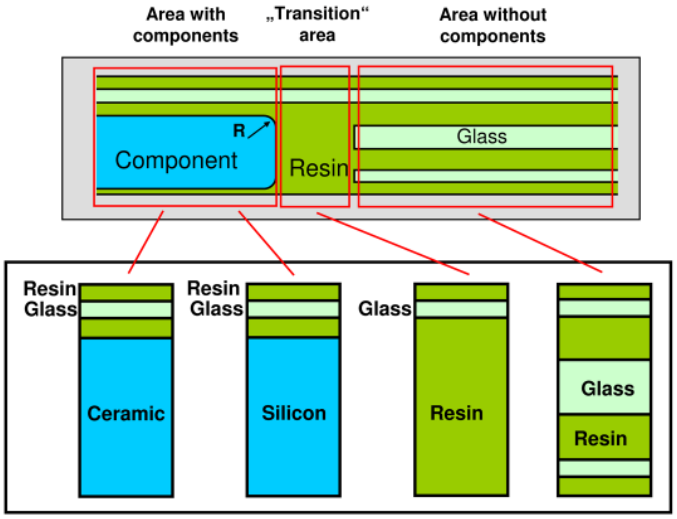


Figure 7: Simplified model of an embedded component in a printed circuit board

With this simple model different cases of stress modeling could be done. Together with the gained data out of the B3B-tests on Si chips and GaAs chips, and fracture investigations on ceramic devices FEM-simulations have been done.
In the following figures 8 and 9, two different stress simulations are described. Figure 8 shows a FEM simulation of the stress distribution caused by embedding Si-chip into a PCB. The red colored areas are regions with higher tensile stress, the blue areas have lower tensile stress. In figure 9 the case of embedding a ceramic device into a printed circuit board is simulated. With this simple approach it is possible to localize stress regions related on the dimensions of embedded component and build up structures. Therefore possible delamination in dedicated embedding constructions can be predicted with a FEM-simulation model.

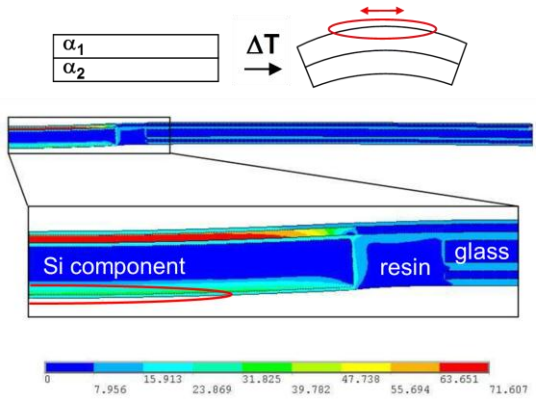


Figure 8: FEM-Simulation of embedded Si-chip

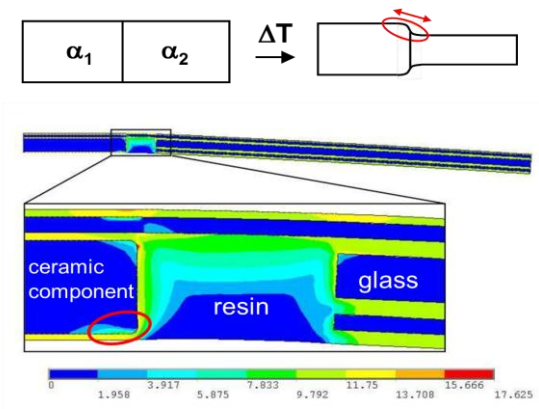


Figure 9: FEM-Simulation of embedded ceramic component

Analysis of the mechanical behaviour of embedded PCBs

To supplement the former study of the stresses seen by embedded components during fabrication, an experimental program was performed to characterize the effect of the PCB construction and base material on thermo-mechanical stresses. This study was conducted on dedicated test vehicles with various build-ups including embedded dies as well as BGA/QFN surface mount components on one side (see figure 6).

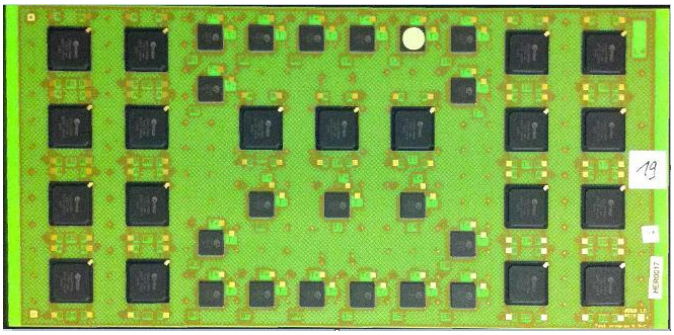


Figure 10: Test vehicle description

The selected assembled components were a 1.0mm-pich PBGA256 of 17x17 mm² and a 0.5mm-pitch QFN68 of 10x10 mm² daisy-chain packages, soldered using a conventional tin-lead assembly process (16 components of each type per board, 240 components of each type tested in total).
The BGA/QFN components in the central area are overlapping embedded chips of various sizes, while there is no embedded components under the other BGA/QFN. A cross-sectional view of a QFN overlapping a Si chip is hown on Figure 11.

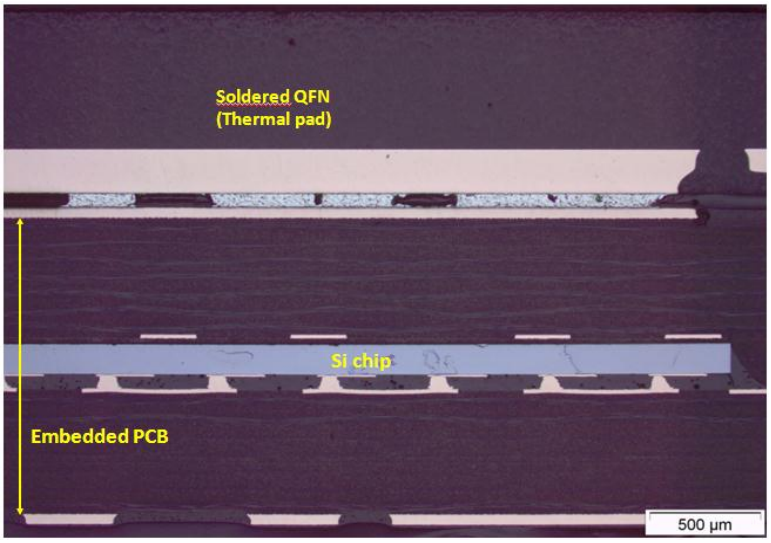


Figure 11 : Test vehicle cross-section view : soldered QFN overlapping an embeded Si chip

The experimental test program included a total of 15 stack-up configurations and the following variables :

- Two FR-4materials : MAT-C (Tg : 180°C) and MAT-D (Tg : 155°C)
- Two resin content [% of volume] : 34% - 43% (MAT-C), 43% - 55% (MAT-D)
- Several total PCB thicknesses between 1.2mm and 2.4mm (all measured on cross-sections)

The different test vehicle assemblies were submitted to an Accelerated Thermal-Cycling (ATC) test in the -55/+125°C range under continuous electrical monitoring. The ATC test was performed until failure of all BGA components and failure distributions were plotted using Weibull graphs: see figure 12 showing the 15 Weibull plots pertaining to the BGA packages. All the values of number of cycles to failure were normalized considering as 1 the F(50%) of the first failed population. The beta parameters were between 8.6 and 14 for the BGA populations, betweeen 4 and 9 for the QFN ones.

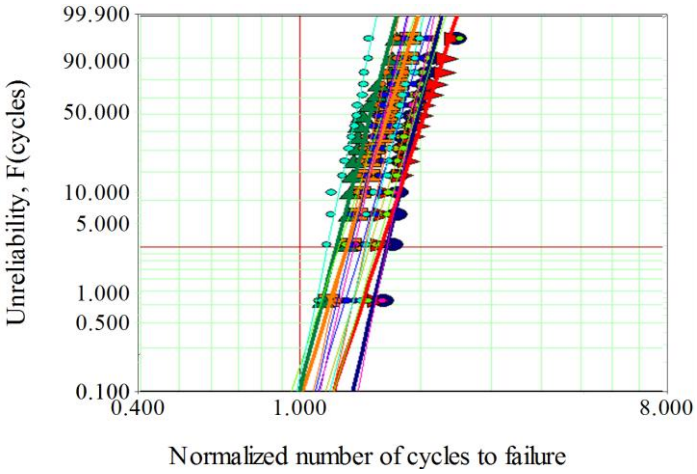


Figure 12: Weibull plot for 15 groups of BGA packages

Influence of the PCB build-up

The first analyzed parameter was the effect of the total PCB the thickness of the boards and the number of cycles to failure for the BGA components: see Figure 13 which shows the thickness of the board of each population as function of the normalized number of cycles to failure, F(63.2%). It can immediately be seen that the resin-content has little influence because the curves of the materials in different colors overlap. Similarly, the effects of the base material and the thickness are small. A 10% increase in thickness leads to about a 5% reduction in the number of cycles to failure.

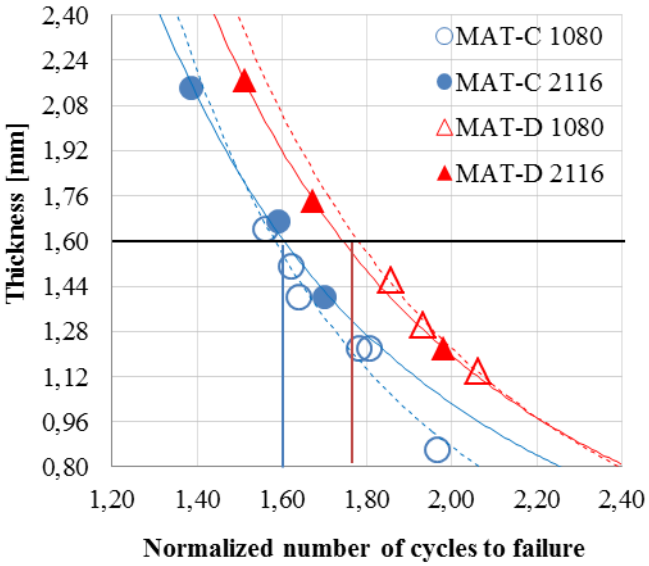


Figure 13: Normalized number of cycles to failure of BGA packages as a function of the PCB thickness

For QFN assemblies, the test results are incomplete as several components did not fail at the end of the ATC test. In this case, the percentage of failures at the end of the tests has been considered for each population according to the thickness

of the PCB (see Figure 14). Taking a thickness of 1.6 mm as a reference, 100% failures were recorded on boards with a lower resin content (boards made with 2116 pre-pregs) and less than 10% of failures were observed on higher resin content boards (1080 pre-pregs).

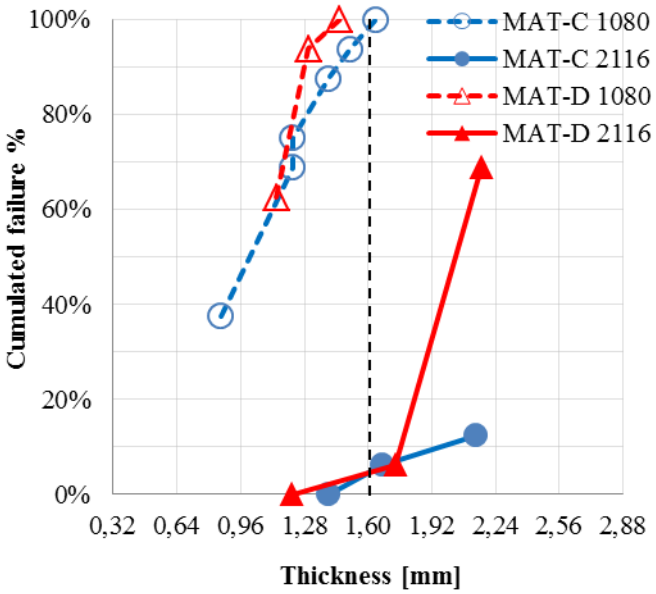


Figure 14: Cumulated failure of each population at the end of the test as a function of the PCB thickness

The Figure 15 shows the analysis of the number of cycles to failure as a function of the PCB thickness. Contrarily to BGA, the influence of the material looks more important. Considering a 1.6 mm-thick PCB, the number of cycles to failure is more than 3 times higher for MAT-C compared to MAT- D.
The difference between the two materials can also be explained by the difference in resin-content values. As mentioned in the description of the test vehicle, MAT-C contains about 34% of resin against 43% for MAT-D which translates into different thermal expansions.

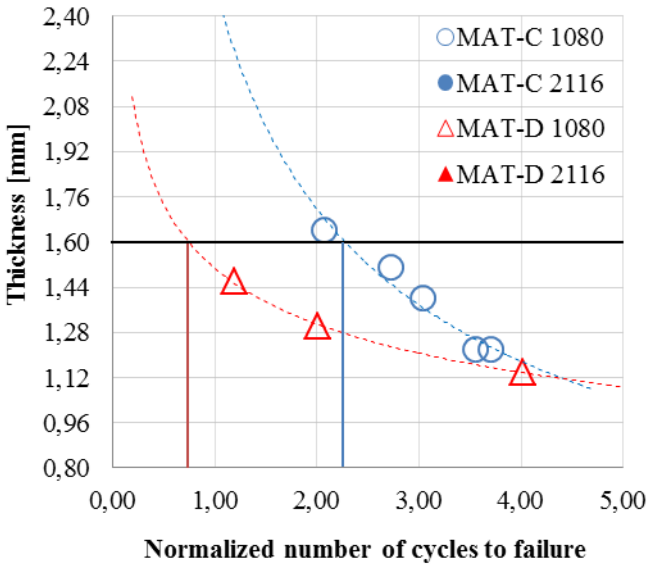


Figure 15: Normalized number of cycles to failure of QFN packages as a function of the PCB thickness

From the study, it can be derived that resin-content has a variable effect on the reliability of electronic package assemblies: high for the tested QFN components, but not significant for the BGA components.
The case of PCBs with embedded Si dies and overlapping surface mount BGA/QFN components has been addressed on another test vehicle board. The corresponding results will be presented in a separate future publication.

Conclusions

Chip embedding technology is currently used in high volume production for miniaturized modules used in smartphones, and is trying to extend to higher complexity devices with larger die sizes. For complex embedded systems, thermo-mechanical concerns increase and needs to be managed. In this paper, it has been shown that a FEM simulation approach has been developped to identify the high stress areas and the deformation fields within an embedded package. The model can be used to simulate the thermo-mechanical stresses seen by embedded components at different PCB manufacturing stages, in particular during lamination which is the most critical.
A complementary experimental test program using a large number of build-up configurations has also been conducted to analyze the incidence of the PCB structure and constitution on the solder joint reliability of BGA/QFN components.
Among the results, the study highlighted that for 1.0mm-pitch BGAs the effect of resin-content was insignificant and the effects of the base material and the PCB thickness were relatively small. By contrast, the influence of those parameters on assembled QFN components is significant, the total resin-content of the board being the most important parameter. Further analysis on a more complex PCB architecture will be presented to show the impact of embedded dies on the reliability of overlapping soldered BGA/QFN packages.

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