SELECTIVE SOLDERING DESIGN FOR RELIABILITY USING A NOVEL TEST BOARD AND SIR TEST METHOD

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ABSTRACT

The reliability of selectively soldered PCBs is a product of a complex interaction of several factors determined by the PCB design layout, flux, selective soldering machine, cleanliness, and end-user environment. Selective solder flux must be present and active to achieve reliable solder connections. The precision of flux transferred to the soldering area is critical to prevent leakage currents and dendritic growth on products used in harsh operating environments.

Surface Insulation Resistance (SIR) is an effective method for predicting long-term failure mechanisms and as a predictive tool for service life reliability. SIR is a quantitative test method to evaluate electrochemical reactions from ionic contamination following the selective soldering process. A custom designed mixed technology test board, used for this study, has a connector next to surface mount components. The reliability of the soldering process will be tested using SIR IPC-TM 2.3.7 test method.

The purpose of this research is to develop a test method designed to evaluate the electrochemical reliability of the selective soldering process at the assembly site. We will examine the impact of four (4) solder fluxes for flux spread and tackiness. Following these tests, the boards will be SIR tested at 40°C, 85% RH for 168 hours.

INTRODUCTION

Doubled sided mixed technology printed circuit boards requires advanced soldering methods. When the design is highly dense, smaller components narrow the conductive pathway. As the distance between conductors narrow, the risk of leakage currents and dendritic growth increase.

When the PCB includes a through-hole component or connector, selective soldering is a suitable method for attaching these components. Selective soldering is a point specific drag and point-to-point soldering method. The concern for selective soldering is the reliability of flux residues if not activated by the soldering process[1].

Selective soldering yields are a function of the equipment, software settings, flux composition, application of the flux, nozzle speed and solder temperature. Lead-free solder temperatures require the drag soldering technique to maintain solder temperatures, which must be controlled to prevent solder bridging, solder stringing, and fillet lifting[2]. The high soldering temperatures create a challenge for the flux. Too little flux results in solder defects, whereas too much flux leave residues that may result in electrochemical migration.

Changes within J-STD-001 Rev. G requires assemblers to qualify soldering processes, including either No-Clean or Cleaned PCBs, that result in acceptable levels of flux and other residues[2]. The acceptability of the residue conditions shall be determined at the point of the manufacturing process. Objective evidence requires a test method that can be used to qualify, validate and control ionic contamination levels.

SELECTIVE SOLDERING PROCESS

Selective soldering applications pose unique problems due to the localization of the soldering process[3]. The process requires high precision, especially when running a No-Clean process. Flux deposition on the board must be carefully controlled[3]. The physicochemical characteristics of the flux combined with selective soldering equipment are mandatory to achieve both solderability and reliability.

Wave solder liquid fluxes are designed to wet and spread. The risk of using a wave solder liquid flux with excellent wetting properties is the movement of the flux to other

neighboring components. During selective soldering process, unactivated flux left in areas outside the soldering point could cause reliability issues in the form of leakage currents and dendritic growth. The process of building reliable assemblies centers on the flux, process parameters, selective soldering machine, and material properties. To enable a highly reliable operation, a collaboration between flux formulators, soldering equipment, and assembly materials manufacturers is vital.

Localization of the flux residues through a drop jet fluxing process is not enough to guarantee the expected performance level. The flux design must be engineered to minimize the impact of unavoidable spreading and satellite's events. These events will result in partially heated flux residues, which won't be removed by the washing action of the solder[4]. They pose a serious threat to the reliability of the assembly, as ionic residues can induce electrochemical migration, corrosion, and resistance losses, which will invariably result in field product failures.

The fluxer configuration on the selective soldering machine plays an integral part in applying the flux, controlling the preheat profile, maintaining heat to the soldering alloy and soldering each filet without the formation of solder bridges. The flux must work in concert with the drop jet dispensing head to flow seamlessly during the entire operation, localize the deposit and finally stay in place[4]. The fluxing process parameters (Open time, Frequency, Robot Speed), as well as the board, preheat temperature are critical parameters, and their optimal settings depend upon the characteristics of the flux (viscosity, surface tension, solid content, solvent)[4].

PURPOSE OF THE RESEARCH

Miniaturization along with the placement of numerous components across a highly dense printed circuit board has brought concerns over the reliability of the No-Clean soldering process. When flux residue becomes trapped under low stand-off components, or in unsoldered areas of the board, the residue may be ionic and leave an unevaporated solvent, activators and metal complex intermediates with different chemical composition and concentration levels depending on the thermal profiles[5].

When building electronic devices, there is mounting evidence that as component density increase, so does the sensitivity of the circuit to ionic contamination[2]. There is a void at the assembly site for testing production assemblies to validate that the soldering process is in control and results in acceptable levels of ionic residues.

The purpose of this research is to develop a test board to evaluate the selective soldering process and test method that can be used to assess the sensitivity of the circuit to ionic contamination.

SIR TEST METHOD

Surface Insulation Resistance (SIR) testing is a method used for incoming board cleanliness, materials investigations and qualifications, quality conformance, prediction of long-term failure mechanisms and as a predictive tool for estimated service life[6]. SIR measures bulk conductivity, leakage through electrolytic contaminants and electrochemical reactions at or below the surface of electronic circuits.

Numerous manufacturing process variables affect the properties of the materials system. Free metallic ions such as tin-copper intermetallic when mobilized reduce surface insulation resistance. Free metallic ions are metal ions that are released or leached from or dissolved from the soldering alloy that is being used in the solder joint formation. To reduce intermetallic formations, electrical conductors are separated by the dielectric solder mask. When the clearance between the conductive path is narrow, the mobility of these metal ions in moisture, combined with the electrical field cause leakage currents and dendritic growth between adjacent conductors. Each of these reactions affects SIR.

On highly dense circuit layouts, smaller and more compact spacing is sensitive to contamination. During the selective soldering process, the flux that is not contained at the soldering location has the potential to leave unactivated flux residue that can spread to outlying areas of the board. Unactivated flux residues can dissolve in water, forming a weak electrolytic solution. Such solutions are often acidic. The flux that migrates away from the soldering site leaves a harmful residue, which results in a higher the rate of attack on exposed metals. The presence of an electrical potential dramatically accelerates the process.

When the selective soldering process is in control, the remaining flux will cross-link. The residue from the soldering area should be benign. The insulating characteristics of the crosslinked flux residue result in higher SIR levels. During selective soldering process, proper heat activation increases flux cross-linking and encapsulation properties.

Good SIR performance is related to the materials selection and controlled process conditions that render an ionically clean assembly. No-Clean flux technologies are designed to leave benign low residue free of ionic contamination. When ionic contamination is present on the board surface and under component terminations, it is critical that the assembly is cleaned to achieve high SIR levels. If ionic contamination remains, it can become entrapped in ensuing operations, leading to lower SIR levels. There are also nonionic residues that can influence SIR, notably glycol and silicone surfactants that are present in permanent solder masks and some solder fluxes.

TEST BOARD DESIGN

SIR test data is dependent on the geometry and configuration of the test vehicle. The test board used for this study is designed to evaluate the reliability of a mixed

technology PCB process. The highly dense test board populated with chip caps and a connector body is ideal for assessing the reliability of the selective soldering process. Figures 1-4 illustrate the design features.

Many factors related to the layout of the test patterns on a printed board can affect the test results. These include line spacing, physical geometry of the test patterns, routing of the lands from test patterns to contact fingers, physical spacing of voltage application lines and current return lines, the physical size of the test board, the presence of guard traces, and surface topography of the laminate. It is essential that the test boards be processed under a set of typical manufacturing conditions.

This highly dense board may respond more quickly to changes in temperature and humidity due to its lower thermal mass. Also, the high density may allow the board to be more sensitive towards the effect of contamination. This is due to the combination of smaller spacings, and larger number of "opportunities" (overlaps tween cathode and anode) for dendritic growth.

The board has four quadrants. Quadrants 1 & 3 SIR electrical traces are patterned to measure resistance at the SMT and through-hole sites on the connector body. Quadrants 2 & 4 SIR traces are patterned to measure surface resistance at on the SMT capacitive components.

It is vital that the test coupon is assembled and in parallel with the manufacturing processes planned for the final production circuit assembly. Trend analysis identifies changes that occur from the design and assembly process. Figure 1 and 2 show the top and bottom side of the test coupon designed to utilize both SMT flux and thru-hole flux near a connector and under a connector as well as to adjacent chip style components.

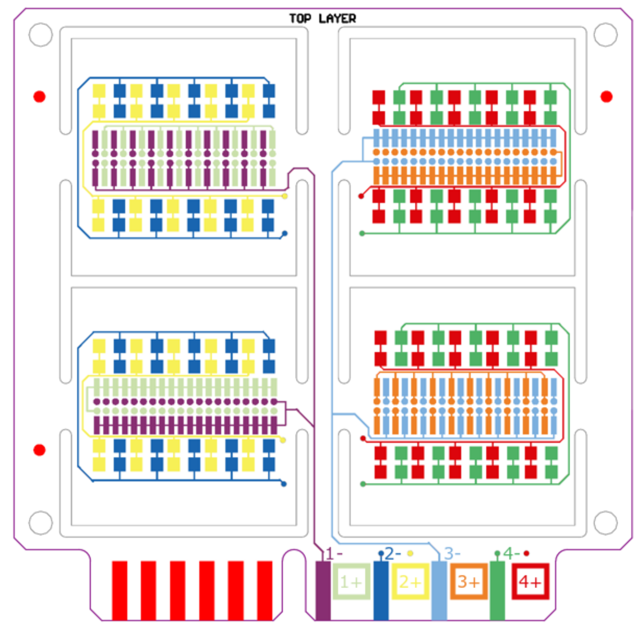

Figure 1: Top Side Pattern and Electrical Routing

Test board design concept utilizes an all- in - one thru-hole and SMT connector. The idea is the outer two rows of a 4-row connector is SMT legs, and the inner two rows of the connector is a thru-hole concept thus achieving an all – in – one connector. The use of an all –in –one connector is to get both SMT flux and thru-hole flux localized underneath a connector body thus promoting a challenging SIR test and thus showing the ability to control two flux types in close proximity to each other.

The connector design, as mentioned, is an all-in-one connector that has both SMT and thru-hole leads in one connector configuration. The test board design utilizes chip style components around the connector. Flux residues from the selective soldering process and SMT components are close proximity. The capillary attraction or overspray from the thru-hole flux application creates the potential for the residues to interact. The flux residues from both processes form a potential reliabilty concern.

The other interesting design feature is the use of the all-in-one connector whereby the connectors are hooked up electrically in parallel so that the resulting SIR measurements test both a horizontal SIR pinout as well as vertical in the same SIR readings. This is to ensure that spacing in both planes is captured during testing. Quadrant 1 and 2 are hooked up as follows: Horizontal rows of connector 1 are hooked to vertical rows of the connector in quadrant 2 to ensure that spread is captured in both directions depending on flux flow and spread. The chip-style components of quadrant 1 and 2 are also hooked up in parallel to ensure they are measured separately from the connector as to not influence the SIR readings and thus we can now assess the results of processing a highly dense connector as well as adjacent components near the connector.

Note quadrant 3 and 4 are set up as a duplicate of quadrant 1 and 2 for repeatability study.

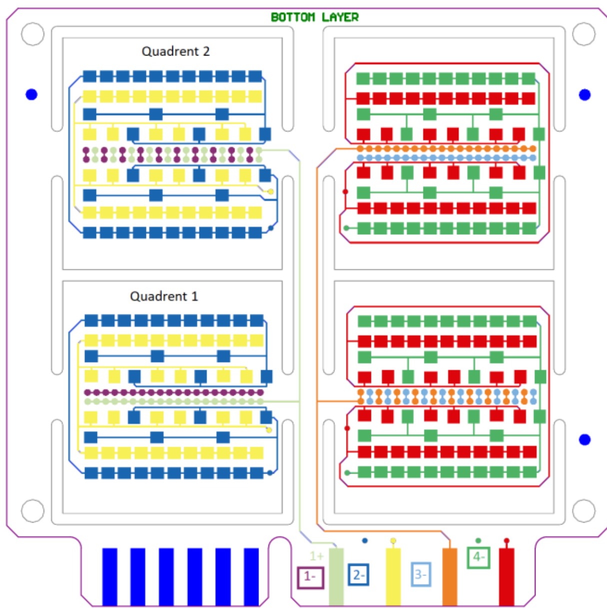

Figure 2: Bottom Side Pattern and Electrical Pattern

Figure 3 shows the spacing in both the horizontal and vertical plane of the all-in-one connector. The connector spacing is as follows: Thru-hole to thru hole in the horizontal plane is .02 inches, and the thru hole to SMT pad is .04 inches. This footprint is a good SIR test for fine pitch selective soldering applications for fine pitch connectors. The dummy 1206 capacitors have a .048 mil space between pads for SIR testing. The chip-style components are oriented for natural capillary attraction under these components should excess flux be presented during the manufacturing process.

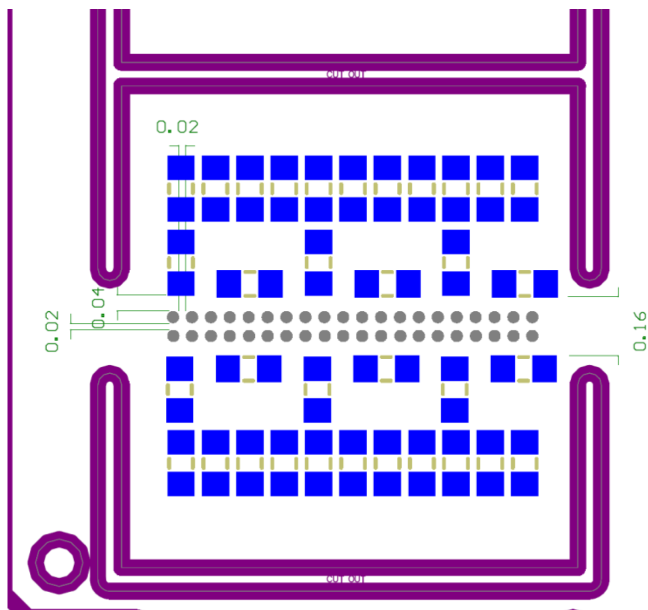

Figure 3: Horizontal and Vertical Line Spacing

The connector two outer rows have SMT solder pins, and the two inner rows are thru-hole pins in the same connector.

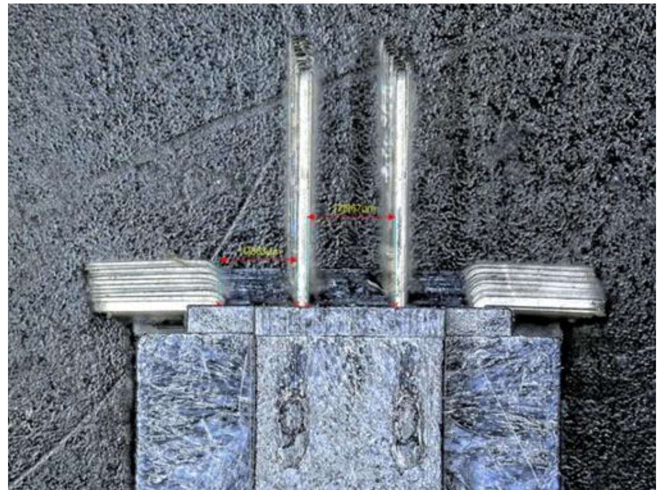

Figure 4: Side Photo of the All-In-One Connector

EXPERIMENTAL

Assemblers who seek to qualify soldering and/or cleaning processes need to determine acceptable levels of flux and other residues. Fluxes and flux residues have often been identified as the root cause of electrochemical failures. Flux chemistry is becoming increasingly complex and so even changing fluxes within one J-STD-004 flux classification (e.g. going from one ROL0 flux to another ROL0 flux) will result in a different residue assay. Since an electronic assembly represents a sum of residues from the process, flux residues from the SMT process may interact with flux residues from the selective soldering process. The designed experiments compare and contrast selective soldering fluxes to determine the best flux that supports a No-Clean process.

Four selective soldering fluxes will be evaluated to determine electrical performance in hot/humid conditions. Three Designed Experiments were run:

1. DOE #1
   a. Flux Tackiness
   b. Flux Spread on PCB
   c. Flux Spread Aluminum Foil
   d. Flux Spread on Fax Paper
2. DOE #2 – SIR
3. DOE #3 ~ IC

DATA FINDINGS

DOE #1 evaluated the localization of the flux from spreading and splashing events.

Chalk was applied to one of the quadrants for each of the four fluxes. Figure 5 illustrates that all fluxes tested were dry and non-tacky.

Flux Tackiness Test Results	
Flux #1	Non Tacky
Flux #2	Non Tacky
Flux #3	Non Tacky
Flux #4	Non Tacky

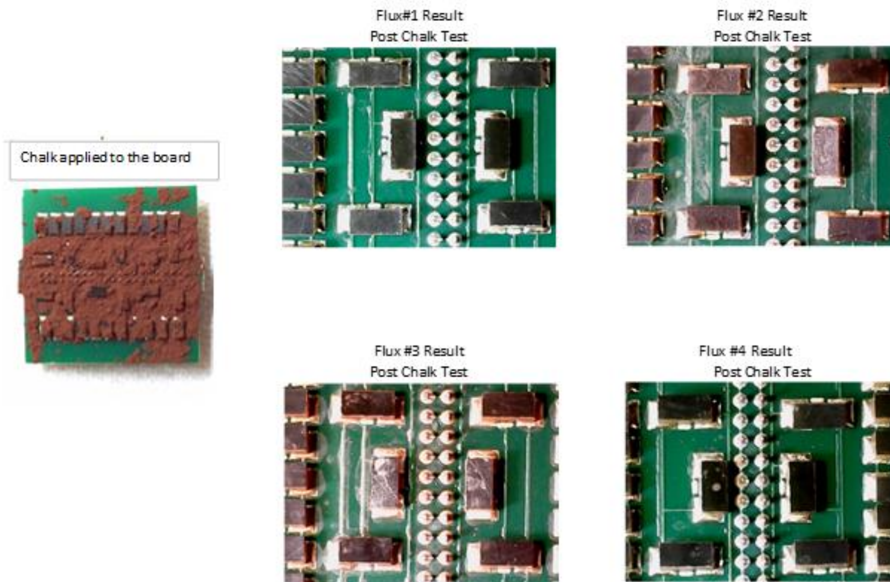

Figure 5: Flux Tackiness Test Results

Figure 6 illustrates the Flux Spread at the site of the connector. All four fluxes showed minimal spreading. Flux #2 was more viscous than the other three fluxes tested.

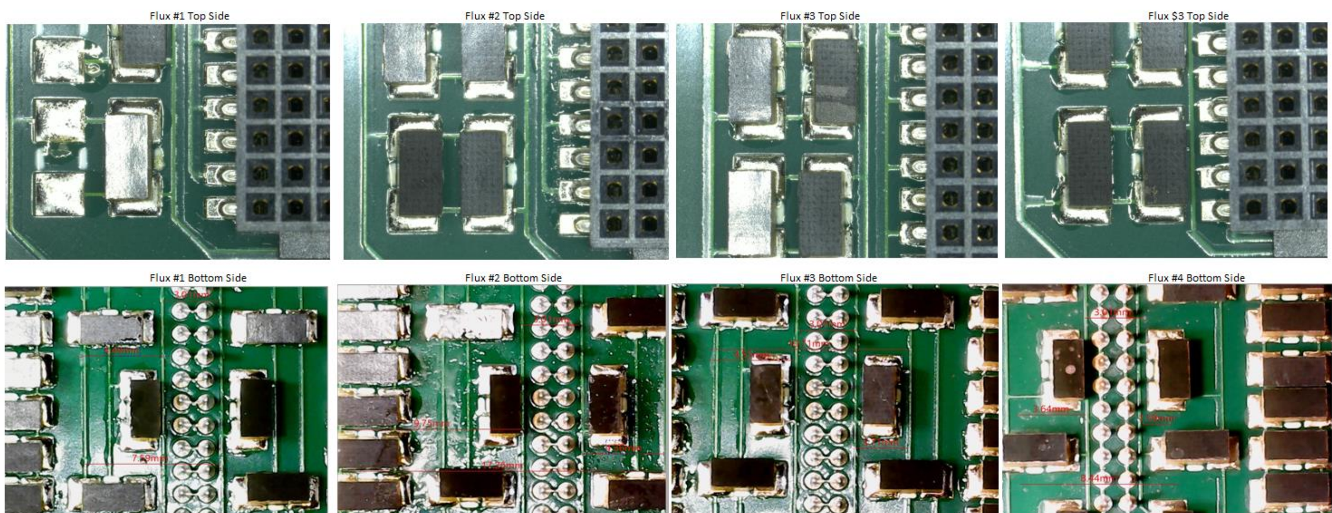

Figure 6: Visual Image of the Connector Body and Flux Residues

Figure 7 tested the flux spread on aluminum foil.

The surface tension of the aluminum foil is 32 Dynes

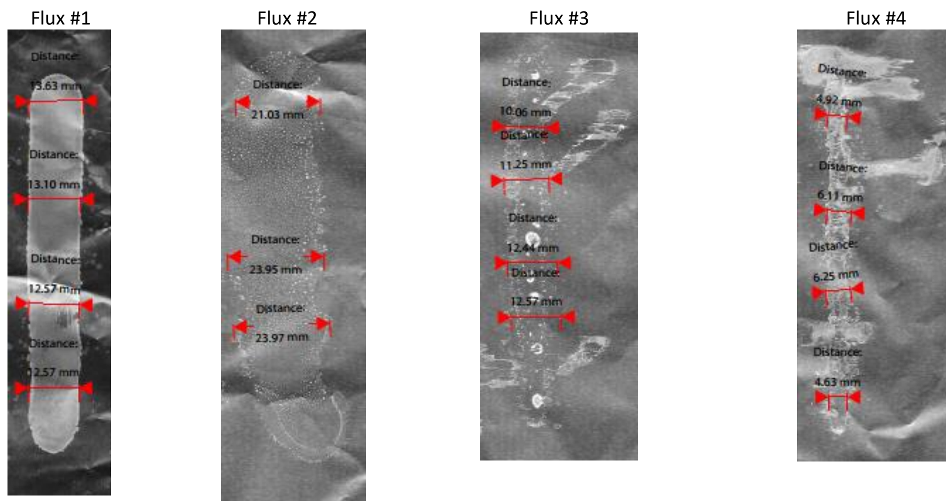

Figure 7: Flux Spread on Aluminum Foil

Figure 8 illustrates flux spread on fax and litmus paper.

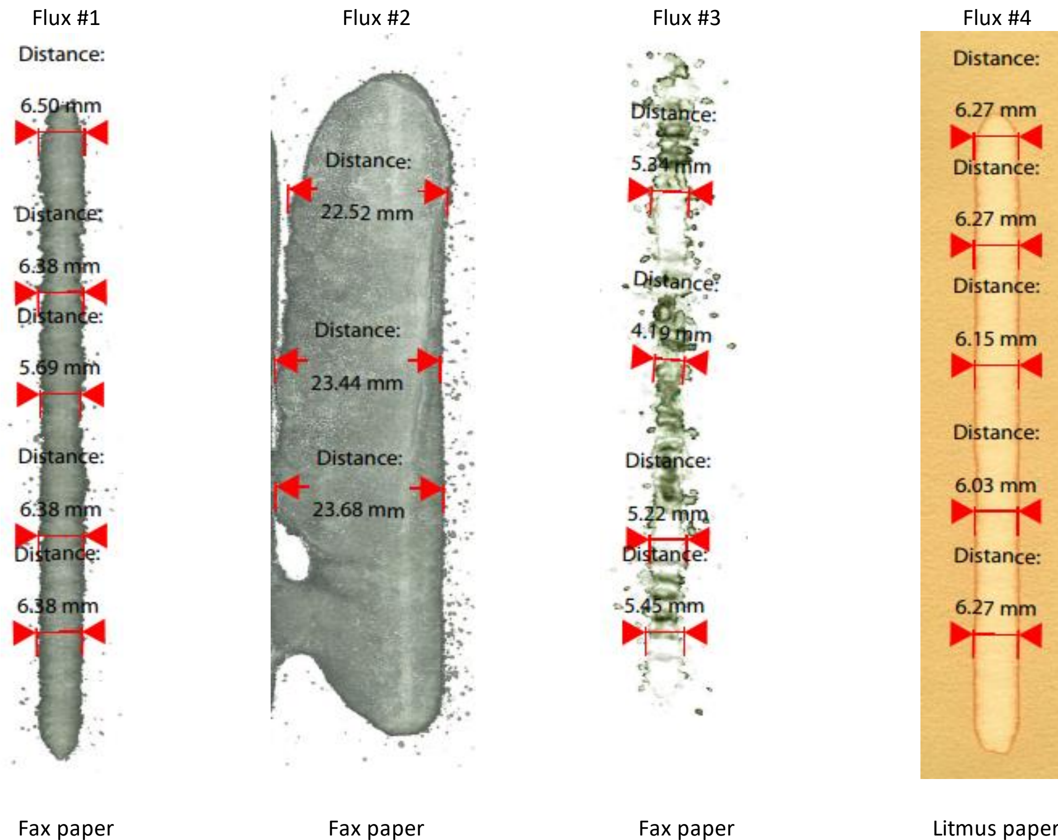

Figure 8: Spread on Fax and Litmus Paper

DOE #2: SIR test method was used to measure bulk conductivity, leakage through electrolytic contaminants and electrochemical reactions at both the connector and capicator areas of the test board. IPC-TM-650 2.6.3.7 test method was used to assess the No-Clean selective solder flux and solder paste flux residues. The test was run at 40°C, 90% RH, and 8V bias. Reading were taken every 20 minutes over a 7-day period (168 hours).

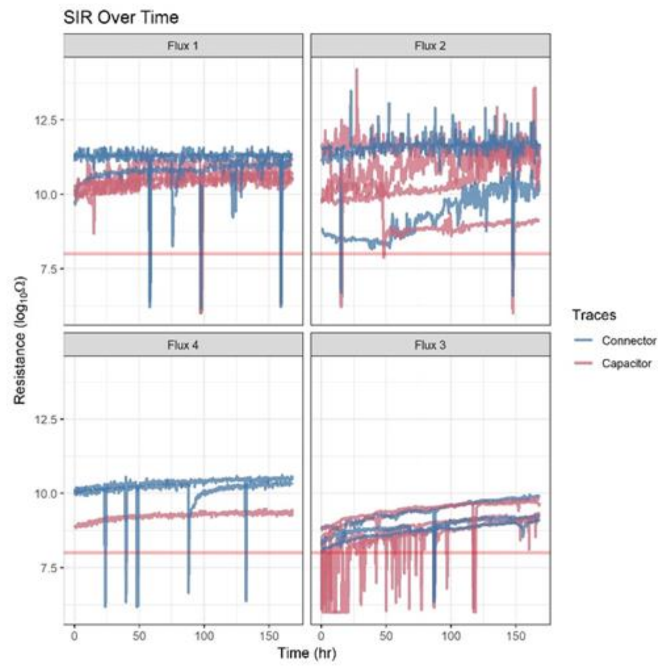

Figure 9: SIR Values of the Connector and Capacitor on Boards Built with Four Liquid Fluxes and One SMT Flux

Figure 10 illustrates a comparison of the flour selective soldering fluxes over the 168 hours test.

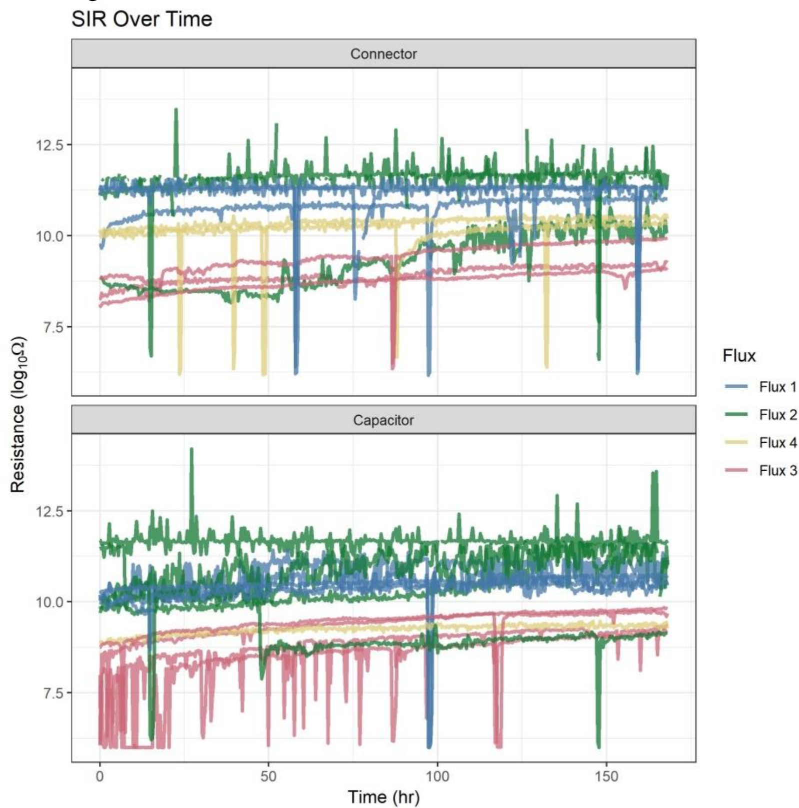

Figure 10: Comparison of the SIR values of the Four Liquid Fluxes and One SMT Flux

Figure 11 illustrates the pooled SIR resistance values for the four selective soldering fluxes evaluated.

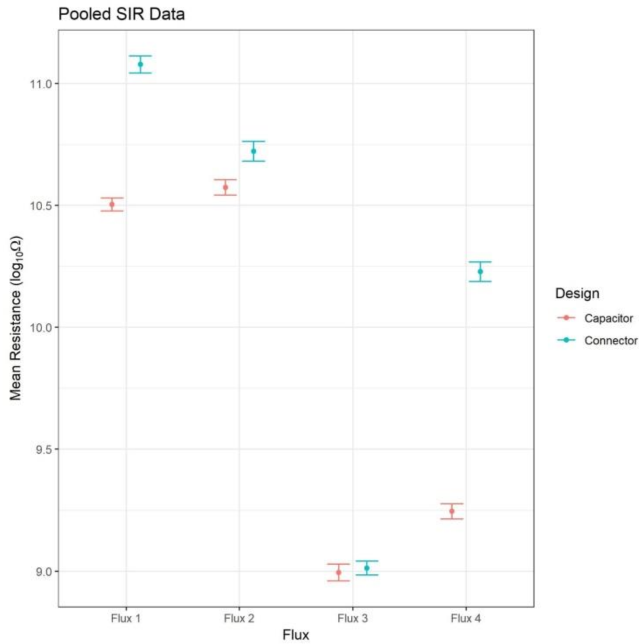

Figure 11: Box Plot of Pooled SIR data for the Four Liquid Fluxes and One SMT Flux

DOE 3: IC Test Evaluations

Following SIR testing, the four quadrants of the test board were sectioned for Ion Chromatography (IPC TM-650 2.6.3.8) testing. With both sides of the board populated, the IC values report the level of ionic contamination at the component area. The boards designated as "Yes" were boards that previously underwent the flux spread testing noted in DOE #1. The handling during this time resulted in higher levels of total ionic contamination.

Figure 12 reports the Total Ionic Contamination (µg/in^2) for each of the four selective soldering fluxes.

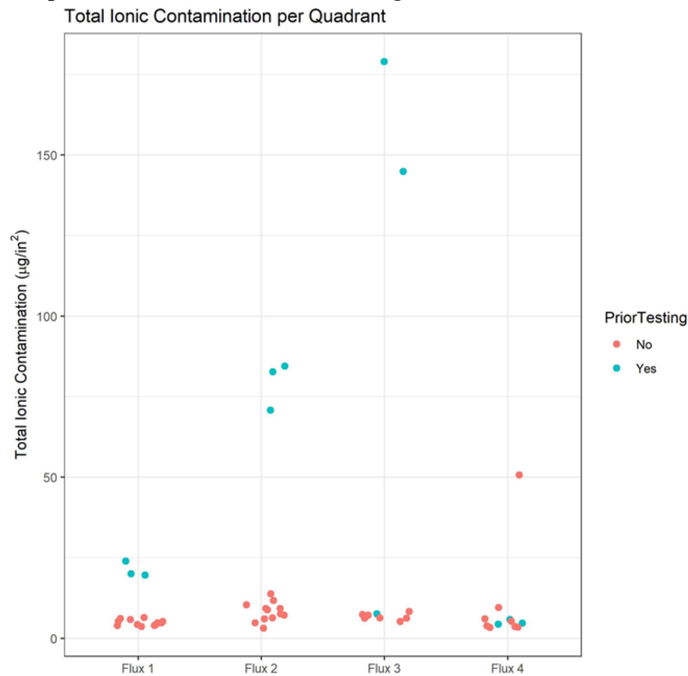

Figure 12: Total Ionic Contamination for the Four Liquid Fluxes and One SMT Flux

Figure 13 reports the total ionic contamination by quadrant for the four selective soldering fluxes. Channels A, B, C, and D represent the four quadrants on each board. The quadrants were separated for the IC testing. Each quadrant represented a separate IC extraction.

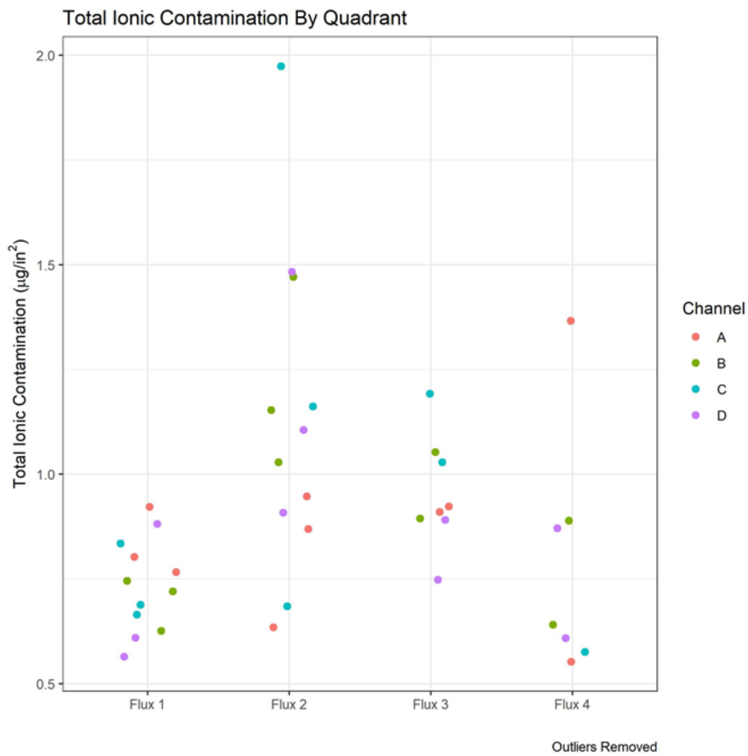

Figure 13: Total Ionic Contamination by Quadrant for the Four Liquid Fluxes and One SMT Flux

Figure 14 reports the distribution of the total ionic contamination for the four selective soldering fluxes.

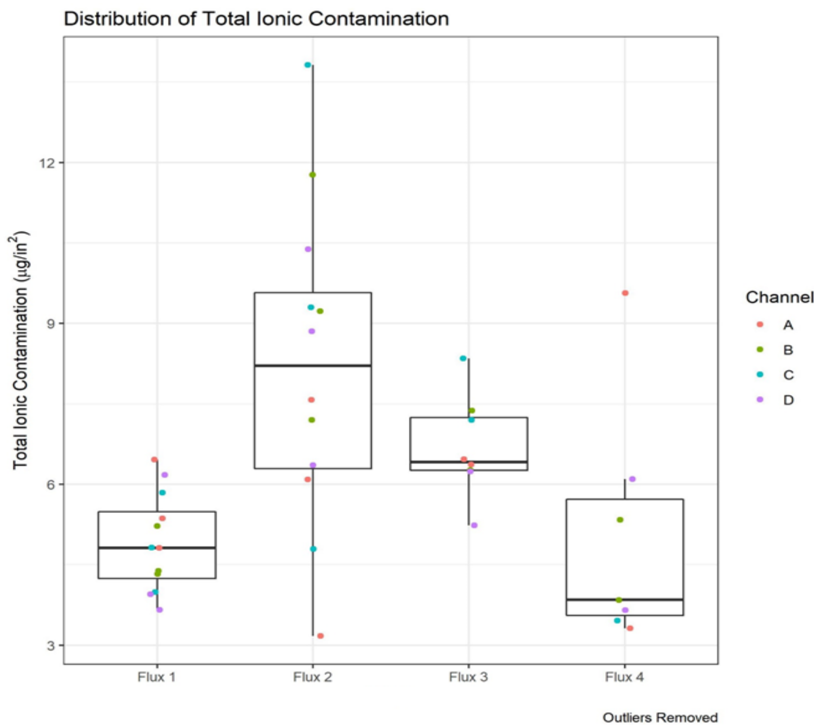

Figure 14: Distribution of Total Ionic Contamination for the Four Liquid Fluxes and One SMT Flux

INFERENCES FROM DATA FINDINGS

Flux characterization, SIR and IC testing were performed on a custom test board designed to evaluate flux bearing materials and the selective soldering process. The experiment compared four different soldering fluxes.

Selective solder flux design requires a high surface tension to prevent spreading and sattellite's during application. Flux 1 and Flux 4 are Selective soldering formulated fluxes. These two fluxes were the best performing fluxes. Flux 1 and Flux 4 had the highest SIR and lowest ionic contamination values. Flux 2 and Flux 3 are wave soldering formulated fluxes.

Selective soldering fluxes must be contained at the point of soldering. The flux that spreads to areas outside the soldering point does not come into contact with solder wave. The typical activator packages used in liquid fluxes may include carboxylic acids, halides, and covalent-bonded halogen compounds. With limited temperature exposure of the activator package, the flux residue that spreads outside the soldering point may contain an unevaporated solvent, raw activator, and metal complex intermediates. SIR testing is an effective method for materials investigations and qualification.

The SIR test results found that Flux 1 had the best overall resistance values for the four selective soldering fluxes tested. The No-Clean flux residues under the capacitors exhibited the highest stability for Fluxes 1 & 4. On Fluxes 2 & 3, the mixture of the liquid soldering flux with No-Clean flux had evidence of leakage current and potential dendritic growth.

The component-specific IC results find that Flux 1 & 4 had the lowest levels of ionic contamination in the connector and capacitor areas.

CONCLUSIONS

OEMs, CMs, and Assemblers find need to evaluate material and process changes on their circuit card assemblies. There is also the need for improved test methods that can be used at the assembly site for system design, process development, process control, and quality assurance. Surface Insulation Resistance testing is an effective method for incoming inspection, materials investigations and qualifications, quality conformance, prediction of long-term failure mechanisms and as a predictive tool for estimated surface life.

It is essential that the test boards be processed under a set of typical manufacturing conditions. The test board design for this research used a highly dense layout for both the connector and SMT components. The board layout included line spacing, physical geometry of the test patterns, routing of the lands from test patterns to contact fingers, physical spacing of voltage application lines and current return lines, the physical size of the test board, the presence of guard traces, and surface topography of the laminate. The testboard was effective at performing materials evaluations on selective soldered boards.

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