Reliability of ENEPIG by Sequential Thermal Cycling and Aging

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Abstract

Electroless nickel electroless palladium immersion gold (ENEPIG) surface finish for printed circuit board (PCB) has now become a key surface finish that is used for both tin-lead and lead-free solder assemblies. This paper presents the reliability of land grid array (LGA) component packages with 1156 pads assembled with tin-lead solder onto PCBs with an ENEPIG finish and then subjected to thermal cycling and then isothermal aging. To determine thermal cycle reliability, daisy-chain LGA1156 packages were used to enable the monitoring of solder joint failures. The assemblies, were built with a vapor phase reflow machine or using a rework station. Then, they were subjected to thermal cycling ranging from –55°C to 125°C. Subsequent to the completion of two hundred thermal cycles, the assemblies were isothermally aged for 324 hours at 125°C to determine the effect of isothermal aging on intermetallic formation and growth, which is one of the concerns for tin-lead solder assemblies. To determine the effect of exposure at temperatures higher than 125°C, the aged samples were subjected to 100 thermal shock cycles between –65°C and 150°C.

A number of characterization methods were used to ensure the integrity of solder joints. These included nondestructive evaluation by X-ray, daisy-chain monitoring at thermal cycle/aging intervals, and destructive characterization by cross-sectioning. The cycled/aged samples were cross-sectioned and characterized by optical and scanning electron microscopy (SEM). Assembly processes and SEM photomicrographs showing damage progression and IMC/microstructural changes, as well as elemental analyses by x-ray energy dispersive spectroscopy (EDS), were also presented.

Key words: ENEPIG, HASL, solder joint reliability, LGA, land grid array, thermal cycle, thermal shock cycle, solder joint reliability, isothermal aging

1.0 INTRODUCTION

The IPC standard team has helped in easing the implementation of electroless nickel electroless palladium immersion gold (ENEPIG) surface finish for printed circuit boards (PCBs) by releasing a standard with a large characterization data base [1,2]. This data and that generated by industry [3] generally concentrated only on the basic testing approaches and mostly for lead-free solders and testing of individual solder ball attachments rather than the advanced ball grid arrays (BGAs) electronic packaging assemblies and for tin-lead solder. It is extremely difficult to correlate test results from the shear of individual balls to the assemblies of BGAs. Reliability testing using BGA packages, especially land grid arrays, with tin-lead solder, is lacking. In addition, controversy exists regarding the reliability/compatibility of ENEPIG with tin-lead solder [4], as there are more consistent positive test results for the lead-free solder joints [5]. A hot air solder level (HASL) finish, which is commonly used for the tin-lead solder, lacks the flatness requirement for the fine pitch ball grid arrays (FBGAs).

The significance of the PCB surface finish on assembly reliability was recognized by the IPC 9701 standard team in its early development, when the team was narrowing the requirements for the tin-lead solder joint testing for the BGA packaging technologies. The team limited the use of the PCB finishes to solder preservative (OSP) and HASL in order to minimize the potential for premature failures by using other finishes. Such restriction was implemented to avoid significant cost and schedule burden on smaller facilities, which generally lack knowledge and experience on the nuances of unique surface finishes such as electroless nickel immersion gold (ENIG). This specification allowed unique surface finishes only for comparison to the baseline finish. The A revision, which also includes recommendations for Pb-free solders, allowed only the use of an OSP finish since the tin-lead HASL was not compatible to Pb-free solders. Other surface finishes including silver (Ag) and tin (Sn) were considered to be acceptable only for a manufacturer's internal data comparison. Also, an ENIG finish could be used for an internal data comparison; however, it was warned that the risk of introducing unintended brittle failure

(black pad) could occur. The ENEPIG was not introduced at this time; therefore, this specification does not discuss this specific surface finish.

With the industry implementation of Restriction of Hazardous Substances (RoHS), the use of a tin-lead HASL finish for PCB with excellent solderability and solder joint reliability has diminished even though this still is the dominant finish for high-reliability applications with tin-lead solder. The process consists of immersing PCB in a tin-lead alloy followed by solder removal by 'air knives', which blow hot air across the surface of the PCB. The lead-free HASL finish has gained some interest for RoHS use, but it suffers from increased copper dissolution and lacks the flatness requirement needed for finer pitch array packages. An electroless nickel immersion gold (ENIG) finish provides the flatness requirements with excellent solderability, but it suffers from the "black pad" potential failure and lacks gold wire bondability that is required for hybrid (wire and solder) technologies [6].

ENEPIG has provided the best solution for the black pad defect by depositing an additional layer of electroless palladium over nickel. The palladium is not etched away during the gold plating process so the potential for the oxidation of nickel (black pad) is eliminated. However, ENEPIG is more costly than ENIG. ENEPIG also provides excellent solder joint reliability for lead-free solder joints, but industry debates continue on its reliability with tin-lead solder assembly.

The IPC-4556 specification for ENEPIG is very comprehensive and includes a wealth of information. The thickness specification for ENEPIG specified as: (1) Nickel: 3 to 6 µm [118.1 to 236.2 µin], (2) Palladium: 0.05 to 0.15 µm [2 to 12 µin], and (3) Gold: A minimum thickness of 0.030 µm [1.2 µin]. All measurements to be taken on a nominal pad size of 1.5 mm x 1.5 mm [0.060 in x 0.060 in] or equivalent area. The new amendment sets an upper limit for the gold thickness at 2.8 µin (0.7 µm) in order to discourage requests for a much higher immersion gold value and avoid its negative effect on reliability. A higher gold thickness will increase dwell time in the gold bath resulting in nickel corrosion under the palladium layer.

This investigation addresses the reliability from an assembly perspective and more realistic thermal cycles and aging environmental conditions. ENEPIG is yet to be widely accepted for high-reliability applications with tin-lead solder assembly. First, technology trends for LGA are discussed followed by an example of the difficulty of reflow for HASL with PCB surface finish compared to ENEPIG finish. Then, briefly discussed is assembly on a PCB with ENEPIG finish using two advanced area array packages, one an LGA with 1156 solder joints and the other one with CLGA 1272 (ceramic LGA) LGAs. The LGAs were subjected to 200 thermal cycles (–55°C to 125°C). Optical and SEM photomicrographs showing solder interface conditions after 200 TC are presented and were compared to samples that were subject to additional 324 hours of aging at 125°C. Furthermore, these were compared to those that were subjected to an additional 100 thermal shock cycles (–65°C to 150°C). The paper concludes with a summary and recommendations for the next steps of investigation.

1.1 LGA and Advanced Packaging Trends

This paper focuses on the second-level (board-level) solder joint reliability and intermetallic formation of LGA1156. Figure 1 categorizes single-chip microelectronics packaging technologies into three key technologies [7-8]:

- Plastic ball grid arrays (PBGAs) including flip-chip die version (FCBGA), land grid array (LGA) with solder balls, quad flat no lead (QFN) and new versions
- Ceramic ball grid array (CBGA), ceramic column grid arrays (CGAs), and ceramic LGA version [9]
- Chip-scale packages, a smaller foot print versions of BGA and wafer level packages (WLPs.)

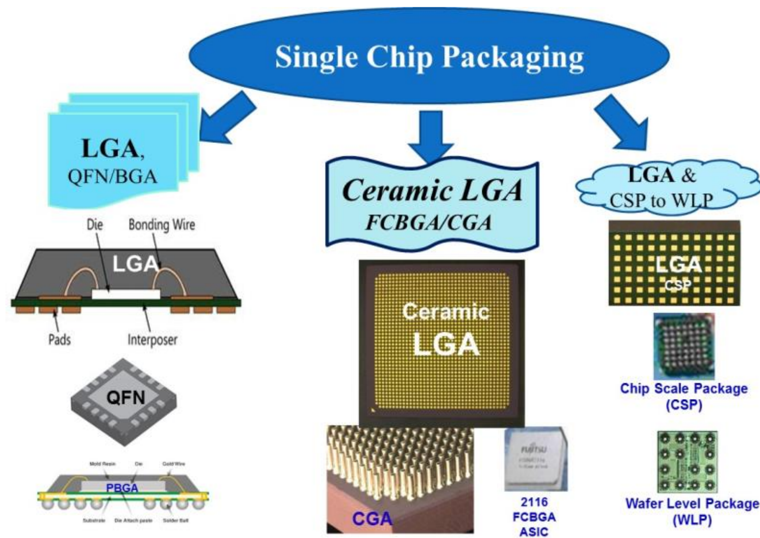

Fig. 1. Single chip packaging technologies covers three main categories. LGA exists in all three categories.

PBGAs and CSPs are now widely used for many commercial electronics applications, including portable and telecommunication products. BGAs with 0.8-1.27-mm pitches are implemented for high-reliability applications and generally demand more stringent thermal and mechanical cycling requirements. The plastic BGAs introduced in the late 1980s and implemented with great caution in the early 1990s, further evolved in the mid-1990s to the CSP (also known as a fine-pitch BGA) having a much finer pitch from 0.4 mm down to 0.3 mm. Recently, fan-out and fan-in wafer level packages have gained significant interest. LGA packages cover a range of counterpart packages from fine pitch CSP to large pitch and high I/O BGAs. Similar to ball array versions, LGAs are surface mountable.

There are no solder balls in LGAs, only land pattern terminations similar to QFNs. Interconnections are formed using solder paste and reflow during surface mount assembly — reducing the assembly height. This allows for a thinner assembly needed for mobile and computing products, especially the RF application that requires lower parasitic noise. .LGAs are the preferred packages for applications that require an ideal combination of low device sizes and profiles, and superior thermal and electrical performance. LGAs have negligible internal stray parasitic elements associated with their external solder pads and closeness to PCBs enable an extremely low thermal resistance to the device. This enables maximum heat transfer from the die to the package pads. However, thermal cycle reliability has an inverse exponential relationship with solder joint height. Therefore, there is a possible significant reduction in solder joint reliability. FEA modeling projects lower cycles-to-failure trends for LGAs compare to BGAs, which are also verified by testing [10].

1.2 HASL Finish Limitation for WLP1600, 0.3-mm Pitch

A test vehicle with various BGAs, sizes, and pitches was designed to determine assembly challenges in for mix pitch and sizes as well as their reliability. Two PCB surface finishes were considered; one standard tin-lead HASL and the other with ENEPIG. The most challenging packages for PCB surface finishes and assemblies were the following two sizes and pitches.

- Two FPBGAs with 0.4-mm pitch and 13-mm^2 body size. One of the CVBGA432 components had SnPb solder balls whereas the other had Pb-free SAC305 solder balls.
- Two daisy-chain WLPs with 0.3-mm pitch and 12-mm^2 body size. The WLP1600 had Pb-free SAC305 solder balls.

Figure 2 shows a section of the PCB that compares the images of daisy-chained pad patterns for ENEPIG and HASL. The baseline for the pitch of 1.00 mm is also included. The enlarged sections of WLP1600 are shown for both surface finish conditions illustrated irregularity in HASL, and regularity in ENEPIG surface finishes. The HASL shows solder shorts covering four pads. Even the solder dome formation is non-uniform. The ENEPIG finish, however, shows excellent consistency for 0.3-mm pitch and higher. So, the ENEPIG is a clear winner. For 0.4-mm pitch, the HASL finish is more consistent even though solder dome formation is still a common feature.

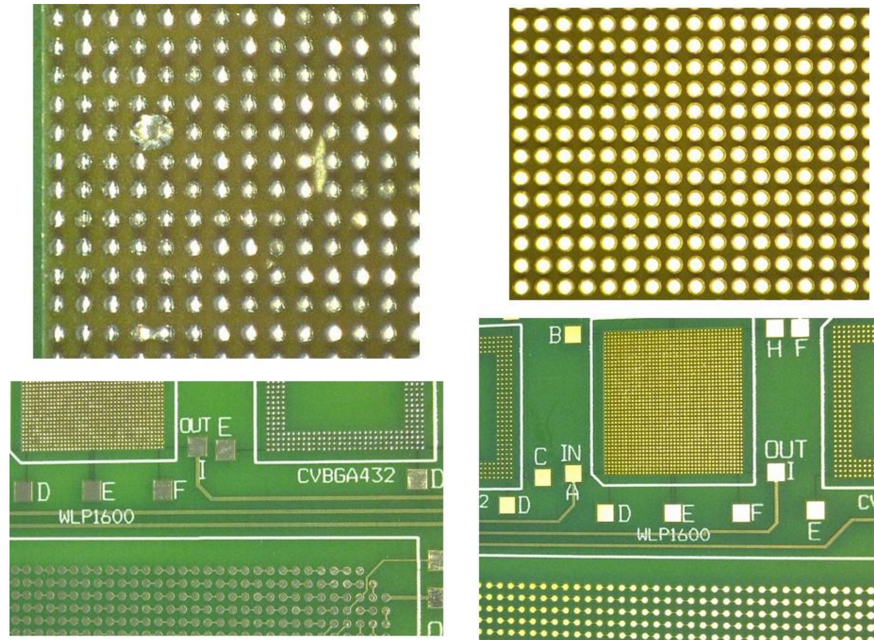

Fig. 2. The images of HASL (left) and ENEPIG (right) PCB finishes. The HASL finish is unacceptable for WLP1600 with 0.3-mm pitch, whereas ENEPIG is acceptable.

1.3 ENEPIG: LGA1156 Assembly and Inspection

To determine the effects of ENEPIG surface finish under a severe thermal stress condition, LGAs were used for assembly onto PCBs that also added additional manufacturing challenges. A printed circuit board was designed to accommodate a plastic LGA1156 package, as well other packages that are beyond the scope of this paper. The ENEPIG thicknesses were defined per IPC-4556, Jan. 2013 release, electroless Ni 118- 236 μin, electroless Pd 2-12 μin, and Immersion Au 1.2 μin minimum.

The LGA1156 had daisy-chain patterns for checking opens after assembly and for opens during the reliability evaluation. High I/O LGA daisy-chain patterns on ENEPIG PCB finish not only enabled solder joint reliability evaluation, it also provided another verification method for the condition of interconnections after assembly. The PCB daisy-chain patterns were designed to match LGA designed packages to make a complete resistance loop after the package was assembled onto the PCB. Three key parameters were evaluated before being ready to commit to a larger number of assemblies for reliability evaluation.

Generally, after LGA1156 and PCB were baked for moisture removal, tin-lead eutectic solder paste was applied on LGA1156 pads and were reflowed to form solder domes on their pad. Ceramic packages were required to repeat the process in order to achieve the desired height of solder dome. After solder paste application on the PCB pads, the LGA1156 was placed onto the PCB and prepared for assembly. Figure 3 shows a photo of the bumped plastic and ceramic LGAs (1156 and 1272 I/Os) and the final assembly. The test vehicle was assembled using a vapor-phase reflow machine.

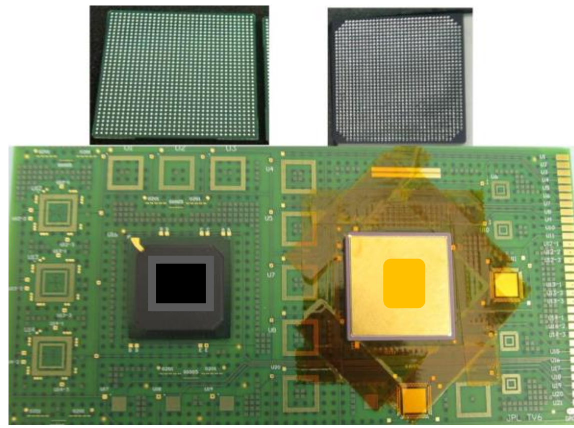

Figure 3. ENEPIG PCB surface finish for the assembly of plastic land grid array (LGA) with 1156 pads (left top) and ceramic LGA (right top). LGA1156 with ceramic version were assembled onto ENEPIG PCB finish (bottom).

The real time 2D X-ray of the two package assemblies revealed no shorts or excessive solder balling and are considered to be acceptable. This build was repeated one more time and achieved acceptable quality results. Figure 4 shows the overall X-ray of the side with the LGA1156. It also shows the corner solder joints at a higher magnification. The X-ray shows the internal configurations of the LGA and the fine pitch packages. During real time examination of the X-ray images at higher magnifications, there were no apparent unusual solder anomalies except the existence of large voids.

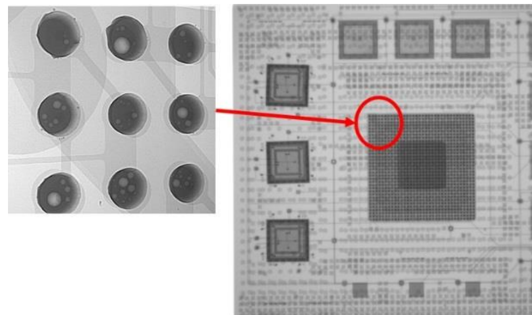

Fig. 4. X-ray photomicrograph images of a section of a test vehicle with plastic LGA1156 showing solder joint voids.

1.4 ENEPIG Microstructure after 200 TC (– 55C/+125°C) for LGA1156

LGA1156 assemblies on ENEPIG finished PCB were subjected to thermal cycling followed by isothermal aging prior to cross-sectioning for microstructural changes. LGA1156 assemblies were subjected to thermal cycling in the range of –55°C to +125°C with a 2° to 5°C/min (target 3°C/min) heating/cooling rate. After 200 thermal cycles, one of the LGA packages was cut in half diagonally for cross-sectioning. Figure 5 shows cross-sectional images of a LGA1156 with the package dimensional values including die size, die thickness, and solder joint height length. Images include both optical and scanning electron microscopy (SEM). The die size relative to the package, is a critical parameter that affects reliability as well as solders under the corner die.

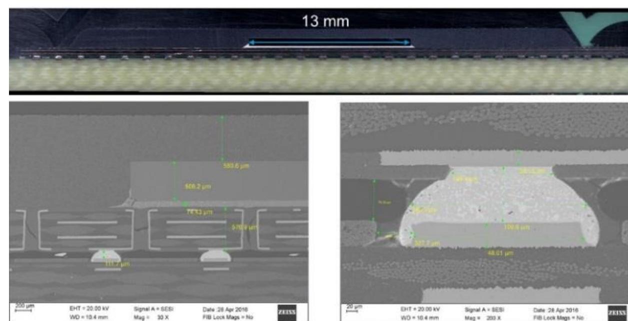

Fig. 5. Representative photomicrographs of LGA1156 after thermal cycling showing die size relative to the package.

Figure 6 shows representative optical and SEM images at high magnification providing details on microstructural features after 200 thermal cycles (–55°C to +125°C). The observation of no cracks confirms the result from the daisy-chain resistance measurement that also showed no increase in resistance after 200 thermal cycles. Generally, more than 20% resistance increases, within a short time increasing to mega ohm resistance, are associated with cracking and opens in the solder joints.

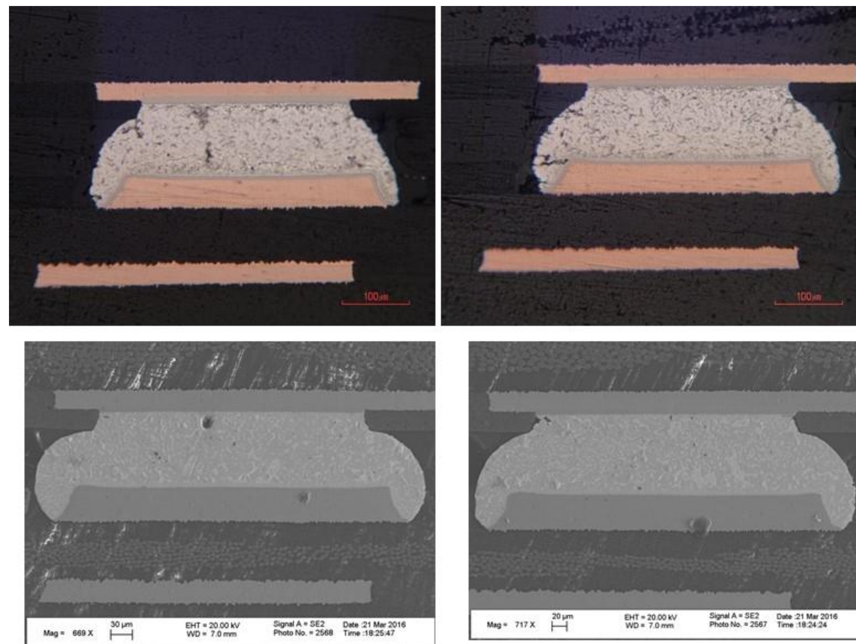

Fig. 6. Representative optical and SEM images of LGA1156 solder joints at 200 thermal cycles (–55°C to 125°C). Acceptable LGA solder joint quality with non-solder mask defined (NSMD) or pad defined configurations are also apparent.

Characterization of the solder/ENEPIG interface is critical to be established after cycling, but before a subsequent isothermal aging for comparison. Figure 7 illustrates representative SEM images with SEM EDX/EDS (energy dispersive x-ray) elemental analysis (e.g., showing existence of Ni, Cu, Sn, and Pb) at the solder interface after 200 thermal cycles (–55°C to +125°C).

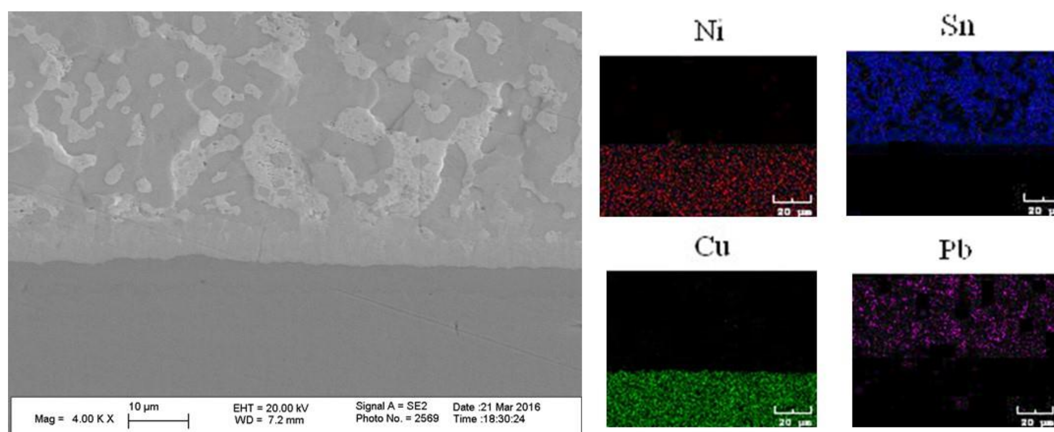

Fig. 7. Representative SEM images with SEM EDS elemental analysis (e.g., showing existence of Ni, Cu, Sn, and Pb) at the solder interface after 200 thermal cycles (–55°C to +125°C).

1.5 200 TC (– 55°C/+125°C) + 324 hr Aging (125°C) for LGA1156

To determine microstructural changes due to isothermal aging, thermally cycled LGA1156, as well as the half of the unused samples from the microsectioned parts were subjected to isothermal aging at 125°C for 324 hours. A section from the cut sample was purposely used in order to eliminate the contribution of manufacturing variables on the ENEPIG/solder interface intermetallic growth. This enabled only the contribution of isothermal aging for direct comparison of the microstructural changes at the interface before and after aging. Note that this approach cannot be used for thermal cycling since half of the package induced a different CTE mismatch than a full size assembled package. The test results could not have captured the effect of the CTE mismatches. Figure 8 compares representative SEM images of samples before and after isothermal aging. No significant changes appear at this magnification due to the additional 324 hr isothermal aging.

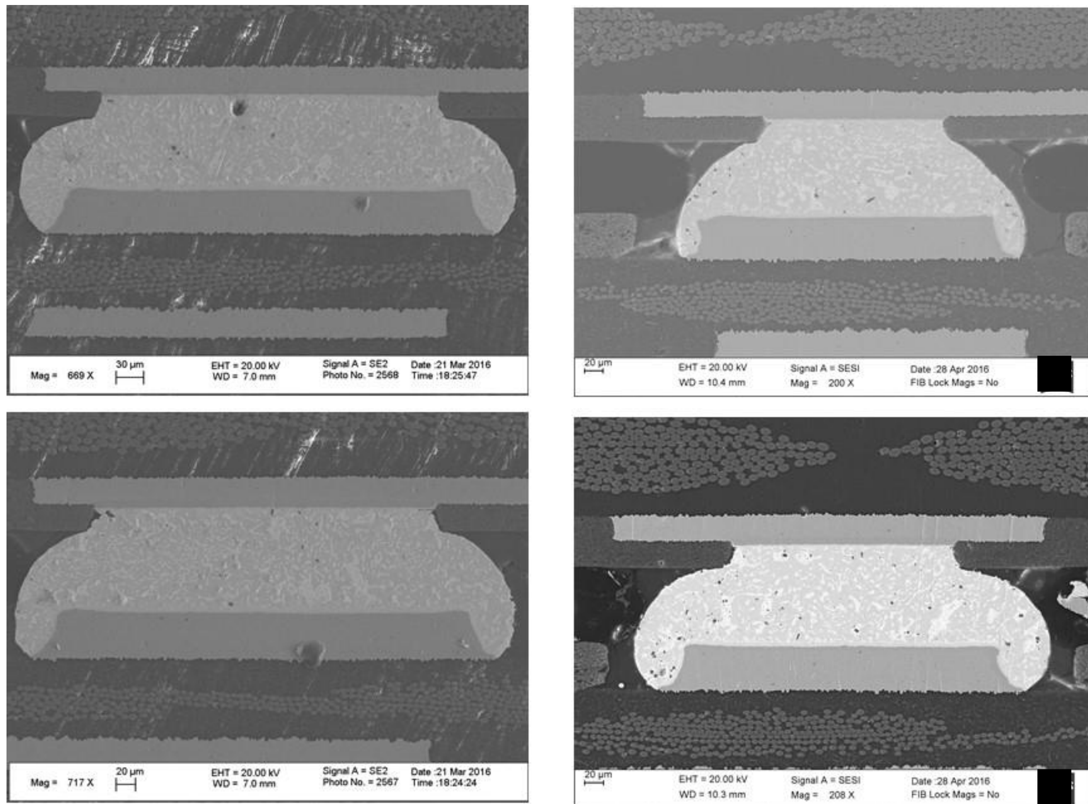

Figure 8. Representative SEM photomicrographs of LGA1156 solder conditions under the die after 200 thermal cycles (–55°C/+125°C), (left), and after subsequent 324 hours of isothermal aging at 125°C (right). Samples were the same— half used after TC— and the other half was used for subsequent aging, polishing, and SEM imaging.

Higher magnification was required to determine microstructural changes at the solder/ENEPIG interface. Figure 9 compares the higher magnification SEM images after 200 TC and after additional 324 hours of aging. It also includes the EDX/EDS elemental mapping analyses performed at the solder/ENEPIG interface showing the key elements to be tin and lead distribution. Grain growth is apparent, which is normal for aging. There is no abrupt change due to isothermal aging.

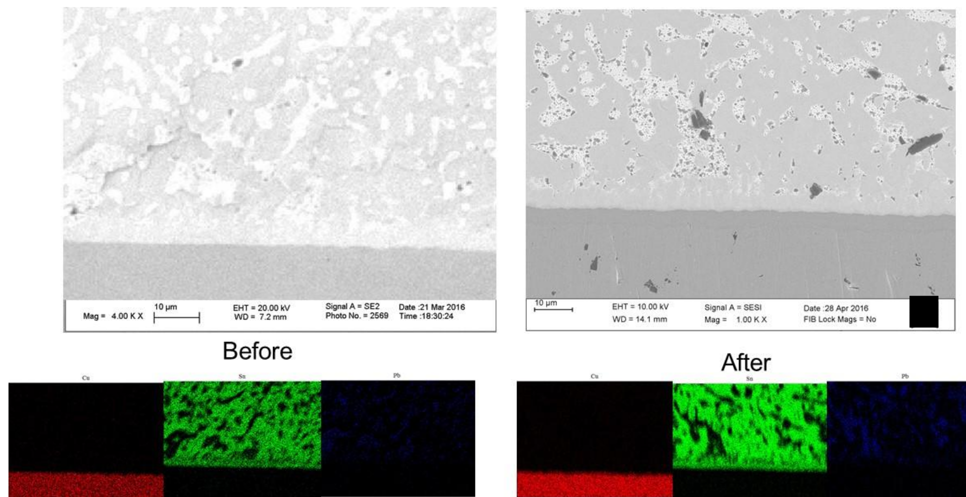

Fig. 9. Representative SEM photomicrographs with EDS elemental analysis of LGA1156 solder conditions after 200 thermal cycles (–55°C/+125°C), left, and after subsequent 324 hours of isothermal aging at 125°C (right). Samples were the same—half used after TC—and another half used for subsequent aging, polishing, and SEM imaging, and elemental analysis.

1.6 200 TC (– 55°C/+125°C) + 100 TS (– 65°C/+150°C) for LGA1156

To determine the effect of higher temperature cycling ranges on interface microstructural changes, the thermally cycled LGA1156 assemblies (200 TC cycles, –55°C/+125°C) were subjected to 100 more severe thermal shock cycles (TS, –65°C/+150°C). Contrary to the thermal cycle condition, which was performed in one chamber, the thermal shock cycle used two chambers and test vehicles were shuttled between the hot and cold chambers. A representative thermal cycle profile is shown in Figure 10. Only three TVs were subjected to this thermal shock cycle regime. All TVs failed between 20 and 60 cycles, but continued to 100 TS to possibly cause further opening of the solder joints. The one with an open after 60 TS was selected for cross-sectioning and the microstructural evaluation of solder and ENEPIG interface.

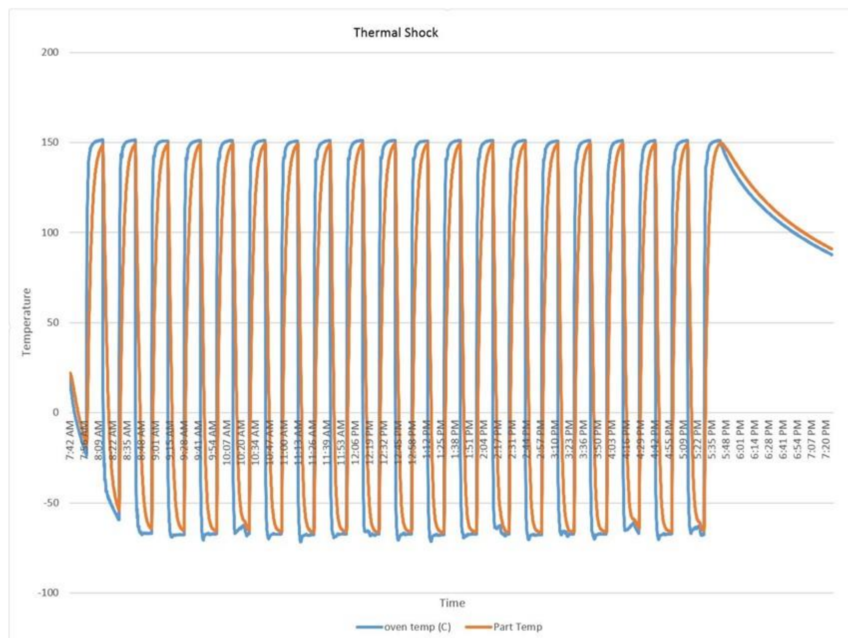

Fig. 10. A representative thermal shock cycle profile (– 65°C/+150°C).

Figure 11 shows representative SEM images of the LGA assembly after 200 TC +100 TS. The cross sections cover the areas with microvia, which was one layer down to provide daisy-chain pairs for continuity test. Figure 12 shows the SEM microstructure with EDS elemental analysis detailing the microstructural changes at the solder/ENEPIG interface.

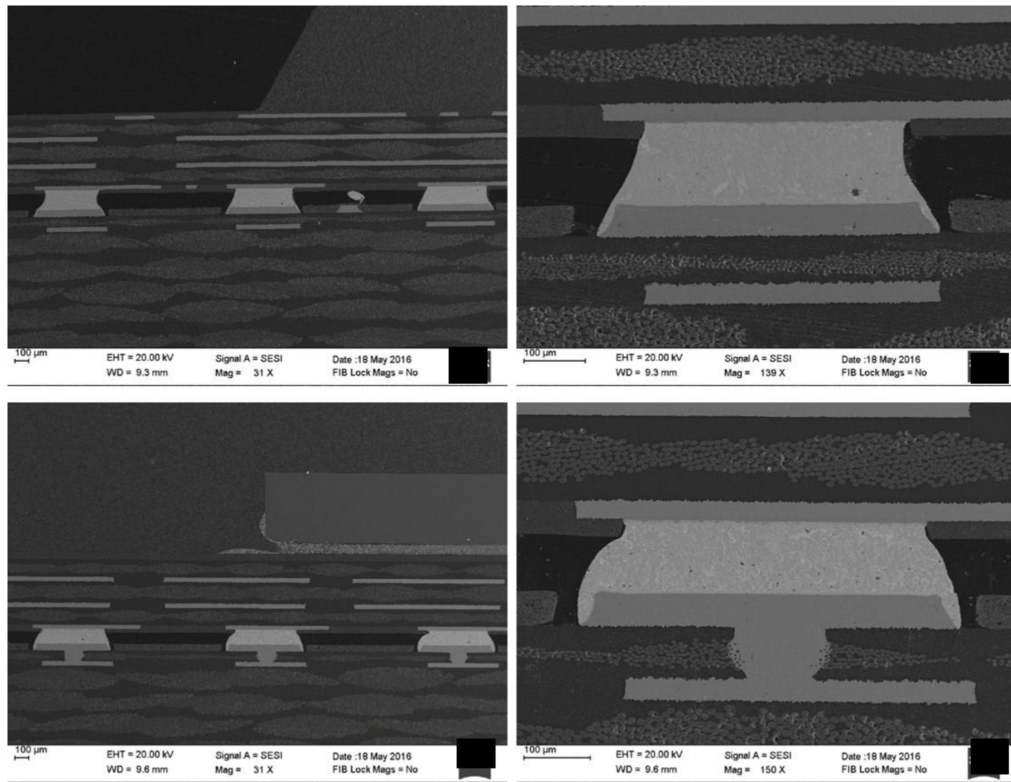

Figure 11. Representative SEM photomicrograph images of LGA1156 solder conditions under the die and over the via after 200 thermal cycles (–55°C/+125°C) and an additional 100 thermal shock cycles (–65°C/+150°C).

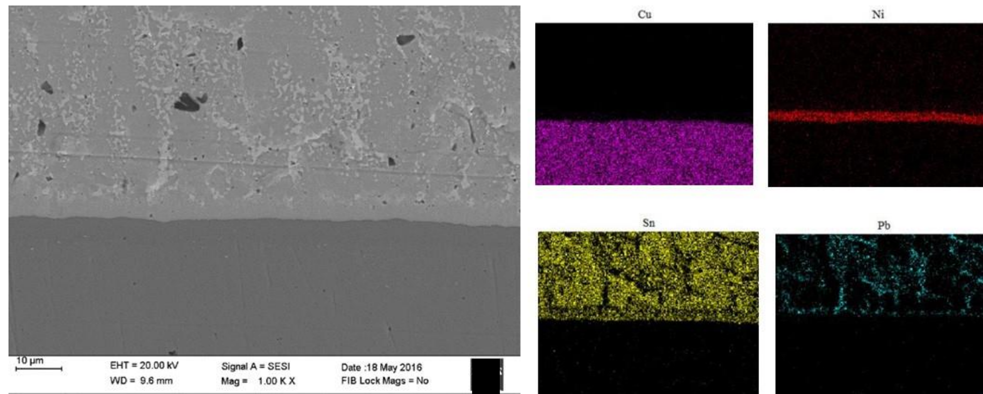

Fig. 12. Representative SEM photomicrographs image with EDS elemental analysis of LGA1156 solder conditions after 200 thermal cycles (–55°C/+125°C) and an additional 100 thermal shock cycles (–65°C/+150°C).

Finally, three SEM images, with their EDS elemental analyses, comparing the effect of additional aging and thermal shock cycles are shown in Figure 13. They cover SEM images after 200TC, after 200 TC plus 324 hours of aging at 125C, and after 200TC plus 100TS. No apparent anomalies were observed.

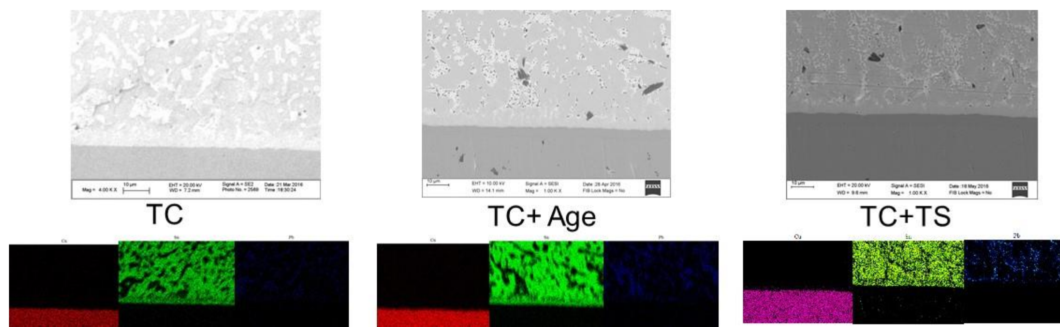

Fig. 13. Representative SEM photomicrographs images with EDS elemental analysis of LGA1156 solder conditions after 200 thermal cycles (TC, –55°C/+125°C), (left), 200 TC plus 324 hours aging at 125°C (middle), and a 200TC plus 100 thermal shock cycles (–65°C/+150°C), right.

2.0 SUMMARY

ENEPIG PCB surface finish reliability characteristics for RoHS solder joint assemblies have been the subject of numerous papers showing favorable results. However, reliability data for tin-lead solder is scarce — sometimes showing negative effects on reliability. This paper addressed the ENEPIG with tin-lead for high reliability electronics hardware to see if there were any apparent issues. For this reason, a number of accelerated thermal cycles and shocks along with isothermal aging were performed using the LGA1156 assemblies to determine the integrity of the solder/ENEPIG interface after each environmental exposure. A summary of findings is listed below:

- After 200 thermal cycles (TC, –55°C to +125°C), no failures were detected by daisy-chain monitoring and no microstructural anomalies occurred at the ENEPIG/ solder interfaces
- After 200 TC plus 324 hr of aging at 125°C, the ENEPIG/solder microstructural changes at the interfaces were within normal expectations
- After 200TC plus 100 thermal shock cycles (TS, –65°C to +150°C), the LGA1156 assemblies failed in the daisy-chains showing resistance opens, but no significant degradations were detected at the ENEPIG/solder interfaces by cross-sectioning and SEM elemental evaluation

The preliminary test results showed the acceptance of the ENEPIG PCB finish with tin-lead solder for short-term duration in high-reliability applications. It also revealed the short-term thermal cycle reliability acceptability of LGA1156 assemblies under standard harsh TC (–55°C to +125°C), but not under a more severe thermal shock cycle (TS, –65°C to +150°C).

3.0 ACKNOWLEDGMENTS

The research described in this publication is being conducted at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Copyright 2016 California Institute of Technology. U.S. Government sponsorship acknowledged.

The author would like to acknowledge the support of the team in this work, especially D. Hunter, A. Mehta, and E. Bradford. The author also extends his appreciation to the program managers of the National Aeronautics and Space Administration Electronics Parts and Packaging (NEPP) Program.

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