

Realization of a New Concept for Power Chip Embedding

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Abstract:

Embedded components technology has launched its implementation in volume products demanding high levels of miniaturization. Small modules with embedded dies and passive components on the top side are mounted in hand held devices. Smartphones have been the enablers for this new technology using the capabilities of embedded components. With this technological background another business field became interesting for embedded components – the embedded power electronics. The roadmap of the automotive industry shows a clear demand for miniaturized power electronic applications. Drivers are the regulations for the international fleet emissions which are focusing on three major trends.

The first trend will be higher efficiency of “classic” internal combustion engines, the second will be the efficiency of body application and the last trend will be the electrification of the drive train. For all targets a huge potential for embedded power electronics is visible. A European project was launched in 2013 as a development project for new power packages and power modules using die embedding technology. For the realization of this technology, copper termination on MOSFETs, IGBTs and power diodes is necessary. Equipment and processes have been developed in the supply chain to support the development of power modules ranging from 500 W to 50 kW. For enhanced thermal performance of power modules, a concept for double sided cooling has been developed. Beside full area contacting the MOSFET on the drain side with copper and contacting the embedded components in a power core with an isolated metal substrate with silver sinter paste, a very effective concept for reducing thermal resistances and stray inductance was shown. With the realization of the 500W demonstrator the proof of concept was realized. This paper will focus on the behavior of the power module for operational conditions of a PedEleC (Pedal Electric Cycle) application. The full reliability evaluation (thermal shock test, reflow test and power cycling) and switching behavior was shown. Furthermore, the thermal properties of the PedEleC power module were verified with the results from thermal simulation. In addition, more detailed investigation of the electrical properties before and after reliability treatment of a single chip test vehicle was shown.

Keywords: power embedding, PCB technology, miniaturization, automotive requirement, electro mobility

1. Introduction – Embedded power modules

The large number of automobiles on today’s roads will continue to cause serious problems for the environment and human health. The main issues are the air pollution (CO₂ emission), global warming and also the rapid depletion of petroleum resources [1].

To address these problems, the research and development activities related to transportation have moved in recent years toward developing electric and hybrid vehicles. By combining an internal combustion engine and an electric motor and optimizing the load sharing according to the driving conditions, the hybrid systems achieve improved fuel economy. Hybrid electric vehicles are currently the most fuel-efficient cars. During acceleration, the motor assists the engine, while during deceleration, regenerative braking acts to charge the battery to improve the fuel efficiency [2].

For driving with an electric or hybrid vehicle, a system is needed to convert the power, which is generated by the engine, into electrical energy. The converted energy is used to charge and discharge the battery and to drive the motor [3]. The power module has to deal with high currents, voltages and temperatures for the application in an electric vehicle in comparison to commercial applications.

Future applications are expected to deal with increased functionality and power. A higher amount of chips, wire bonds and interconnection structures is needed. This can cause two major issues. Bond wires cause too high stray inductance which influences the switching behavior. Higher power will cause increased heat during the operating time. Therefore, a special heat management concept is needed.

A promising concept to handle these requirements is the power embedding technology. Advantages of this technology are the size reduction for smaller and lighter construction, lower inductance circuit concept (offers higher voltages or higher power density), good heat dissipation and increased reliability.

2. Power electronics in automotive applications

2.1 Drivers for embedding technology in automotive applications

The typical conditions at a TCU (Transmission Control Unit) location are very harsh. The customer requires high complexity and increased functionality concurrent with mechanical restriction due to size. Besides high application temperatures above 150 °C and high vibration load, direct contact with aggressive media can be needed. For automotive

applications a lifetime of 15 years and 8000 operating hours is today's standard, for plug in hybrid functionalities at least 27000 hours are expected. The cost aspect is always a main driver of the developments.

For all these requirements, the embedding technology offers a solution to fulfill the customer wishes. Embedding has a high miniaturization potential on all levels by functional integration starting at the components, over the substrates to the whole system. Thermal, electrical and reliability performance can be increased due to the concept of integration of the components (encapsulation of components) and a direct copper-copper-interconnection. By evaluation of the cost potential a direct comparison between conventional substrate solutions and the embedded one is not recommended. But by minimizing also the full system due to substrate size reduction or replacement of a two-substrate solution with a single substrate solution (additional assembly area), a cost reduction potential at the system level is expected.

3. Development topics

During the project, power modules based on a new embedding concept have been developed. The components are embedded in a so-called power core and can be integrated in a new concept to create power modules.

This new embedding concept was designed to use a double sided thermal management concept. Besides this, it was expected to support space requirements by providing additional miniaturization. Furthermore, better electrical performance and higher reliability was expected.

Main achievements of the project are mentioned below:

- Technology and process development for power core with embedded thinned power semiconductors and the material evaluation for highly reliable products.
- Process and interface development for interconnection of IMS (Insulated metal substrate - thin copper, isolation layer, thick copper) PCB with power core by new sinter-lamination-process to build up the final power module.
- Thermo-mechanical evaluation and simulation of the power module and optimization for high reliability.
- Evaluation of embedded modules compared to existing solution to evaluate the potential and benefits of the embedding concept.

3.1 Applications

During the project several demonstrators have been realized. Besides evaluating the electrical and thermal performance of a single chip demonstrator, a power and a logic module for a PedEleC application was realized. This application for low power consumption is based on MOSFETs B6 topology as shown in Figure 1. Furthermore, thermal management and low space requirements have been considered. The system design depends on end user requirements and specification, which includes electrical and thermal performance, reliability and mechanical requirements.

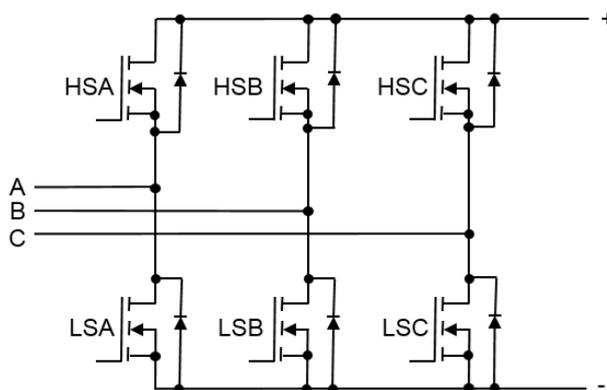


Figure 1: B6 topology with MOSFETs (A, B, C: phases, HS: High side, LS: Low side)

The embedding concept allows a very close positioning of the single components to each other, which results also in a minimization of the inductance of the switching cell. This leads to a reduction of the overvoltage during the switching of the power semiconductors and finally a faster switching is possible.

3.2 Embedding concept

The principal build-up of the new embedding concept is shown in Figure 2.

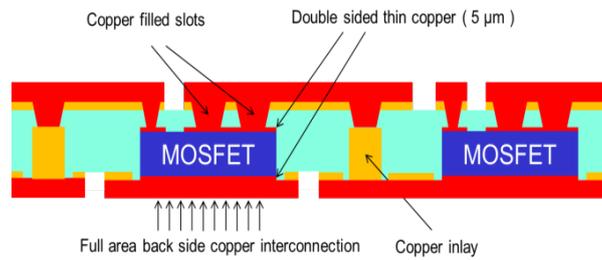


Figure 2: Principle concept of power module

First of all, thinned bare die copper terminated power semiconductors are integrated in an organic substrate (glass fiber reinforced epoxy resin) by a lamination process. The interconnection of the top side contacts was realized with copper filled μ Via technology. The back side of the components is connected by full area galvanic copper. This is the principal set up for the embedded power core.

For the build-up of the embedded power module IMS have been silver sintered on the top and bottom side of the power core. To protect the sinter layer and for a better mechanical stability, a combined lamination process is used to fill the gaps between the sinter depots with resin from the PCB prepreg.

The final module is shown in Figure 3 and a cross section in Figure 4.

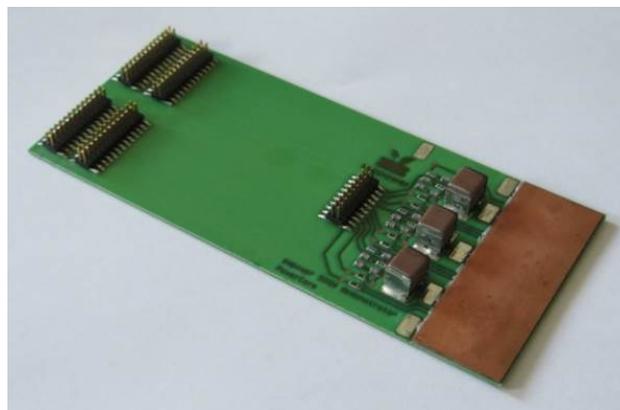


Figure 3: Power module with embedded MOSFETs, IMS and assembled passive components and connectors



Figure 4: Cross section of power module with embedded MOSFETs

3.3 Benefits of the embedding technology concept

During investigations and the evaluation of the results, the embedding technology shows high potential regarding miniaturization, electrical and thermal performance as well as reliability aspects. The potential has been evaluated on the 500 W power demonstrator in comparison to a benchmark module which uses conventional PCB technology with SMT mounted packaged components (see Figure 5). Due to the lower power of this module, organic substrate technology can be used.

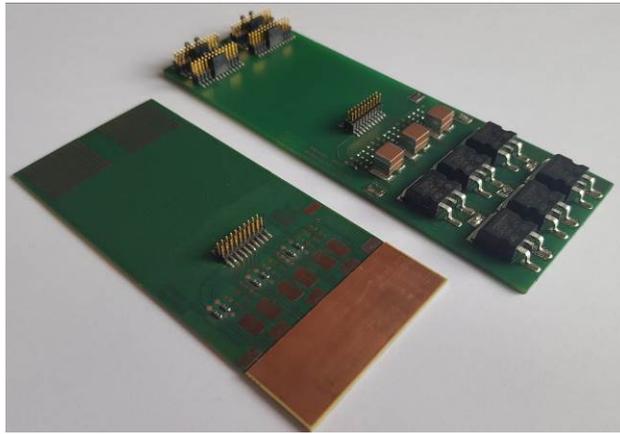


Figure 5: Modules for testing and benchmark (Front: embedded module, Back: SMT benchmark module)

Miniaturization potential: By comparison of the SMT benchmark module and the embedded module a size reduction of around 20% can be reached (see Figure 6). This is the size reduction potential of the full modules. By evaluation of the miniaturization regarding the active area (power component area), a size reduction of around 50 % can be realized. The active area is marked in yellow in Figure 6. This is a huge reduction of the size. The size reduction potential seems to be less by comparison of embedding technology with DCB (Direct Copper Bonded) and bare die technology, because the bare die technology has also the potential to miniaturize the substrate due to their smaller footprint. But also in a theoretical evaluation of the size reduction potential between these two technologies, a decrease of the substrate of around 25 % seems to be possible.

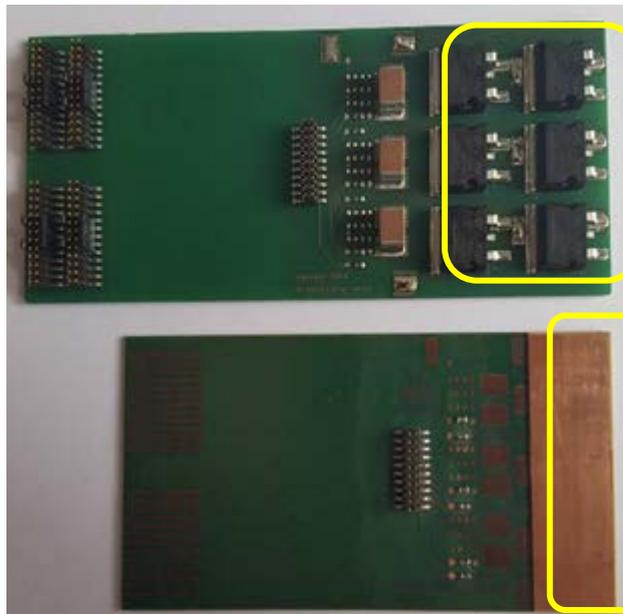


Figure 6: SMT benchmark module in comparison to embedded module for demonstration of miniaturization potential (active area with MOSFETs marked in yellow)

Electrical performance: For the characterization of the switching behavior of the demonstrator, a double-pulse-measurement is an established method. By means of two pulses, switch current can be set, and the current and voltage waveforms are recorded during a shift. The first pulse is used for precise adjustment of the switch current and the measurement is carried out during the second pulse.

For a comparison and evaluation of the electrical performance of the embedded modules, the benchmark module was also tested. Figure 7 shows the switching off behavior of the SMT benchmark module and Figure 8 of the embedded module.

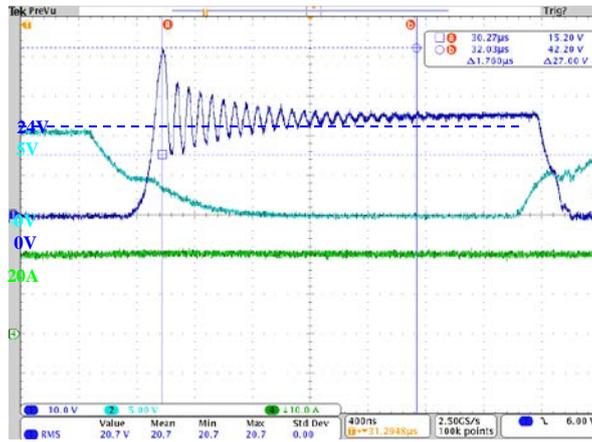


Figure 7: Switch off behavior of SMT benchmark module with a gate resistance of 51Ω (Green: Phase current (20A), Light blue: Gate voltage (5V), Blue: Drain Source voltage (24V))

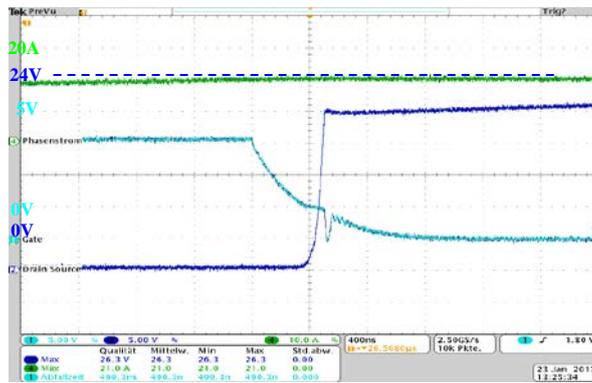


Figure 8: Switch off behavior of embedded module with a gate resistance of 51Ω (Green: Phase current (20A), Light blue: Gate voltage (5V), Blue: Drain Source voltage (24V))

In general, the embedded modules show good switching behavior, especially in comparison to the SMT benchmark module. This is realized by the possibility to design low inductive layouts for embedded circuits (short paths). The overvoltage and the swinging of the Drain-Source voltage can be reduced (Blue line in Figure 7 and Figure 8) which results in less switching losses and provides a low inductive setup. By reducing the switching losses, the switching on and off time can also be reduced, and a faster switching is possible.

Thermal performance

The benchmark between the SMD mounted module and embedded module shows significant differences on thermal resistances illustrated in Table 1. In the case of double sided cooling, the measured value of a thermal resistance is about 30% compared to the SMD version. Due to the different heat path, where the heat has to flow through the lead frame and the PCB, the thermal resistance is much higher compared to the embedded module, where the heat flows directly from both surfaces of the MOSFET to the heat sink via vertical silver sinter interconnects.

Table 1: Measured values of thermal resistance

Transistor connection	Q2 A/L1	Q4 A/L2	Q6 A/L3	Q1 B/L1	Q3 B/L2	Q5 B/L3	Average
SMT Module (benchmark)	4,40	4,35	4,57	4,39	5,79	5,49	4,83
Top-side cooling	2,42	2,09	2,45	2,17	2,49	2,74	2,39
Bottom-side cooling	1,50	1,45	1,61	1,59	2,01	2,15	1,72
Double-side cooling	1,22	1,28	1,33	1,29	1,78	1,99	1,48

Reflow stability: To guarantee the following assembly process by soldering, the reflow stability of the embedded setup must be given. A typical reflow test for SMT assembly was performed three times on the modules. After testing the electrical functionality, cross sections have been done to analyze the interconnection structures in the module. It was focused on the Gate connection, the Source connection and the Drain connection. Furthermore, the adhesion of the PCB base material on the surface of the semiconductor was evaluated, as well as the silver sinter interconnection.

Figure 9 shows the Source contact area of the MOSFET. The Source pad connection and the backside full area connection show a reliable structure. No delamination from the surface of the MOSFET can be identified. The sinter interconnection of the IMS on the top and the bottom side of the power core shows no cracks or delamination.

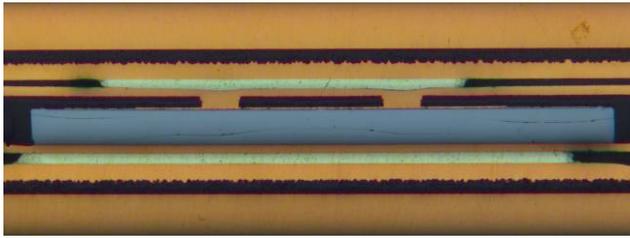


Figure 9: Cross section of MOSFET after three times reflow (Source contact area)

In Figure 10 the Gate connection is shown. Like before, a reliable interconnection can be seen and no delamination between base material and semiconductor or cracks in the base material have been created during the reflow test.

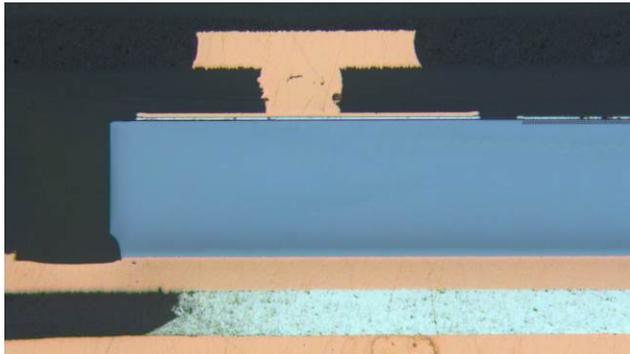


Figure 10: Cross section of MOSFET: Gate contact area after three times reflow

Thermal shock test (TST): For evaluation of the thermo-mechanical stability of the interconnection structures, a thermal shock test was performed (-40 °C/+150 °C). The functionality of the modules was tested by measuring the thermal resistance of each MOSFET. This was done by using the reverse diode, so the MOSFET itself has been used as a heater. The parameters of the thermal shock test are shown in Table 2.

Table 2: Parameters of Thermal Shock Test

TST	Description
Chamber	Two chamber designs (hot and cold)
Chamber parameters	Cold: -40°C, Hot: +150°C Dwell time: 15 min Duration: 1000 cycles
Measurement system	After each 250 cycles measurement of the thermal resistance
Tested structure	B6 bridge with embedded MOSFETs
Pass/Fail criteria	No significant increase of thermal resistance, no delamination and cracks within PCB

The results of the thermal resistance measurements are shown in Figure 11. No significant increase of the thermal resistance are indicated. The difference between the high side (HS) and the low side (LS) MOSFETs is caused by the layout. The low side FET cooling is worse than the high side one (configuration of MOSFETs in the layout and the resulting electrical and thermal paths). The variation of the thermal resistance is in the measurement tolerance of ±5%.

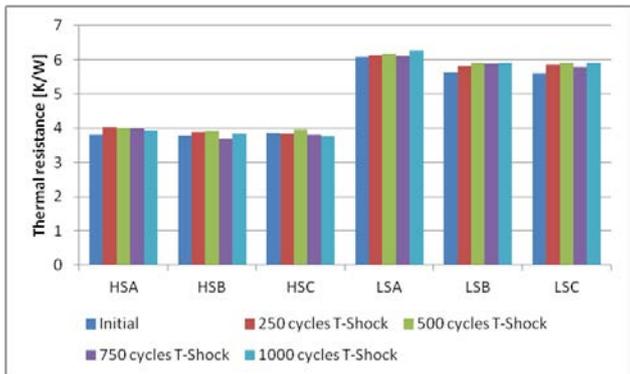


Figure 11: Results of thermal resistance measurement during TST

The Gate connection is the smallest structure in the setup and from mechanical aspects the most critical. But it also shows a good interconnection after 1000 thermal shocks, as it can be seen in Figure 12.

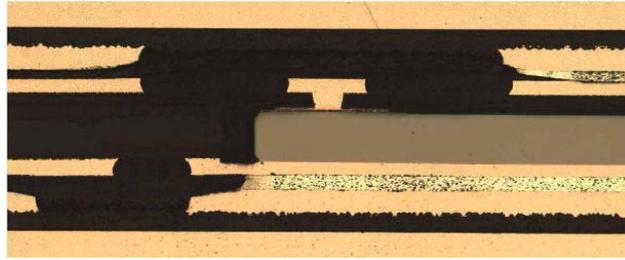


Figure 12: Cross section of Gate contact of embedded MOSFET after 1000 thermal shocks

Power cycling of power module – B6 bridge

First power cycling tests are performed at the module level. The test setup is illustrated in Figure 13 and 14. The high current connection is made to the common drain connection of the high and low side FETs and the short-circuited phase connection of the module. By that, the high and low side FET will operate in parallel mode during the test.



Figure 13: Power cycling tester

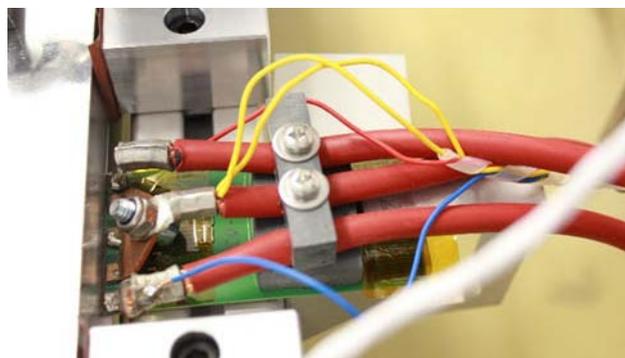


Figure 14: Power cycling test setup

For monitoring the junction temperature during the active power cycling, the internal reverse diode is calibrated at different temperatures prior to starting the test as a standard procedure. The goal is to realize a temperature swing of 100 K with each active cycle. A duration of 3s heating is required followed by cooling down to 20°C, which is realized by switching off the current for 6s. It needs to be mentioned, that due to the configuration of the module the high side dies only realize a temperature swing of 60 K whereas the low side dies reach 100 K. This effect is caused by the configuration of the FETs in the module and the resulting different thermal paths.

The test criteria was, that an increase of the forward voltage of 20% is defined as a module failure. The test was stopped after 300000 active power cycles without any noticeable increase of the forward voltage.

3.4 The single chip test vehicle

The aim of the single chip test vehicle was to evaluate the new embedding technology using a MOSFET in the so-called power core with full area connection of the drain in a conventional multilayer. This multilayer, a 6-layer PCB with thick copper layers should simulate a 48V automotive power application. More details of the construction can be seen in Figure 15.

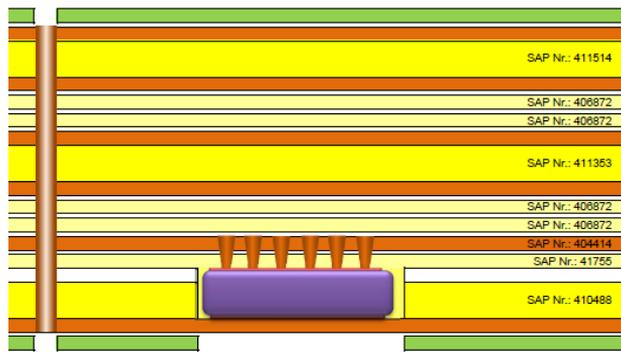


Figure 15: Buildup of single chip test vehicle

For the power supply, press fit connectors were used which can handle up to 1 kA to simulate the automotive conditions. With the new construction, highly effective cooling of the MOSFET was enabled by soldering the bottom side of the test vehicle to a heat sink for optimal test conditions. Furthermore, sensing lines were located directly on the MOSFET at different positions to measure the exact voltage for R_{DSon} calculation and measurement of the voltage drop on connectors. Figure 16 shows the embedded die in the power core which is a part of the 6-layer test vehicle. On the top side of the MOSFET the micro via connections of the big source pad and the smaller gate pad can be seen.

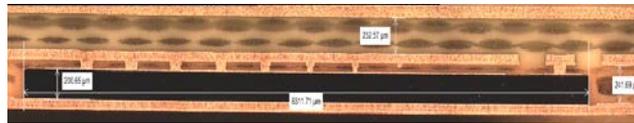


Figure 16: Cross section of the power core

A further aim of the evaluation was the comparison of the electrical parameters of the new concept with embedded MOSFET with a conventional concept using MOSFETs in molded packages mounted on the multilayer board. The focus was the comparison of the embedded die with the molded package. The most important parameters for a static evaluation are resistance, capacitance and leakage currents. These parameters were measured on the board as received from production and after the TST test for 1000 cycles $-55^{\circ}\text{C} / 150^{\circ}\text{C}$.

R_{DSon} measurement over current shows a small reduction on the embedded die construction compared with the data sheet of the molded package. The reduction of the electrical resistance is achieved by the usage of a grid of micro via which are connecting the source pad and a thick copper plane which is connected to the micro via instead of using wire bonds or copper clips in the molding package. After TST a small increase of the R_{DSon} of 1.6 % can be seen as an effect of thermal ageing. Figure 17 and 18 show the graphs of R_{DSon} over current.

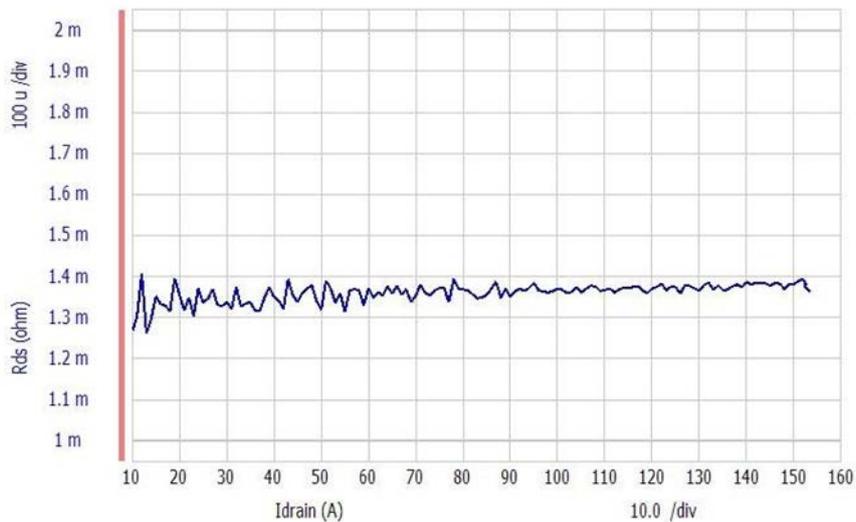


Figure 17: R_{DSon} of embedded MOSFET

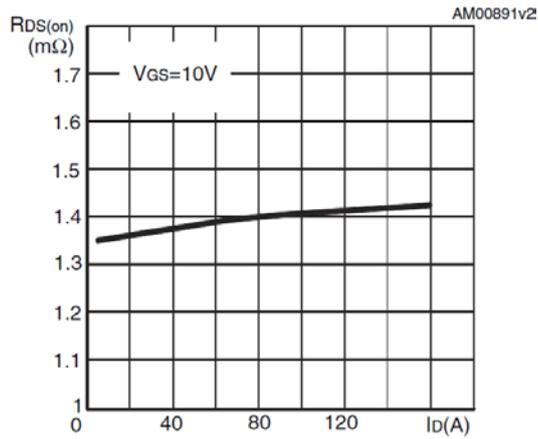


Figure 18: Datasheet of molded package

The influence of the packaging technology on the capacitance of the MOSFET was the next topic. Input capacitance, output capacitance and reverse transfer capacitance of the packed die was evaluated, and the definitions are shown in Figure 19.

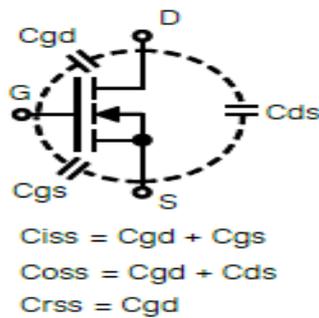


Figure 19: Definitions of capacitances for a MOSFET

All measurements have been done with a power device analyzer at a range of 0 - 40V level. The results from the embedded version and the commercial available components have been very similar, even after the TST treatment of the embedded die in the power core with no significant deviations from the initial measurements seen. Figures 20 and 21 show the measured input, output and reverse transfer capacitance.

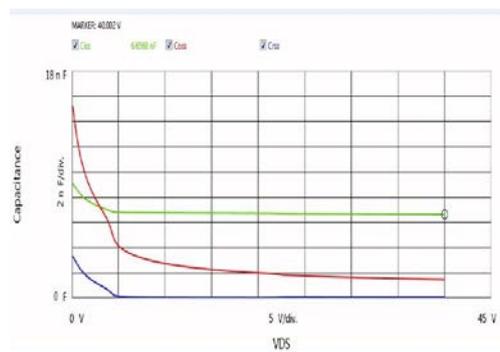


Figure 20: C_{iss} , C_{oss} , C_{rss} of embedded MOSFET

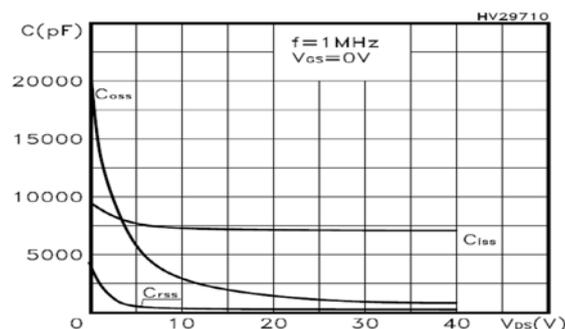


Figure 21: C_{iss} , C_{oss} , C_{rss} of molded Package

The third parameter which was evaluated with the power analyzer was the leakage current of the 40V MOSFET embedded in the single chip test vehicle. The drain-source leakage current I_{DSS} was typical at 2 nA and increased to 5 nA after TST treatment. The maximum specified current of the molded package is 10 μ A. Also the gate-source current I_{GSS} showed very low values of 5pA before and 5,6 pA after TST. The maximum specified current of the molded package is 200 nA.

The embedded MOSFET of the single chip test vehicle was benchmarked with the datasheet of a commercially available MOSFET component. This benchmark is shown in Table 3.

Table 3: Benchmark of single chip testvehicle

Test	Test Conditions	Spec	Measured	Result
Breakdown Voltage ($B_{V_{DSS}}$)	$V_{GS} = 0$ V, $I_D = 250$ μ A	min 40 V	43 V	ok
Drain Leakage Current (I_{DSS})	$V_{DS} = 40$ V, $V_{GS} = 0$ V	max 10 μ A	2,3-2,9 nA	ok
Gate Leakage Current (I_{GSS})	$V_{DS} = 0$ V, $V_{GS} = 20$ V	max 200 nA	5 pA	ok
Gate to Source threshold Voltage ($V_{GS(th)}$)	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	2 - 4 V	2,8- 2,9	ok
Drain to Source On Resistance ($R_{DS(on)}$)	$V_{GS} = 10$ V, $I_D = 80$ μ A	max 1,7 m Ω	1,4 - 1,5 m Ω	ok
Capacitance Measurements – Input (C_{iss})	$V_{DS} = 25$ V, $V_{GS} = 0$ V, $f = 1$ MHz	7,4 nF	7,9 nF	ok
Output (C_{oss})	$V_{DS} = 25$ V, $V_{GS} = 0$ V, $f = 1$ MHz	1,8 nF	1,8 nF	ok
Body Diode Forward Characteristics V_{SD} vs. I_{SD}	$V_{GS} = 0$ V, $I_S = 180$ A	max 1,5 V	0,9 V	ok

4. Conclusions

During the project a new embedding concept was developed for integration of power components. The embedding technology shows promising potential for automotive applications due to the high miniaturization potential and good electrical performance. Additionally, the concept provides good reflow stability and high resistance against thermal shock testing. The electrical benchmark of the embedded die with a molded package showed equal performance. Especially for the leakage current measurements the embedded version showed superior behavior.

The embedding technology provides the opportunity to deal with automotive customer requirements with a cost competitive PCB technology and comparable or even better electrical, thermal and reliability characteristics.

5. References

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6. Glossary

CO_2 :	Carbon dioxide
<i>MOSFET</i> :	Metal Oxide Semiconductor Field Effect Transistor
<i>DCB</i> :	Direct Copper Bonded
<i>CTE</i> :	Coefficient of Thermal Expansion
<i>DC</i> :	Direct Current
<i>AC</i> :	Alternating Current
<i>TCU</i> :	Transmission Control Unit
<i>PCB</i> :	Printed Circuit board
<i>Pedelec</i> :	Pedal Electric Cycle
<i>SMT</i> :	Surface Mounted technology
<i>IC</i> :	Integrated Circuit
<i>TST</i> :	Thermal Shock Test