

## HOW DOES PRINTED SOLDER PASTE VOLUME AFFECT SOLDER JOINT RELIABILITY?

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### ABSTRACT

Printing of solder paste and stencil technology has been well studied and many papers have been presented on the topic. Very few studies have looked at how solder paste volume affects solder joint reliability. It is the aim of this work to correlate printed solder paste volume to solder joint reliability.

The circuit board chosen for this work includes a variety of component sizes and types. The components tested are as follows: 0402, 0603, 0805, and 1206 Imperial chip components (1005, 1608, 2012, 3216 metric); PLCC; SOT, and SOIC leaded components. In an effort to determine the lower limit of acceptable solder paste volume, printed volumes were varied between 25 and 125% of nominal. Solder joint quality was assessed using IPC-A-610 standard methods and cross-sectional analysis. Solder joint strength was measured using shear and pull tests. Thermal cycling between -40 °C and 125 °C was done for 1000 cycles and solder joint quality and strength was measured again.

In summary, the solder joint reliability data was correlated to printed solder paste volume. This was done in an effort to establish basic guidelines for the printed solder paste volumes required to generate reliable solder joints.

Key words: solder paste volume, solder joint reliability, stencil design, solder joint inspection

### INTRODUCTION

Many studies have been published which address printing of solder paste and improvements to the printing process [1-4]. There are also many studies on the reliability of solder joints which utilize thermal cycling to generate failures and assess reliability in the solder joints [5-10]. Recently a thesis by Sriperumbudur [11] has discussed solder paste volume and how it relates to solder joint reliability for land grid array (LGA), ball grid array (BGA), and quad-flat no-lead (QFN)

components. It is the aim of this paper to correlate printed solder paste volume to solder joint reliability for passive chip components and lead-frame components.

Solder paste stencil files are typically created along with the data for the circuit board. The initial stencil layers are often created at the same size (1:1) as the copper layers. If the stencils are made using the original data without modification, then printing issues would occur such as bridging, solder balling, etc. Engineers and stencil manufacturers modify the stencil design to enhance printing and eliminate printing defects. Modifications are often made in accordance with IPC-7525 Stencil Design Guidelines [12]. It is common practice to reduce the stencil apertures by 10% area to as much as 50% area as compared to the copper pads. This significantly reduces the volume of solder paste that is printed. When fine pitch micro ball grid array ( $\mu$ BGA) or 0201 Imperial (0603 metric) and smaller passive components are used then the stencil thickness may also be reduced. This is done to maintain the aperture area ratio above the industry standard minimum value of 0.66. Reducing stencil thickness also reduces the volume of the printed solder paste. The solder joints created from the reduced solder paste volume must meet IPC-A-610 [13] and J-STD-001 [14] criteria, but are the solder joints reliable? What is the lower limit of solder paste volume required to produce a reliable solder joint? Will the solder joints survive for the lifetime of the assembly? In order to help answer these questions, reliability testing must be performed with a range of solder volumes to determine the lower limit of the printed solder paste volume which can be used.

The IPC-A-610 and J-STD-001 standards allow for a range of solder volumes. The inspection criteria in these standards centers around the following topics:

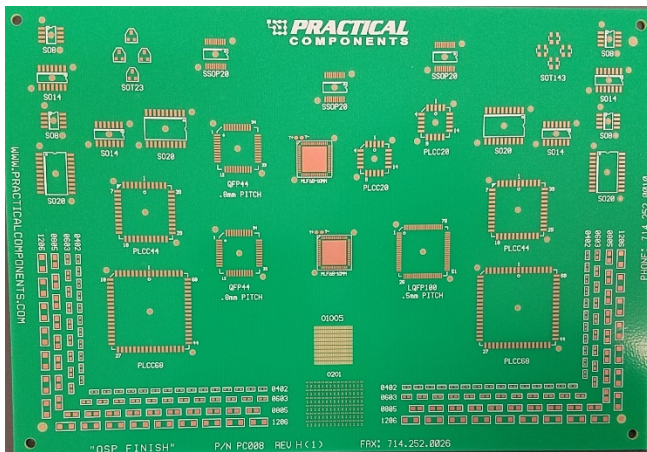
- Solder wetting angles

- Spread or coverage of solder including wetting or de-wetting
- Exposed basis metal
- Pin holes or blow holes
- Cold solder or incomplete reflow
- Excess solder and bridging
- Solder balls and mid-chip beads
- Disturbed solder joints, hot tears or shrinkage cracks
- Fractured or cracked solder
- Position of the components relative to the pads
- Solder joint height, width and length
- Solder thickness

The assembled boards created for this study were inspected to these standards. Shear and pull strength was measured from the solder joints. Thermal cycling was performed and additional shear and pull strength data was gathered. The inspection and solder joint strength data was correlated to printed solder paste volume as shown in the following sections.

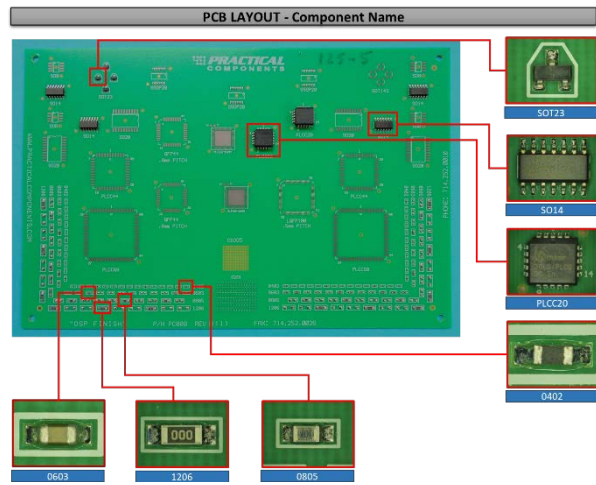
### EXPERIMENTAL METHODOLOGY

The test circuit board used was PCB008 (Figure 1) from Practical Components with organic solderability preservative (OSP-HT) surface finish. This circuit board has a variety of component types and lends itself well to this work.



**Figure 1:** PCB008 Test Circuit Board

Side one of the PCB008 circuit board was used and a selection of components from this side were tested (Figure 2).



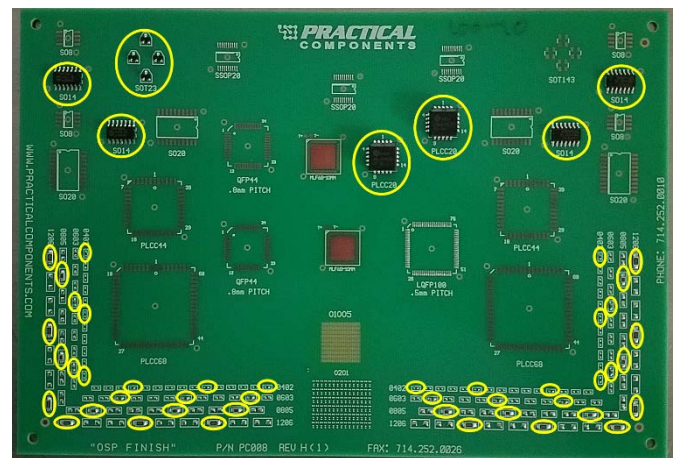
**Figure 2:** Components on the PCB008 Test Circuit Board

A list of the component types and number of placements is shown below (Table 1).

**Table 1:** PCB008 Component Placements

Component	Number of Component Placements per Circuit Board
SOT23	4
SO14 (1.27 mm or 50 mil pitch)	4
PLCC20 (1.27 mm or 50 mil pitch)	2
1206 Imperial (3216 metric)	12
0805 Imperial (2012 metric)	10
0603 Imperial (1608 metric)	10
0402 Imperial (1005 metric)	12

The component placements were spaced in such a way to allow adequate space for shear and pull strength testing (Figure 3). Ten boards were assembled for each solder paste volume level.



**Figure 3:** Component Placements and Spacings on the PCB008 Test Circuit Board

The stencil design for each solder paste volume variation was based upon the supplied stencil data. The solder paste

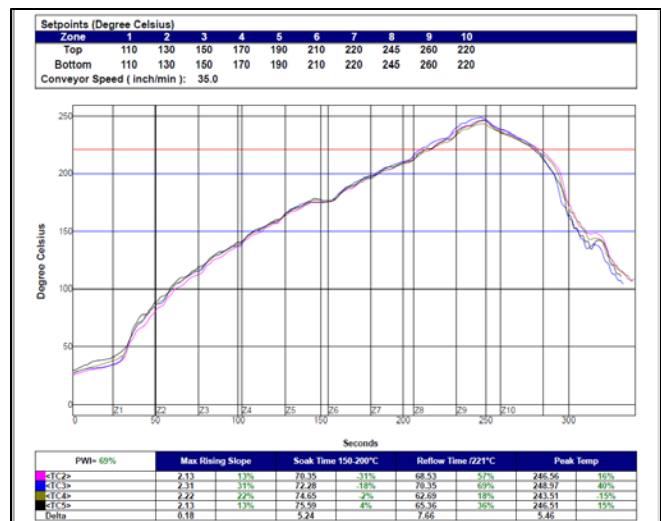
volumes were varied as follows: 125%, 100%, 75%, 50%, 40%, 30%, and 25%. For the 25% volume stencil, the solder joints were not properly formed due to the extremely low solder volumes, therefore the circuit boards made with the 25% solder volume stencil were removed from consideration for pull and shear testing. The 100% volume stencil was made as received from the supplied stencil layer. The other stencils were based upon the 100% stencil design and were made by changing the aperture sizes and/or reducing the stencil thickness (Table 2).

**Table 2:** Stencil Designs for Each Volume Variation

Solder Paste Volume	Stencil Thickness in $\mu\text{m}$ (mils)	Stencil Design (Based Upon the 100% Stencil)
125%	102 (4)	Apertures enlarged to 125% from the 100% stencil.
100%	102 (4)	Stencil data used as received.
75%	76 (3)	Reduced thickness. Apertures kept the same as the 100% stencil.
50%	51 (2)	Reduced thickness. Apertures kept the same as the 100% stencil.
40%	51 (2)	Reduced thickness. Apertures reduced to achieve 40% volume.
30%	51 (2)	Reduced thickness. Apertures reduced to achieve 30% volume.
25%	51 (2)	Reduced thickness. Apertures reduced to achieve 25% volume.

All stencils were made from fine grain stainless steel (2-5 micron) without nano-coatings. It should be noted that the lowest volume stencils (25, 30 and 40%) required modification of the position of the solder paste print on the passive chip components. The solder paste bricks were moved closer to the center of the pad sets which enabled the components to touch the solder paste.

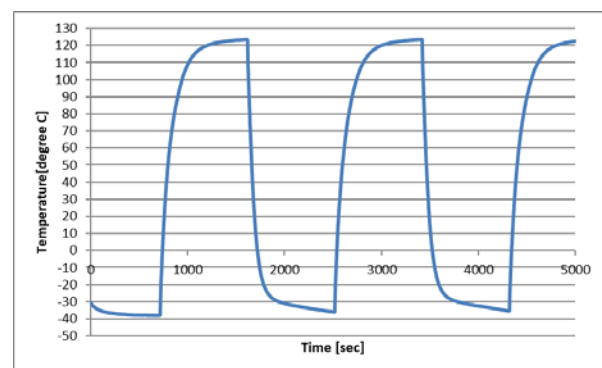
The solder paste used was a no clean, SAC305 Type 4 solder paste. The print parameters were as follows: 30 mm/sec print speed, 300 mm blade length, 5.0 kg pressure, and 3.0 mm/sec separation speed over a 2.0 mm separation distance. The printed solder paste volume was measured with a solder paste inspection system (SPI). The reflow oven used was a 10-zone convection oven. The reflow profile was a linear ramp to spike type profile (Figure 4).



**Figure 4:** Linear Ramp to Spike Reflow Profile for the PCB008 Test Circuit Board

Reflow was done in an air atmosphere and the measured reflow parameters were as follows. The soak time from 150 to 200 °C was 70 to 75 seconds. The time above liquidus (>221 °C) was 63 to 70 seconds. The peak temperature was 243 to 249 °C. After reflow the circuit boards were inspected per IPC-A-610 and J-STD-001 criteria. The data for inspection failures was tallied and summarized by solder paste volume level.

Ten circuit boards were made for each solder paste volume variation. Circuit boards #1 - 4 were used for shear and pull strength testing to measure solder joint strength. Circuit board #5 was used for cross sectioning of representative solder joints. Circuit boards #6 - 10 were thermally cycled for 1000 cycles. The thermal cycle was from -40 °C to 125 °C with 10-minute dwell times and 5-minute ramp times (Figure 5).



**Figure 5:** Thermal Cycling Profile

After thermal cycling, circuit boards #6 - 9 were used for shear and pull strength testing. Circuit board #10 was used for cross sectioning of representative solder joints.

Shear strength testing was done on the passive chip components: 1206, 0805, 0603, and 0402. Pull strength

testing was done on the lead-frame components: SOT23, SO14 and PLCC20 (Table 3).

**Table 3: Shear and Pull Testing Parameters**

Component	Test Type	Stroke	Clearance
0402	Chip Shear	0.5mm/sec	Below 1/4 of component width
0603	Chip Shear	0.5mm/sec	Below 1/4 of component width
0805	Chip Shear	0.5mm/sec	Below 1/4 of component width
1206	Chip Shear	0.5mm/sec	Below 1/4 of component width
SOT23	45° Lead Pull	0.12mm/sec	~
SO14	90° Lead Pull	0.12mm/sec	~
PLCC20	90° Lead Pull	0.12mm/sec	~

The pull strength data available for the SOT23 components was inconsistent and incomplete and therefore was removed from this paper. The data was summarized for each solder paste volume and each component type.

## RESULTS AND DISCUSSION

### Solder Paste SPI Results

The target or aperture solder paste volumes for each component broken out by stencil are shown below (Table 4). These target volumes were calculated from the stencil thicknesses and aperture sizes.

**Table 4: Target or Aperture Solder Paste Volumes (mils<sup>3</sup>) Based on Each Stencil Design**

Component	Stencil						
	25%	30%	40%	50%	75%	100%	125%
0402	500	600	800	1000	1500	2000	2500
0603	1200	1440	1920	2400	3600	4800	6000
0805	3000	3600	4800	6000	9000	12000	15000
1206	3600	4320	5760	7200	10800	14400	18000
PLCC20	1875	2250	3000	3750	5625	7500	9375
SO14	1875	2250	3000	3750	5625	7500	9375
SOT23	1225	1470	1960	2450	3675	4900	6125
SOT23 L	1750	2100	2800	3500	5250	7000	8750

The SOT23 component has two different pad sizes and therefore has two different stencil aperture target volumes. The larger SOT23 aperture is denoted as SOT23L. The measured mean transfer efficiencies (TE %) for each component broken out by stencil are shown below (Table 5). These TE% values are calculated using the 100% stencil target volume.

**Table 5: Measured Mean Transfer Efficiencies (%) Based on the 100% Stencil Target Volumes**

Component	Stencil						
	25%	30%	40%	50%	75%	100%	125%
0402	31%	39%	50%	54%	85%	110%	138%
0603	32%	39%	50%	52%	84%	117%	158%
0805	30%	36%	47%	45%	82%	116%	155%
1206	34%	41%	52%	52%	91%	119%	166%
PLCC20	25%	33%	43%	58%	87%	113%	149%
SO14	28%	31%	40%	60%	81%	112%	187%
SOT23	29%	36%	45%	54%	82%	112%	146%
SOT23 L	32%	40%	48%	66%	91%	122%	142%

The transfer efficiencies are above the targets of the stencil designs. This indicates that the actual printed solder paste volumes were higher than the target volumes. The measured mean solder paste volumes for each component broken out by stencil are shown below (Table 6).

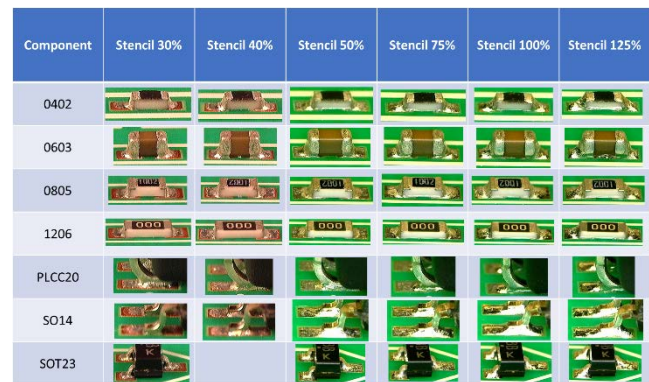
**Table 6: Measured Mean Solder Paste Volumes (mils<sup>3</sup>)**

Component	Stencil						
	25%	30%	40%	50%	75%	100%	125%
0402	628	777	1000	1076	1709	2197	2752
0603	1556	1884	2379	2484	4026	5616	7589
0805	3601	4355	5692	5402	9805	13884	18638
1206	4825	5951	7448	7455	13097	17087	23845
PLCC20	1861	2510	3210	4330	6519	8502	11150
SO14	2074	2352	3004	4509	6061	8434	14020
SOT23	1402	1772	2184	2662	4034	5487	7151
SOT23 L	2267	2773	3376	4638	6402	8527	9939

The mean solder paste volumes and corresponding transfer efficiencies are used for data comparisons throughout the remainder of this paper.

### Solder Joint Inspection Results

Representative pictures of the solder joints formed from the various stencils are shown below (Figure 6).



**Figure 6: Solder Joint Pictures for Each Component by Stencil**

The solder joints were visually inspected in accordance with IPC-A-610 and J-STD-001 standards. The solder joints show good wetting to the component leads with acceptable contact angles for all of the stencils and components. The contact angles at the board pads are also acceptable but there is exposed base metal on the board pads for the 30%, 40% and 50% stencils. Exposed board pad metal is common and considered acceptable for OSP surface finish. The amount of exposed (non-wetted) board pad metal decreases with increasing solder volume as expected. There is very little to no exposed board pad metal for the 75%, 100%, and 125% stencils.

After inspection, the defects were tallied by component and stencil volume (Table 7).

**Table 7: Defect Percentages by Component and Stencil Volume**

Stencil	SO14	SOT23		PLCC20	1206		0805		0603		0402	
		Missing	SB		SB	SKOP	SB	SKOP	SB	SKOP	SB	SKOP
30%	0%	33%	0%	0%	23%	1%	3%	0%	5%	0%	0%	17%
40%	0%	100%	0%	0%	29%	0%	13%	0%	21%	0%	0%	12%
50%	0%	35%	0%	0%	63%	3%	48%	0%	45%	0%	0%	8%
75%	0%	18%	25%	0%	73%	0%	63%	0%	45%	0%	10%	8%
100%	0%	15%	10%	0%	87%	0%	80%	0%	50%	0%	1%	6%
125%	0%	8%	15%	0%	99%	0%	80%	0%	79%	0%	27%	3%

All of the components on every circuit board and stencil volume were inspected. The defect percentages represent

the percentage of components that showed a particular defect. The defects observed were of 3 types: missing components due to placement issues or insufficient paste to hold the components on the boards, solder balling or mid-chip beading, and skew off pad which was due to component placement issues or lack of paste to hold the components in position.

Missing components only occurred for the SOT23 components, and this was due to insufficient paste volume to hold the components on the board. The SOT23 components were not placed for the 40% stencil volume so this defect rate was noted as 100% missing. Generally speaking the rate of missing components increased with decreasing solder volume. This occurred during component placement. The placement system had sufficient vacuum release blow off pressure to move the SOT23 components off of the solder paste. This tended to occur more frequently with lower solder paste volumes.

Solder balling or mid-chip beading was the main defect observed. Random solder balling occurred on the SOT23 components. Mid-chip beading occurred on the passive chip components. Solder balls and mid-chip beads could be re-worked in production to ensure that electrical spacing is maintained. These defects do not affect the solder joint strength portion of this work but were tallied in order to correlate to the stencil volumes. Generally speaking, solder balling and mid chip beading increase with increasing solder paste volume. For example, the 1206 components with the 30% stencil gave 23% mid-chip beading which increased to 99% mid-chip beading for the 125% stencil. The stencil apertures were rectangles as originally designed but could be modified to reduce the mid-chip beading rate.

Skew off pad was observed mainly for the 0402 components and the lower solder paste volumes (30 and 40% stencils). This was due to a combination of placement issues and lack of solder paste to hold the 0402 components in place. As solder paste volume increased the rate of skew decreased. This defect could affect shear strength results especially for the 0402 components. This will be noted in the discussion section of the paper about shear strength for the 0402 components.

### Shear and Pull Strength Data

The shear strength data for the passive chip components and the pull strength data for the leaded components on the as-received boards is shown below (Figure 7).

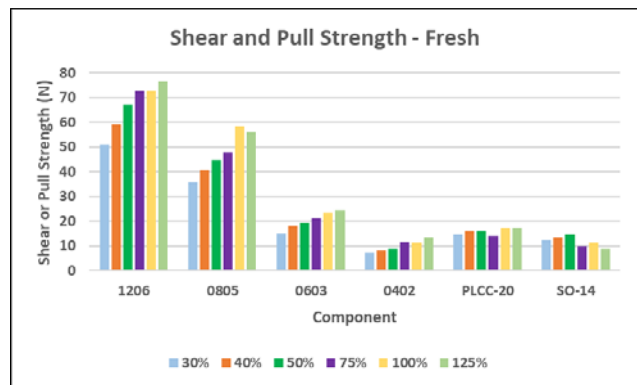


Figure 7: Shear and Pull Strength for the As-received Circuit Boards

The shear strength increased with increasing solder paste volume for the passive chip components. Solder paste volume has a large effect on shear strength for the 1206 and 0805 passive components. Shear strength does not vary as much for the smaller 0603 and 0402 passive components with variation in solder paste volume. The shear strength of the 0402 components could have been affected by the skew seen, especially with the lower stencil volumes (30 and 40%). The leaded components showed very little difference in pull strength for the different solder paste volumes.

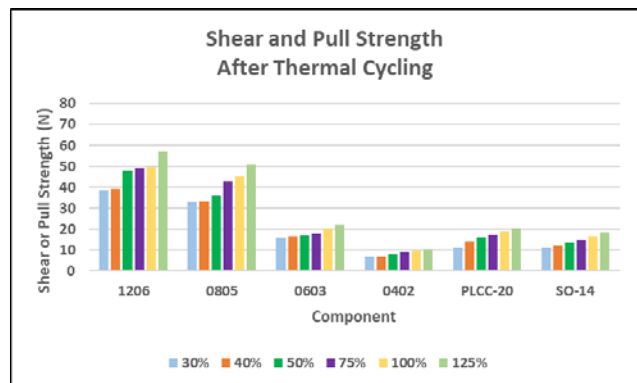
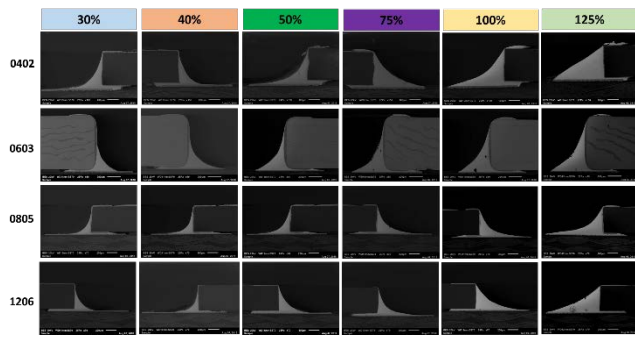


Figure 8: Shear and Pull Strength for the Thermally Cycled Circuit Boards

The shear strength for the thermally cycled circuit boards was lower overall than for the as-received circuit boards. The same general trend of shear strength increasing with solder paste volume was seen for the passive chip components and the leaded components.

### Cross Sectional Images and Intermetallic Thickness for the Passive Chip Components

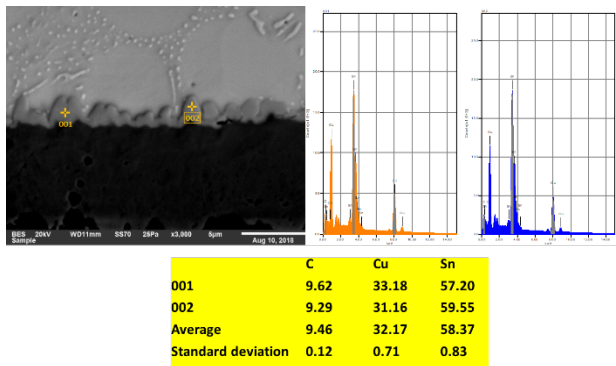
Cross sections were made of the solder joints for the passive chip components before thermal cycling was performed (Figure 9).



**Figure 9:** Cross Sectional Images of Solder Joints for the Passive Chip Components and Each Stencil Volume (As-received)

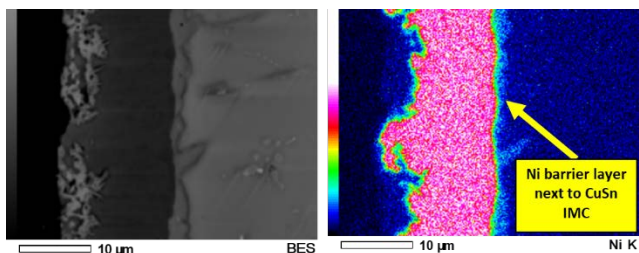
These cross-sectional images show that the solder joints are well formed even with the lowest stencil volume (30%). Wetting is evident on the circuit board pads and on the component leads. The 0603 components are taller than the other passive chip components.

Energy dispersive x-ray (EDX) was used to identify the elemental composition of the intermetallic layers. The composition of the intermetallic compound layer (IMC) at the board pad interface is made up of copper (Cu) and tin (Sn) in a ratio indicating a  $Cu_6Sn_5$  IMC (Figure 10).



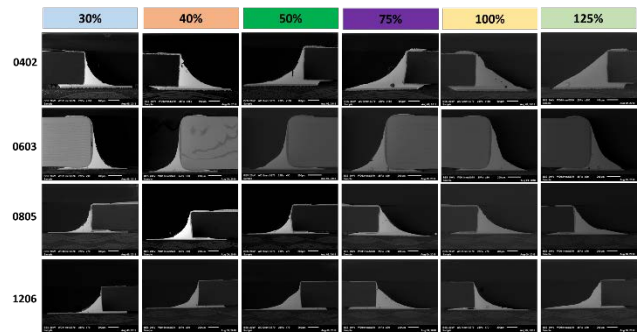
**Figure 10:** EDX Analysis of the Intermetallic Layer at the Circuit Board Pad Interface

The elemental composition at the component interface is made up of Cu and Sn next to a nickel (Ni) barrier layer (Figure 11).



**Figure 11:** EDX Analysis of the Intermetallic Layer at the Component Interface

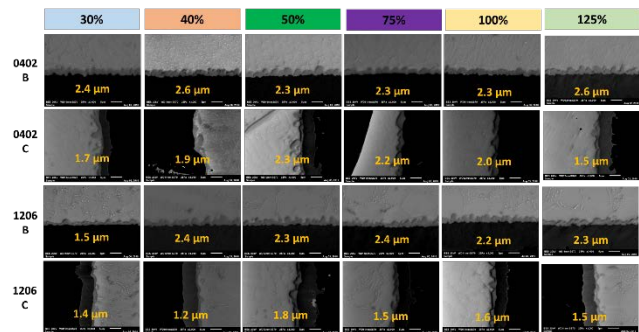
Cross sections were made of each passive chip solder joint type after thermal cycling (Figure 12).



**Figure 12:** Cross Sectional Images of Solder Joints for the Passive Chip Components and Each Stencil Volume After Thermal Cycling

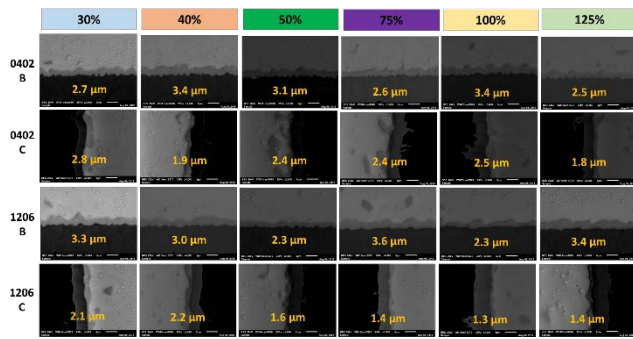
The shape of the solder joints did not change much due to thermal cycling. In general, the solder joints become less concave as the solder volume increases from 30% to 125%. As component size increases from 0402 to 1206 the solder joints become more concave for a given stencil volume.

The intermetallic thickness of the solder joints was measured at the component lead and the board pad interfaces. Image J software was used to do this with images at 3000x magnification. The intermetallic thicknesses for the 0402 and 1206 components before thermal cycling are shown below (Figure 13).



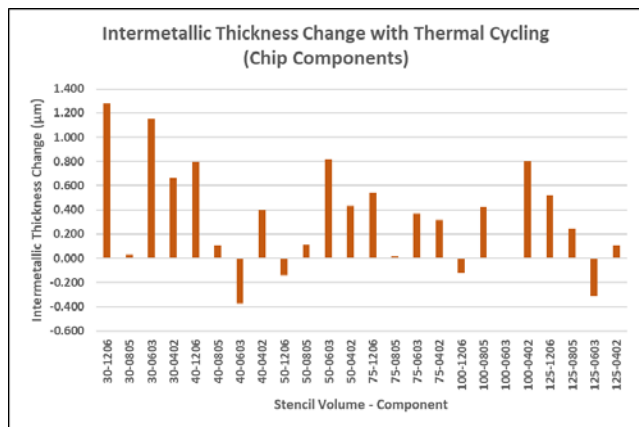
**Figure 13:** Intermetallic Thickness for the As-received 0402 and 1206 Solder Joints. B = Board Pad Interface. C = Component Lead Interface

The intermetallic thicknesses for the 0402 and 1206 components after thermal cycling are shown below (Figure 14).



**Figure 14:** Intermetallic Thickness for the Thermally Cycled 0402 and 1206 Solder Joints. B = Board Pad Interface. C = Component Lead Interface

The intermetallic thicknesses increased with thermal cycling as expected. The mean increase in intermetallic thickness across all passive chip components was 0.341  $\mu\text{m}$ . The amount of increase seems to be dependent upon the solder paste volume (Figure 15).

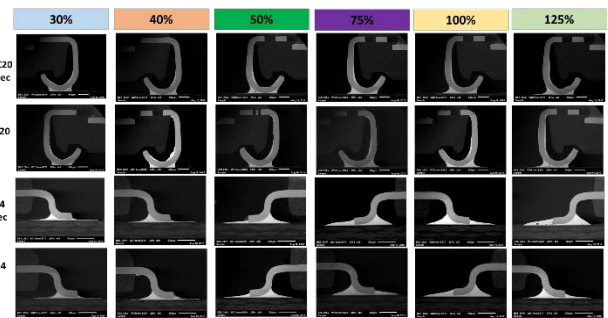


**Figure 15:** Intermetallic Thickness Change with Thermal Cycling for Each Stencil Volume and the Passive Chip Components

Thermal cycling induced larger changes in the intermetallic thickness for the lower stencil volumes (30%) than for the higher stencil volumes (100 and 125%).

**Cross Sectional Images and Intermetallic Thickness for the Lead-Frame Components**

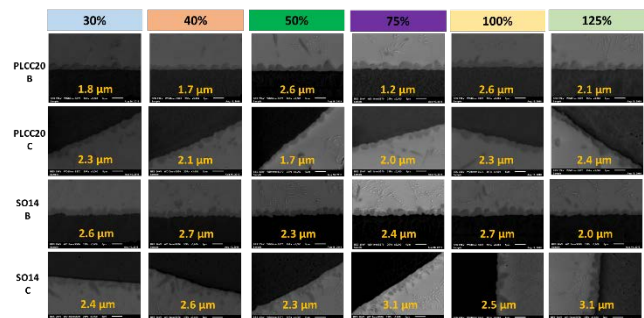
Cross sections were made of the solder joints for the leaded (PLCC20 and SO14) components before and after thermal cycling was performed (Figure 16).



**Figure 16:** Cross Sectional Images of Solder Joints for the Leaded Components and Each Stencil Volume

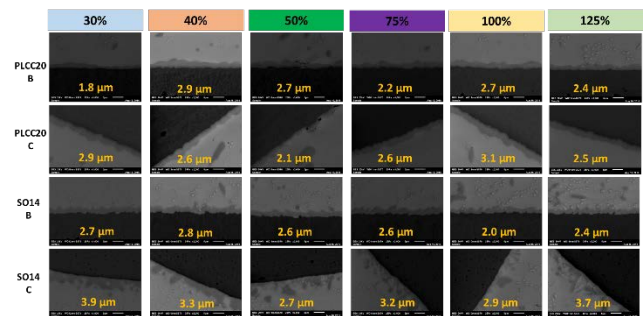
As solder volume increases the solder joints tend to spread farther up the leads and farther on the circuit board pads. With the 30% volume stencil, the solder at the heel of the SO14 and PLCC20 components does not reach a height of the lead thickness. Wetting is evident on both of these components, but the solder height may not be acceptable.

The intermetallic thickness of the solder joints was measured at the component lead and the board pad interfaces. Image J software was used to do this with images at 3000x magnification. The intermetallic thicknesses for the PLCC20 and SO14 components before thermal cycling are shown below (Figure 17).



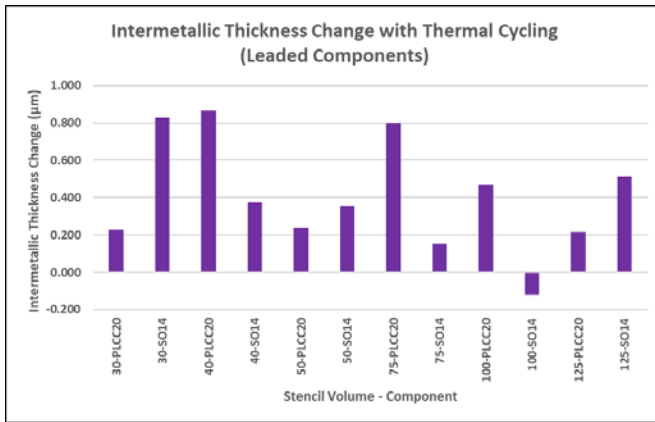
**Figure 17:** Intermetallic Thickness for the As-received PLCC20 and SO14 Solder Joints. B = Board Pad Interface. C = Component Lead Interface

The intermetallic thicknesses for the PLCC20 and SO14 components after thermal cycling are shown below (Figure 18).



**Figure 18:** Intermetallic Thickness for the Thermally Cycled PLCC20 and SO14 Solder Joints. B = Board Pad Interface. C = Component Lead Interface

The intermetallic thicknesses increased with thermal cycling as expected. The mean increase in intermetallic thickness for both leaded components was 0.410  $\mu\text{m}$ . The amount of intermetallic thickness change seems independent of the solder paste volume (Figure 19).

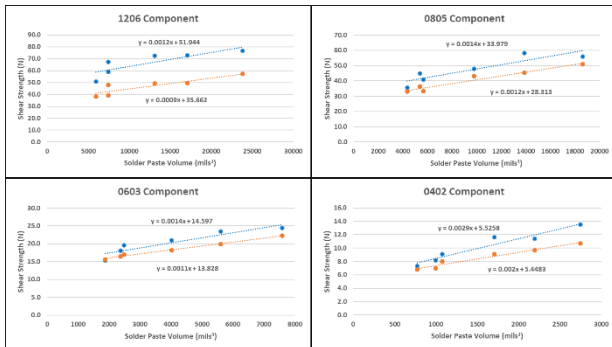


**Figure 19:** Intermetallic Thickness Change with Thermal Cycling for Each Stencil Volume and the Leaded Components

The stencil volume had less of an effect on the change in intermetallic thickness for the leaded components than it did for the passive chip components.

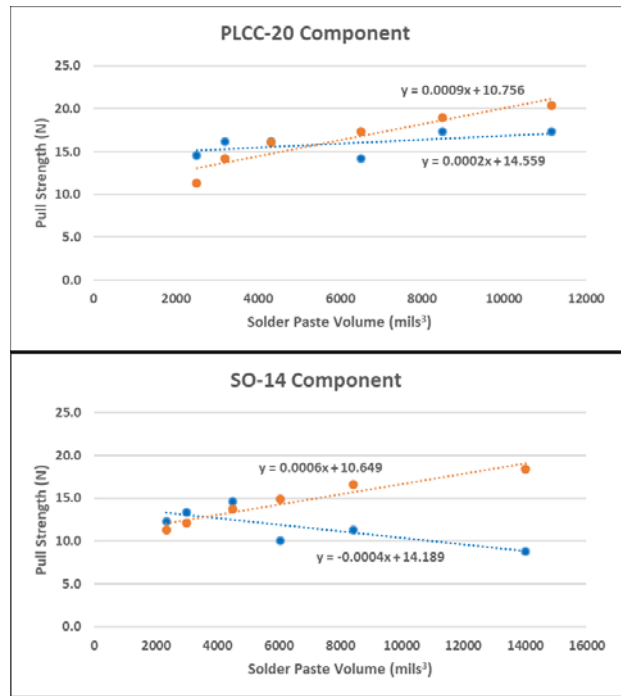
**Correlation of Solder Joint Strength to Solder Volume**

As solder paste volume increases the shear strength of the passive chip component solder joints also increases (Figure 20).



**Figure 20:** Shear Strength of Passive Chip Components Variation with Solder Volume. Blue = As-received Solder Joints. Orange = Thermally Cycled Solder Joints.

This trend was not the case for the leaded components especially for the SOIC component (Figure 21).



**Figure 21:** Pull Strength of Leaded Components Variation with Solder Volume. Blue = As-received Solder Joints. Orange = Thermally Cycled Solder Joints.

The pull strength for the as-received PLCC20 solder joints was fairly consistent regardless of solder paste volume. After thermal cycling the pull strength increased with increasing solder paste volume. Before thermal cycling the SO14 components showed decreasing solder joint strength with increasing solder volume. After thermal cycling, the pull strength of the SO14 solder joints increased with increasing solder volume.

**Summary of Results**

The 25% volume stencil produced solder joints that were not well formed for all the component types tested. Wetting was inadequate with clear areas of non-wetting. The 30% stencil produced solder joints that passed visual inspection, but the cross sections of the leaded components showed wetting on the component leads that may be inadequate. The 30% and higher stencil volumes produced solder joints that are acceptable on the larger passive chip components. The 50% and higher stencil volumes produced solder joints that are acceptable on the smaller passive chip components.

The SO14 and PLCC20 components did not show soldering defects other than solder joint height with the 30% volume stencil. There were many missing SOT23 components with the 30, 40, and 50% volume stencils due to inadequate solder paste volume to hold the components in place during processing. The SOT23 components with the 75, 100, and 125% volume stencils showed some random solder balling around the solder joints. The 1206 components showed mid chip beading with every stencil volume, and this defect increased with increasing solder paste volumes. The 0805 and 0603 components showed very little mid chip beading



with the 30 and 40% volume stencils, but this increased with the 50% and higher volume stencils. The 0402 components showed mid chip beading only on the 75%, 100% and 125% volume stencils. The 0402 components showed some skew with the 30 and 40% volume stencils, but this decreased with the 50% and higher volume stencils. Some of the 0402 components skew was attributed to placement issues. Mid chip beading and skew could be reduced through modification of the stencil design.

The shear and pull strength tests showed some differences in performance for the different stencil volumes. The 30 and 40% stencil volumes produced shear strengths that may be unacceptable for the passive chip components. The stencil volume did not have as great of an effect on the leaded component pull strength. The pull strength for the leaded components may be acceptable for the 40% and higher stencil volumes.

Intermetallic thickness increased with thermal cycling, but this change in thickness was dependent upon the stencil volume. As stencil volume increased, the amount of change in intermetallic thickness decreased for the passive chip components. This same trend was true for the leaded components but to a lesser extent.

Here are recommended stencil volumes (transfer efficiencies) for acceptable and reliable solder joints (Table 8). These recommendations are based upon this work and previous work done by Bath [5].

**Table 8:** Stencil Volume or TE% Required for Acceptable and Reliable PCBAs by Component.

Component	TE% for Acceptable Solder Joints	TE% for Reliable Solder Joints
0402 Imperial (1005 metric)	50	50
0603 Imperial (1608 metric)	50	50
0805 Imperial (2012 metric)	30	50
1206 Imperial (3216 metric)	30	50
PLCC20	40	40*
SO14	40	40*
SOT23	75	More testing data needed

\*There was no comparison data available from other work for the PLCC and SOIC pull test data.

In other work, Sriperumbudur [11] reports that the following transfer efficiency levels are acceptable for assembly and reliability of specific BGA and LGA/QFN components on printed circuit board assemblies (Table 9).

**Table 9:** Comparable Transfer Efficiency Required for Acceptable and Reliable PCBAs by Component.

Component	TE% for Acceptable Solder Joints	TE% for Reliable Solder Joints
LGA 208	60	80
LGA 97	50	70
QFN 100	30	50
QFN 156	30	50
BGA 144	30	30
BGA 360	30	30

These transfer efficiency levels are similar to those recommended above (Table 8).

## CONCLUSIONS

This study gives some guidelines on the effects of solder paste volume for certain components in terms of manufacturing yield and reliability. It is apparent that a wide range of solder paste volumes can be used to create acceptable solder joints, but if the solder volume is too low then solder joints may not be reliable. Changing solder paste volume can induce certain defects but these defects are correctable. It is advisable for PCB assemblers to set up their own standards for acceptable solder paste volume based on the components used.

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## REFERENCES

- [1] J. Bath, T. Lentz, G. Smith, "An Investigation into the Use of Nano-Coated Stencils to Improve Solder Paste Printing with Small Stencil Aperture Area Ratios", *Proceedings of IPC Apex Expo*, 2016.
- [2] T. Lentz, "Performing Enhancing Nano-coatings: Changing the Rules of Stencil Design", *Proceedings of SMTA International*, 2014.
- [3] G. Smith, "Impact of Stencil Foil Type on Solder Paste Transfer Efficiency for Laser Cut SMT Stencils", *Proceedings of SMTA International*, 2017.
- [4] M. Burgess, L. Gyalog, "The Importance of Stencil Tension for High Yield SMT Printing", *Proceedings of SMTA International*, 2017.
- [5] J. Bath, E. Crombez, "Surface Mount Assembly Evaluations with Lead-Free Solder Pastes", *Proceedings of SMTA-Nepcon East*, 2000.

- [6] R. Padilla, D. Daily, et. al, "Surviving 3K Thermal Cycles with Variable Void Levels (-40°C to 125°C)", Proceedings of IPC Apex Expo, 2018.
- [7] A. Raj, S. Sridhar, et. al, "Comparative Study on Impact of Various Low Creep Doped Lead Free Solder Alloys", Proceedings of SMTA International, 2017.
- [8] T. Wada, S. Tsuchiya, et. al., "Improving Thermal Cycle and Mechanical Drop Impact Resistance of a Lead-Free Tin-Silver-Bismuth-Indium Solder Alloy with Minor Doping of Copper Additive", Proceedings of IPC Apex Expo, 2017.
- [9] R. Ghaffarian, S. Ramkumar, A. Varanasi, "Lead Free 0201 Assembly and Thermal Cycle/Aging Reliability", Proceedings of IPC Apex Expo, 2006.
- [10] M. Dusek, J. Nottay, C. Hunt, "The Use of Shear Testing and Thermal Cycling for Assessment of Solder Joint Reliability", National Physical Laboratory - Middlesex, UK, June 2000.
- [11] S. Sriperumbudur, "Effects of Solder Paste Volume on PCBA Assembly Yield and Reliability", Rochester Institute of Technology, Thesis, May 2016.
- [12] Stencil Design Task Group (5-21e), "Stencil Design Guidelines", IPC-7525B, October 2011.
- [13] IPC-A-610 Task Group (7-31b), "Acceptability of Electronic Assemblies", IPC-A-610 Rev G, October 2017.
- [14] J-STD-001 Task Group (5-22a), "Requirements for Soldered Electrical and Electronic Assemblies", J-STD-001 Rev G, October 2017.