As originally published in the IPC APEX EXPO Conference Proceedings.

Printed Circuit Board Fabrication Processes and Their Effects on Fine Copper Barrel Cracks

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Abstract
The onset of copper barrel cracks is typically induced by the presence of manufacturing defects. In the absence of discernible manufacturing defects, the causes of copper barrel cracks in printed circuit board (PCB) plated through holes is not well understood. Accordingly, there is a need to determine what affects the onset of barrel cracks and then control those causes to mitigate their initiation.

The objective of this research is to conduct a design of experiment (DOE) to determine if there is a relationship between PCB fabrication processes and the prevalence of fine barrel cracks. The test vehicle used will be a 16-layer epoxy-based PCB that has two different sized plated through holes as well as buried vias.

The DOE will include an 8 run experiment with 2 center point runs for a total of 10 runs. This experimental setup is a half fractional factorial with resolution IV. Resolution IV means that main effects, each factor considered individually, are confounded with 3-way interactions. The PCB manufacturing processes selected as factors include laminate cooling rate, plating current density, pulse waveform, and hot air solder leveling (HASL) reflow. A confounded interaction cannot be separated out statistically from its "aliased" main effect. This DOE is a screening design, which is preferred for early investigation since the likelihood that a 3-way interaction would dominate over a main effect is extremely unlikely.

For this DOE, some deviations from an ideal experimentation setup are present. Since each coupon has multiple holes, samples are not uniquely independent. Also, the factors of pulse waveform and current density are not independent. The pulse waveform is also a nominal variable listed as a continuous factor for design purposes and has no center point value.

Introduction
The initiation of this research resulted from a PCB qualification process for a missile guidance system. This qualification process utilized the thermal shock requirements of MIL-PRF-31032/1C where a failure is defined as the presence of any crack in a plated via induced by the thermal shock test. A preliminary survey of the PCBs that failed thermal shock qualification showed an incidence rate of approximately 15% across multiple suppliers. An incident was defined as at least one fine barrel crack in any copper plated via. These results led the investigators to question that if cracks were present, under what manufacturing conditions could the cracks be mitigated or eliminated.

Plan Details
A team of designers, PCB manufacturing and plating experts, PCB testing agents, and a DOE expert was formed to review PCB manufacturing methods and to develop a DOE that would identify what processes may have a causal relationship with the initiation of barrel cracks. The four factors and levels chosen are shown in Table 1. After identification of significant factors and preferred levels, a second optimization experiment, examining second order or higher interactions, is planned.

Table 1 - DOE Factors and Levels

Factor	Level Description	Low Level	Center Point	High Level
Laminate Cooling Rate	Air, Water Jacket	Water (Standard)		Air
Plating Current Density	Amps Per Square Foot	8	11	14
Pulse Waveform	More Pulse (-1) to More DC (+1)	-1	0	1
HASL Reflow	Number of Reflows	1	3	5

The laminate cooling rate is defined by what method is used to cool the laminated books to room temperature. The standard process is the water jacketed cooling process. The current density is the current as specified in the rectification control panel. The pulse waveform ranges from a 'more pulse' (level -1) to a 'more DC' (level +1) waveform. The hot air solder leveling (HASL) is the number of times that a board is subjected to HASL reflow. The screening experiment and runs are shown in Table 2.

Table 2 - DOE Experiment Runs

Standard Order	Run Order	Center Point	Factors			
			Cooling Method	Current Density	Pulse Waveform	HASL Reflow
1	1	1	Water	8	-1	1
7	2	1	Water	14	1	1
9	3	0	Water	11	0	3
6	4	1	Air	8	1	1
3	5	1	Water	14	-1	5
8	6	1	Air	14	1	5
2	8	1	Air	8	-1	5
10	7	0	Air	11	0	3
5	9	1	Water	8	1	5
4	10	1	Air	14	-1	1

A detailed manufacturing plan was developed that included key characteristics such as lamination, plating, and drilling. Lamination was performed simultaneously: six books in press at one time; three books with controlled water cooling and three books with slow cooling (Air) in the room. Cooling rates were monitored by thermocouple. To minimize experimental variation resulting from other PCB manufacturing processes, all boards were plated in the same tank as well as in the same cell using the same flight bar. Drilling was performed on the same machines, noting which spindles were used.

Two panels with six PCBs and various coupons were used for each run of the experiment. Since the panels were processed simultaneously to minimize experimental variation, the second panel represented a repeat run rather than a true DOE replicate. However, the data resulting from the second panels was included in the analysis to provide further validation. The total number of samples per run was 36. A sample is defined as one discrete barrel. A Type I error rate (α), the risk of falsely assuming a factor, which has no impact, as significant, was assumed to be 5%. The Type II error rate (β), the risk of failing to detect a factor that, in reality, is significant, is assumed to be 5%. Based on these risks, using 36 samples enabled the detection of an improvement to 7.5% (or lower) or degradation to 21.7% (or higher) in terms of the crack incidence rate. To ensure sufficient sample size, three coupons with four barrels each were cut from two boards per run. The panel layout is shown in Figure 1.

The three coupons have different types of barrel features. The first coupon, PTH1, has four 635 µm (0.025") plated through holes (PTH) for connectors. The second coupon, PTH2, has four solder mask tented 457.2 µm (0.018") plated through holes. The last coupon, BV3, has four buried vias (BV) 381 µm (0.015") that were configured between layers 2 and 15. The barrel numbers for each coupon are shown in the cut plan, Figure 2.

A coupon serialization scheme was developed in order to maintain traceability of all the samples. After the experiment was completed at the PCB supplier, the boards and test coupons were sent to the design agent where two PCBs per panel were removed and shipped to the testing agent. A thermal stress test was conducted, in accordance with test method number 2.6.8 of IPC-TM-650, Test Condition C (3 times at 232°C), on one board from each run at the same coupon locations as shown in Figure 2. This thermal stress test verified that the new fabrication methods did not induce eyebrow cracks and that via plating integrity was maintained. The remaining three boards from each run were used to perform the 100-cycle thermal shock test as outlined in MIL-PRF-31032/1C, paragraph 4.7.6.3 (IPC-TM-650, Method 2.6.7.2) with temperature extremes of -65°C to +125°C. When possible, all PCBs were run through the thermal chamber simultaneously to minimize test variation. The testing agent also ran the Interconnect Stress Test (IST) on IST Coupon D, shown in Figure 2, through 100 thermal cycles at 150°C and performed resistance testing in a different oven run. The testing agent labeled the via coupons, in accordance with the naming convention, and prepared and inspected the coupons according to their internal process procedures.

A total of 360 samples (30 thermal shock PCBs, 3 coupons on each, 4 locations per coupon) was used for the DOE. A positive sample consists of a barrel that the testing agency identified as having a barrel crack. Multiple cracks on one barrel were considered one positive instance of a barrel crack. Coupons could have multiple barrels with cracks and all barrels counted toward positive samples. To control possible influence from the inspection process, coupons were evaluated by the same inspector when possible. Documentation of any positive samples including the barrel number, as specified in Figure 2, the location of the crack on the barrel, an image of the crack, and a measurement of the crack was required.

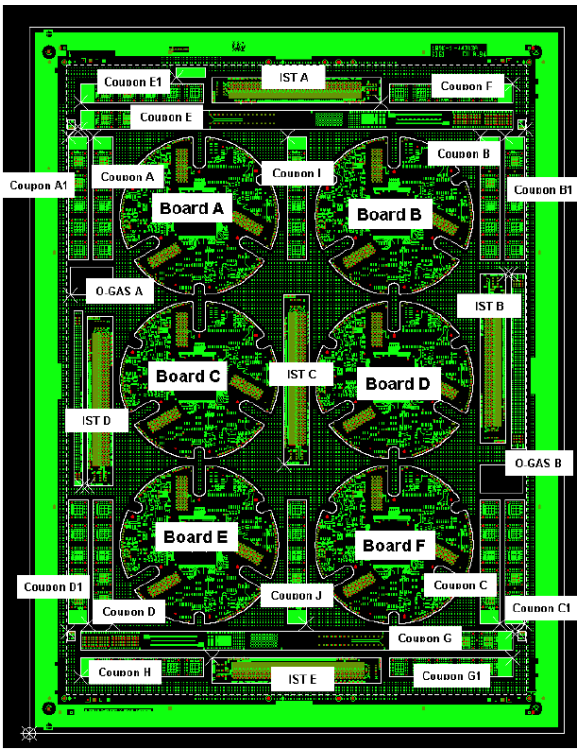

Figure 1 - Panel Layout

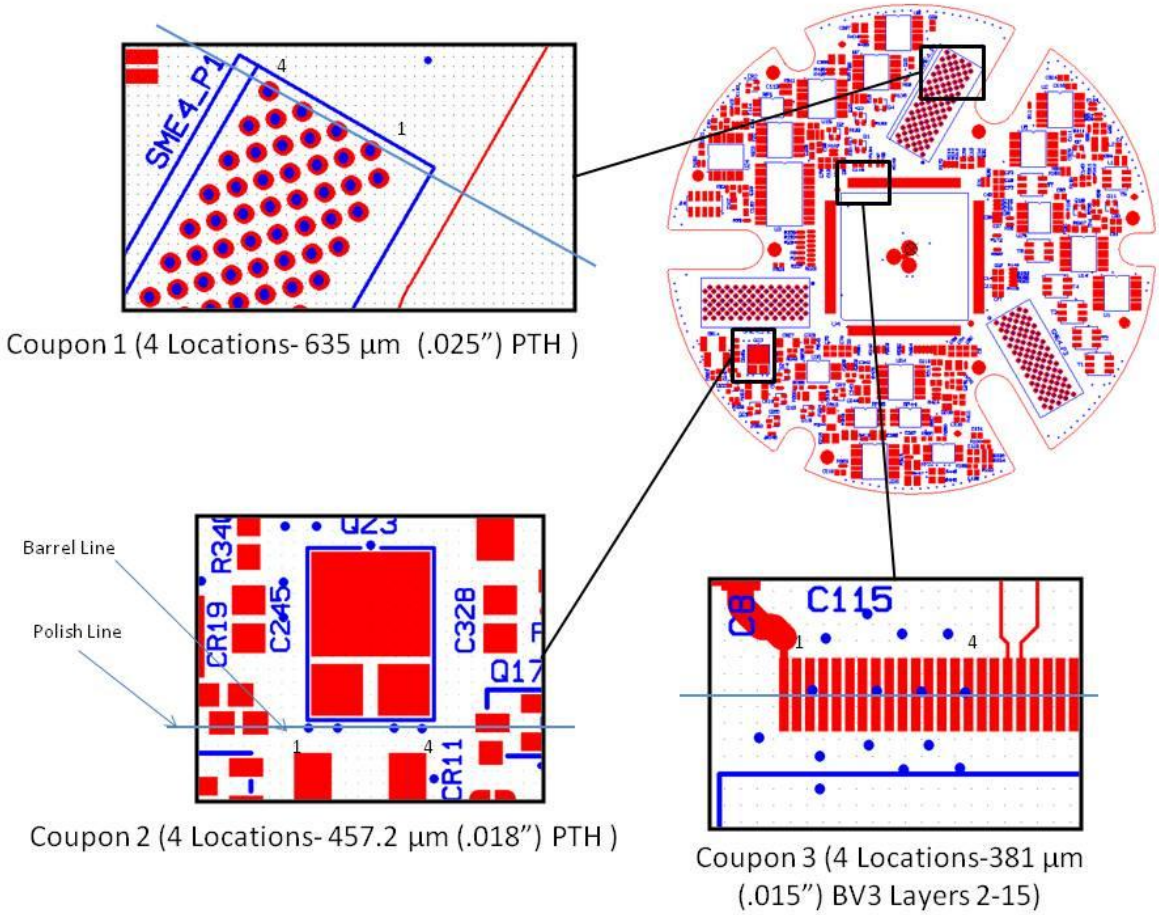

Figure 2 - DOE Cut Plan

Results

The optimization plot shown in Figure 3 indicates that, within the design space tested, the optimal settings to minimize crack length average (ave) and crack length standard deviation (std) are as shown in Table 3.

Figure 3 uses a composite desirability index since the behavior of one response may differ from another response for certain factor settings. However, the response slopes for both the average and standard deviation are parallel, with the exception of HASL reflow, where the standard deviation slope is fairly flat. An ideal desirability index equals 1.0, which is a unitless measure of how well the optimal DOE factor settings result in meeting the specification limits for the response variables. A goal (or target) of zero (i..e., no crack) was specified with an upper limit, which is required by the optimization scheme, equal to 33.0 µm. The zero target, or no cracks, is weighted by a constant, ten on a scale of one to ten, since the goal is minimization of crack lengths. The predicted average crack length, if observed, is 0.7798 µm with standard deviation of 1.8077 µm. The composite desirability index, D, based upon the separate desirability indices, d, for each response variable, equals 0.82508.

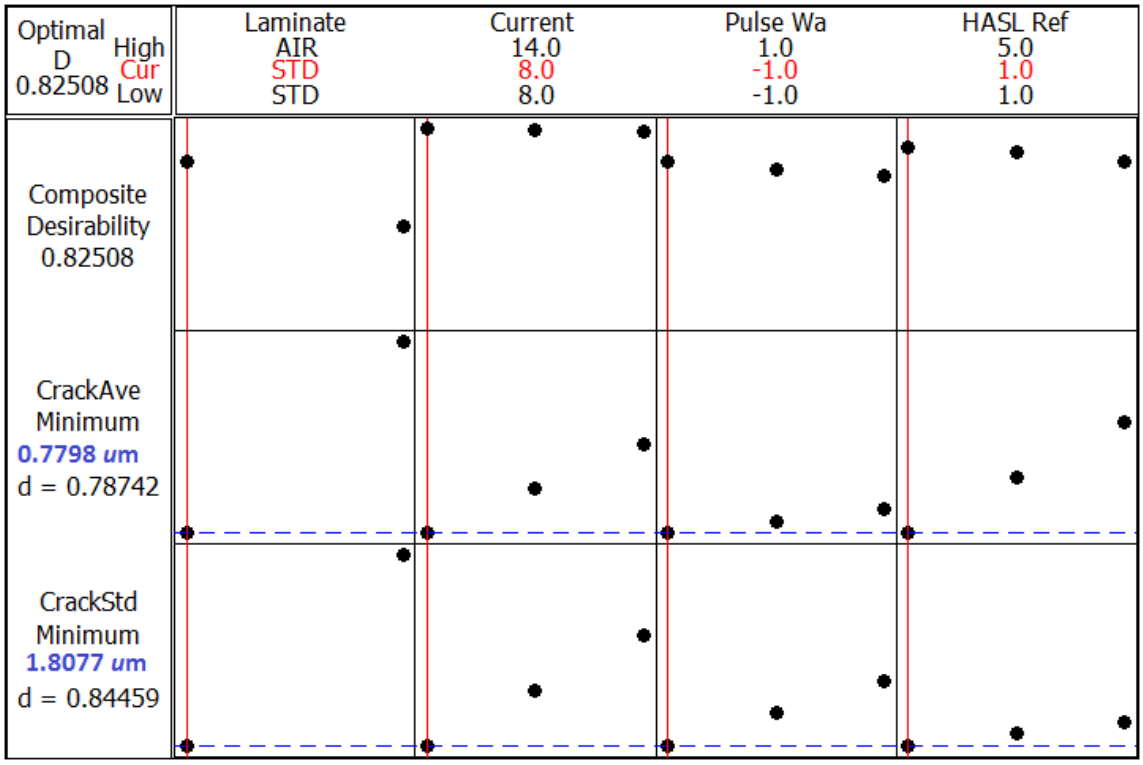

Figure 3 - Optimization Plot of Crack Length Average and Standard Deviation (optimal settings)

Table 3 - Optimal DOE Settings

Factor	Description	Recommended Setting
Laminate Cooling Method	Water Jacket (Standard) or Air	Standard
Plating Current Density	Amps per Square Foot	8
Pulse Waveform	More Pulse (-1) to More DC (+1)	-1
HASL Reflow	Number of Reflows	1

A binary logistic regression was conducted on the incidence of cracks. This analysis enables identification of significant factors with cracking as an attribute variable (i.e., 0: no crack, 1: crack). A summary is shown in Table 4.

Table 4 - Logistic Regression on Crack Incidence Rate

Coupon	Air Cooling Odds Ratio	Significance	HASL Reflow Odds Ratio	Significance
457.2 µm PTH	2.20	0.065	1.25	0.067
635 µm PTH	5.61	0.001	1.60	0.001
Buried Via	5.57	0.001	1.77	0.000

The odds ratio indicates the likelihood of a crack occurring at that location based on changing one factor setting with the other factor setting held constant. For example, when changing from water to air for the laminate cooling method, with the same number of reflow cycles, the likelihood of cracking increases, on average, for both the 635 µm PTH and buried vias, by 561% and 577%, based upon the respective odds ratios of 5.61 and 5.57. For HASL reflow, the odds ratio is interpreted for each one-unit increase in reflow cycle. So, each additional cycle beyond one cycle, using the same laminate cooling method increases the average likelihood of cracking by 25% to 77% (1.25 to 1.77), with buried vias at most risk. Note that the 457.2 µm PTH results were not within the 0.05 significance threshold, which corresponds to 95% confidence. However, reporting the odds ratio is still useful for comparison purposes.

Table 5 summarizes the crack incidence rate for the DOE data and validates the odds ratio results in Table 4.

Table 5 - Crack Incidence Rate

Coupon Cracked?	Laminate Cooling		HASL Reflow		
	Standard	Air	1	3*	5
No	95	54	77	34	38
Yes	85	126	67	38	106

* Center point has 72 total versus 144 total for other runs.

Figure 4, Figure 5, and Figure 6 portray box-and-whisker plots (a.k.a. "box plots") for the response variable maximum crack length, whereby no crack is assigned a value of zero for these variable data. The median (50th percentile) values for each grouping are shown and correspond to the inner horizontal line within the box. The outer box edges represent the 25th and 75th percentiles. The "whiskers" are the minimum and maximum, with the exception of outliers ('*') exceeding the interquartile range (75th minus 25th percentiles).

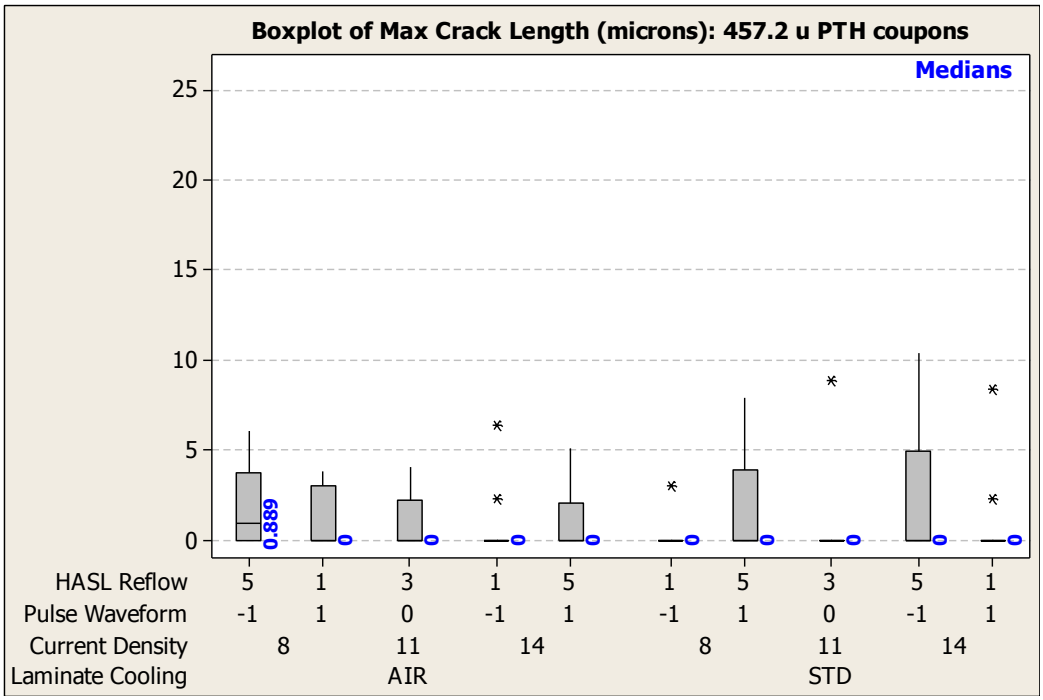

Figure 4 - Box Plot of Maximum Crack Length (457.2 µm PTH coupons)

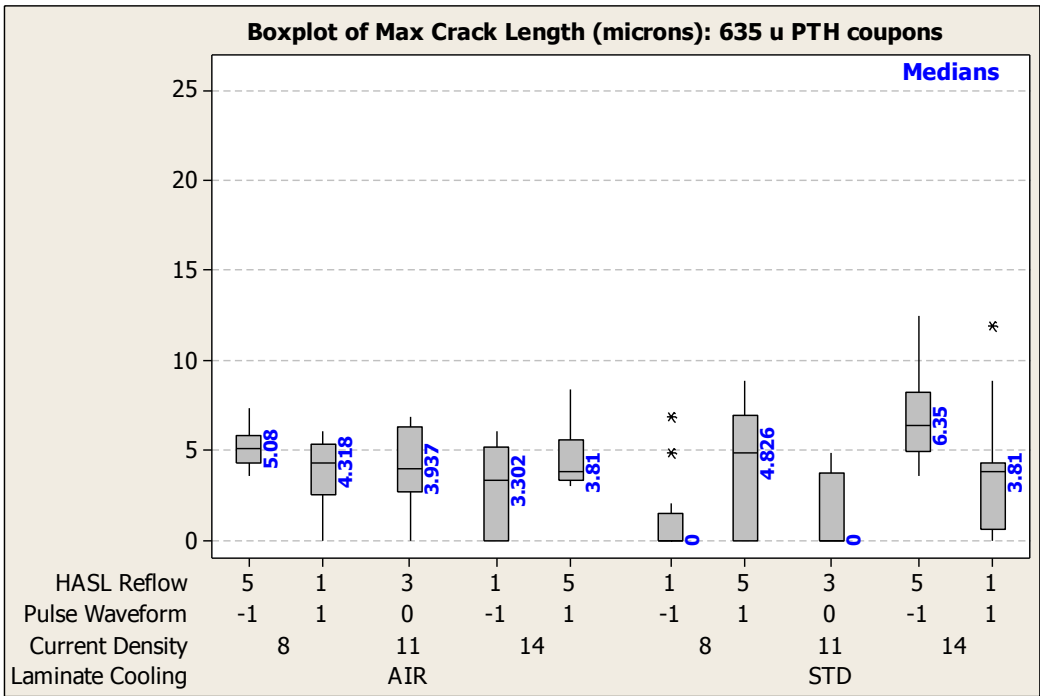

Figure 5: Box Plot of Maximum Crack Length (635 µm PTH coupons)

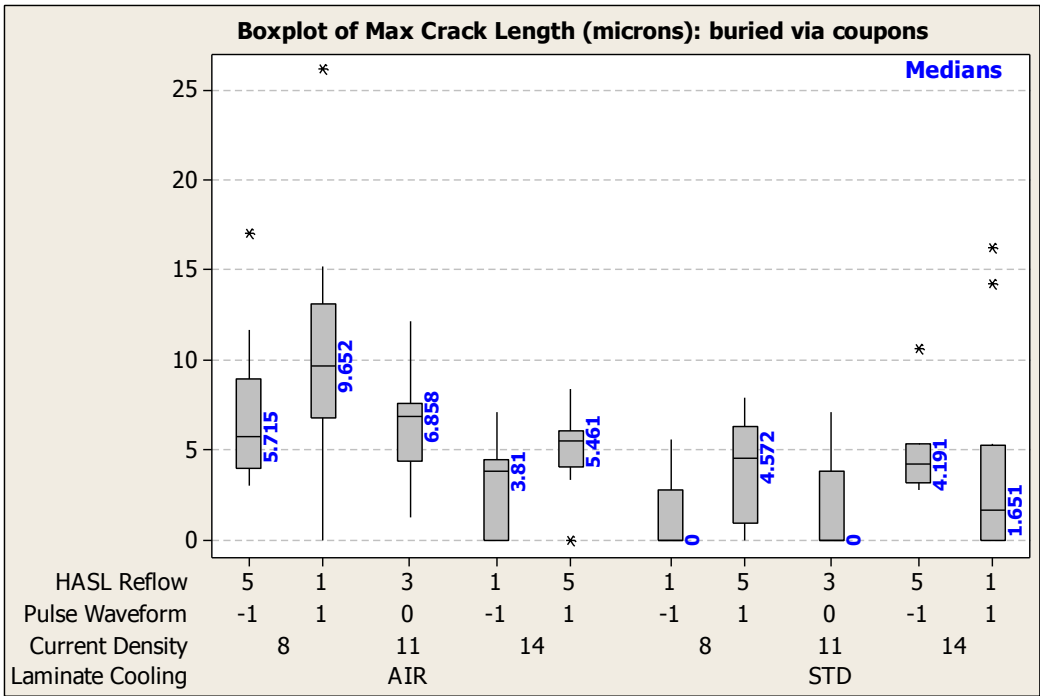

Figure 6 - Box Plot of Maximum Crack Length (buried via coupons)

Box plots are useful for examining both the centering and variability of response data as well as identifying outliers. Outliers may stem from measurement or data entry error and may warrant investigation depending on the frequency and thus influence on the final analysis. In general, the buried via coupon type has the highest median values for most DOE factor settings, notably with air cooling, and 457.2 µm PTH indicates the lowest crack lengths. The graphs are plotted on the same y-axis scale to facilitate comparing magnitudes.

Figure 7, Figure 8, and Figure 9 depict the box plots for average plating thickness by coupon location. In general, the plating thickness of buried vias exhibits less variability than the other coupon types for most of the factor settings. All DOE factor settings and coupon locations meet the plating thickness specification minimum of 30.48 µm (0.0012")

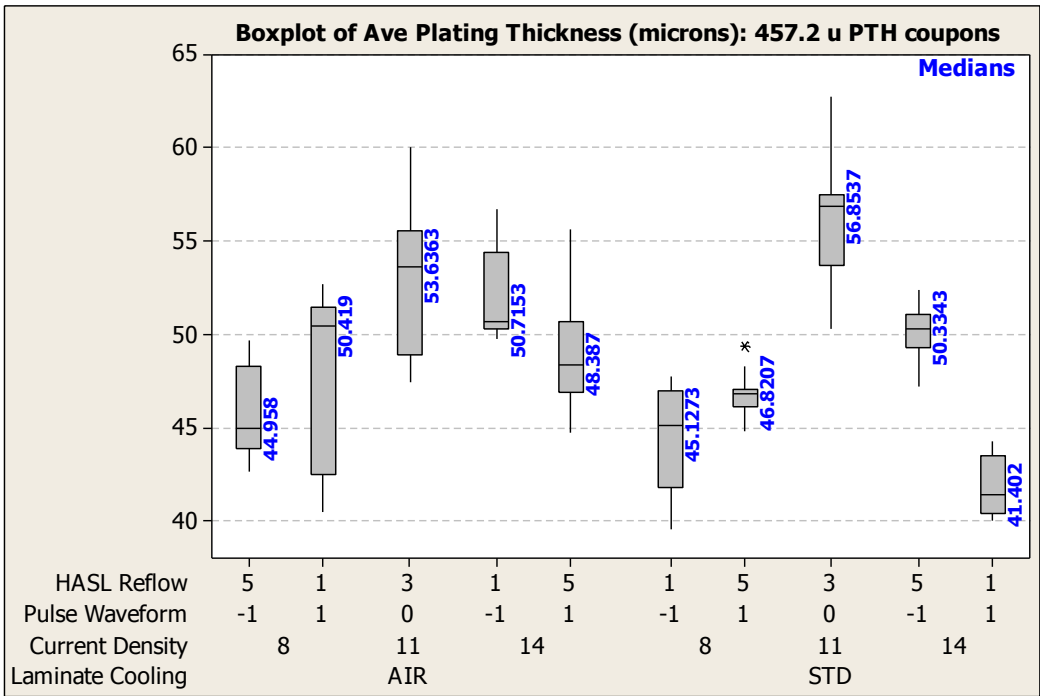

Figure 7 - Box Plot of Average Plating Thickness (457.2 µm PTH coupons)

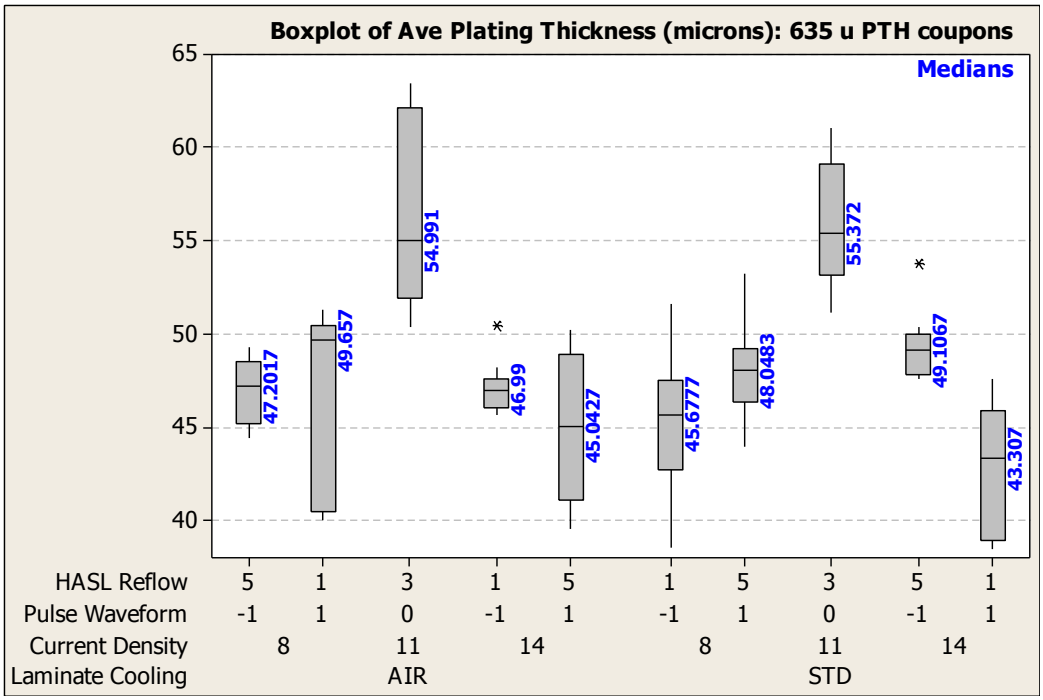

Figure 8 - Box Plot of Average Plating Thickness (635 µm PTH coupons)

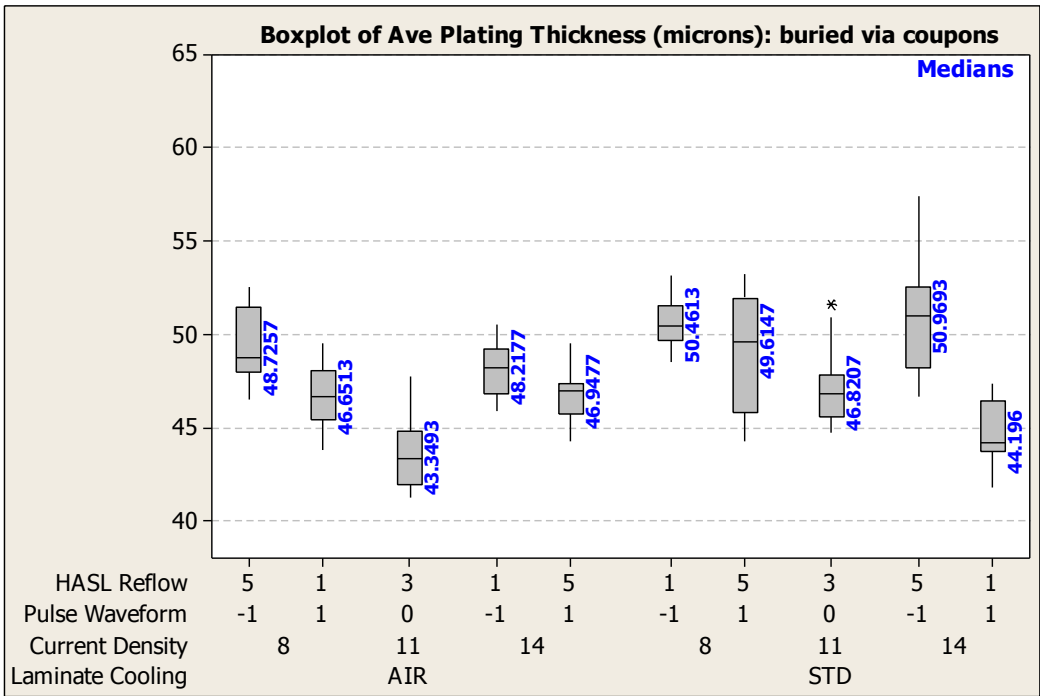

Figure 9 - Box Plot of Average Plating Thickness (buried via coupons)

The data were separated by via type (457.2 µm PTH, 635 µm PTH, buried) to assess significant factors on the responses and to determine if any recommended settings differ from Table 3. A useful method to identify significant DOE factors is the normal probability plot of the effects. This plot is based upon the premise of the normal distribution with z-score calculations and corresponding normal percentiles. Plot points that do not fall near the line, representing the "flattened" normal curve, usually signal important effects. Important effects are larger and generally further from the fitted line than unimportant effects. Unimportant effects tend to be smaller and centered about zero. The plotted z-score not only indicates the relative magnitude but also the direction of the mean response. Since crack length should be minimized, the optimal setting for a negative effect is the highest (and vice versa for positive effects). For higher-order effects (e.g., AB inferring an interaction of laminate cooling method*current density), the corresponding interaction plot should be reviewed to determine the optimum.

Figure 10 indicates that with 95% confidence (i.e., 5% chance of concluding that a factor is significant, when, in reality, the factor does not have an impact on the response), only HASL reflow, with the effect plotted in red, has a significant impact on maximum crack length for the 457.2 µm PTHs. No significant interaction effects (e.g., laminate cooling*current density) are identified and are therefore not plotted for this via type. A plot of the main (or first order) effects (Figure 11) indicates that one HASL reflow is the preferred setting for 457.2 µm PTHs, which corresponds with the optimal recommendations in Table 3.

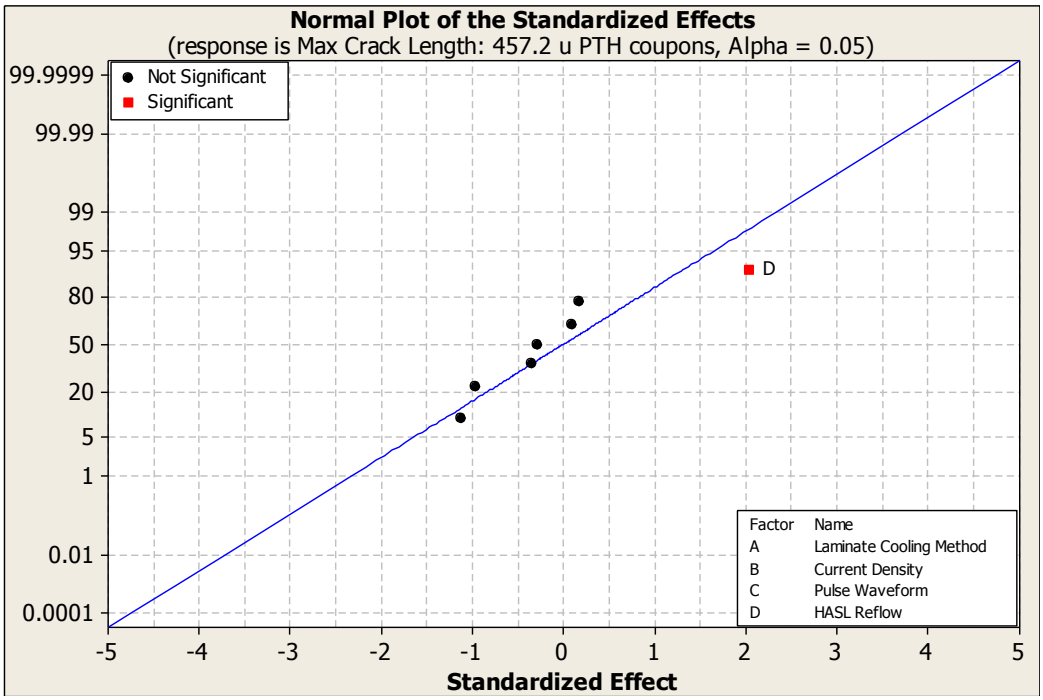

Figure 10 - Normal Probability Plot of the Effects: Maximum Crack Length (457.2 µm PTH coupons)

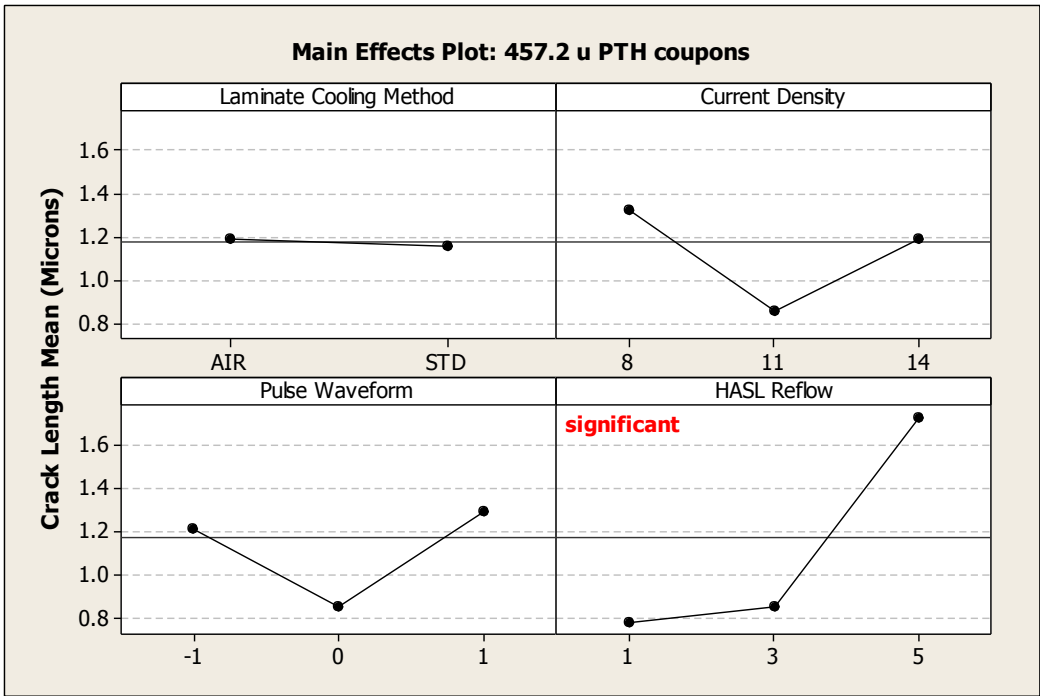

Figure 11 - Main Effects Plot: Maximum Crack Length (457.2 µm PTH coupons)

Figure 12 indicates that current density, HASL reflow, and the interaction effect, laminate cooling method*current density, are significant for maximum crack length for 635 µm PTHs.

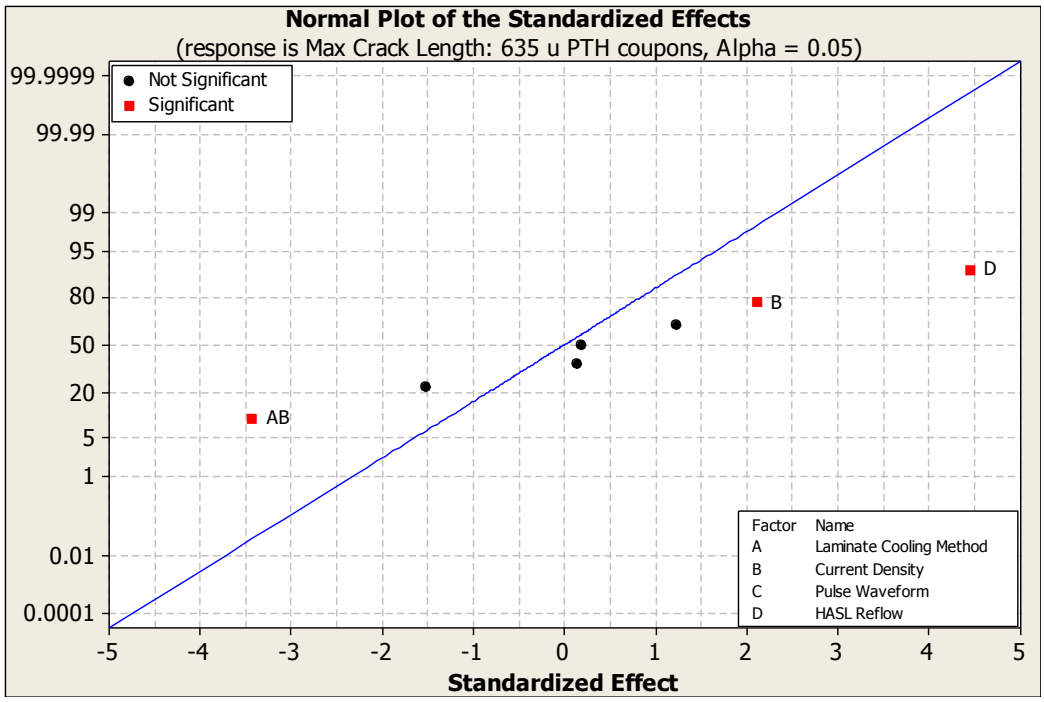

Figure 12 - Normal Probability Plot of the Effects: Maximum Crack Length (635 µm PTH coupons)

Figure 13 indicates that one HASL Reflow is preferred for 635 µm PTHs, which corresponds with the optimal recommendations in Table 3. The significant interaction effect, identified in Figure 12, is interpreted by reviewing Figure 14.

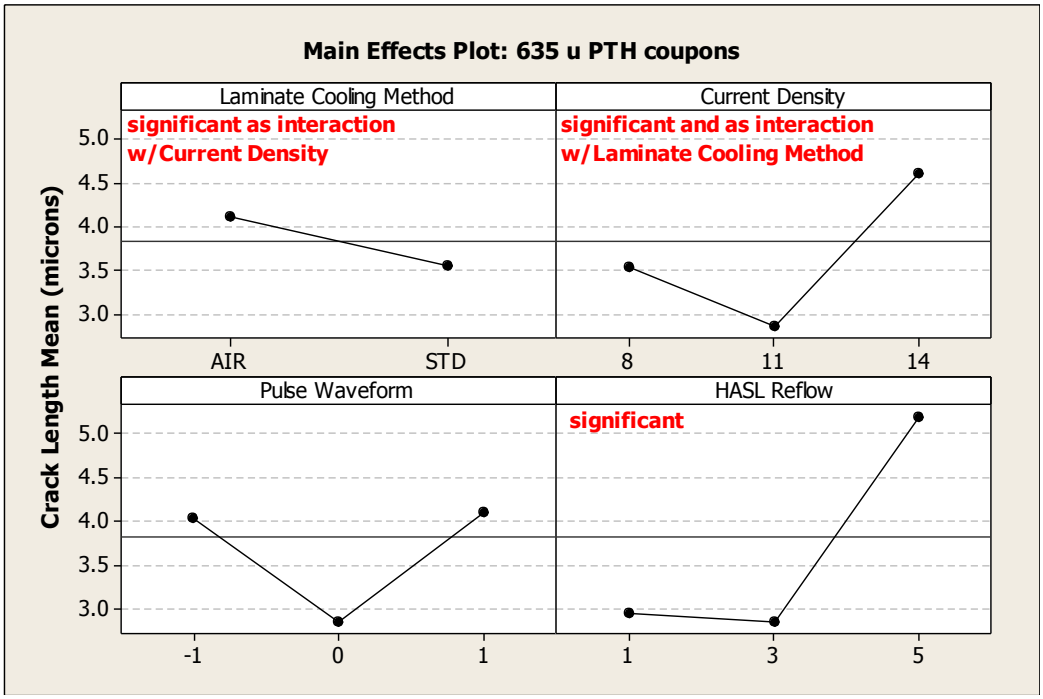

Figure 13 - Main Effects Plot: Maximum Crack Length (635 µm PTH coupons)

The laminate cooling method*current density interaction is shown in Figure 14. Interactions are evident when lines connecting the mean values are not parallel, and a stronger effect is indicated by intersecting lines. In other words, the resultant mean is interrelated between two (or more) factor settings. Since this DOE is a screening design, only second-order interactions are analyzed. For water cooling, only current density 14 is statistically different (in this instance worse) than either current density 8 or 11, which are not statistically different. To minimize cracking for 635 µm PTHs, water cooling is recommended in conjunction with current density 8 or 11. Thus, the optimal recommendations based on all locations, water cooling with current density 8 as presented in Table 3 remain substantiated.

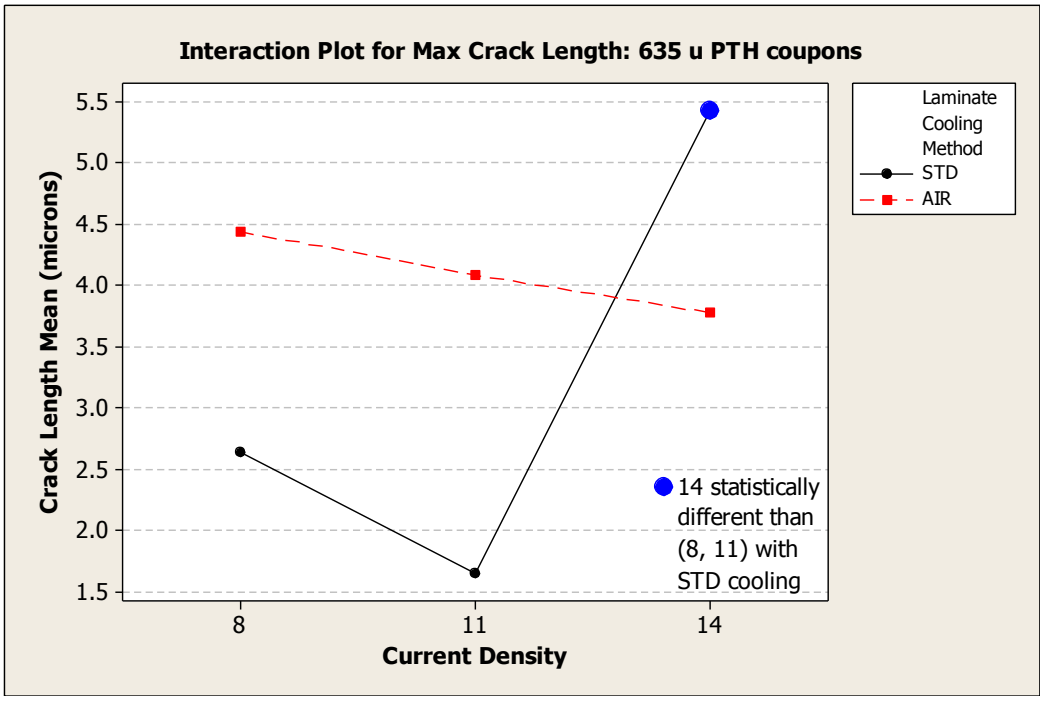

Figure 14 - Interaction Plot (Laminate Cooling Method*Current Density): Maximum Crack Length (635 µm PTH coupons)

Figure 15 indicates that pulse waveform, laminate cooling method, and the interaction effect, laminate cooling method*current density, are significant for maximum crack length for buried vias.

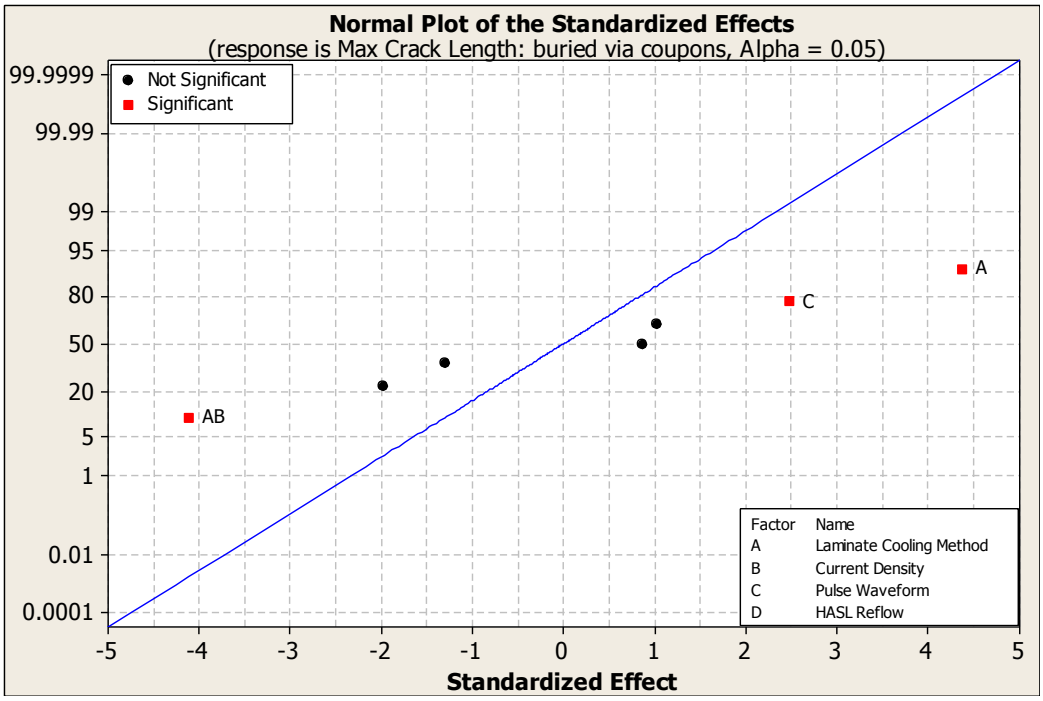

Figure 15 - Normal Probability Plot of the Effects: Maximum Crack Length (buried via coupons)

Figure 16 indicates that the water cooling method and a pulse waveform not equal to a setting of 1 are preferred for buried vias, which corresponds with the optimal recommendations in Table 3.

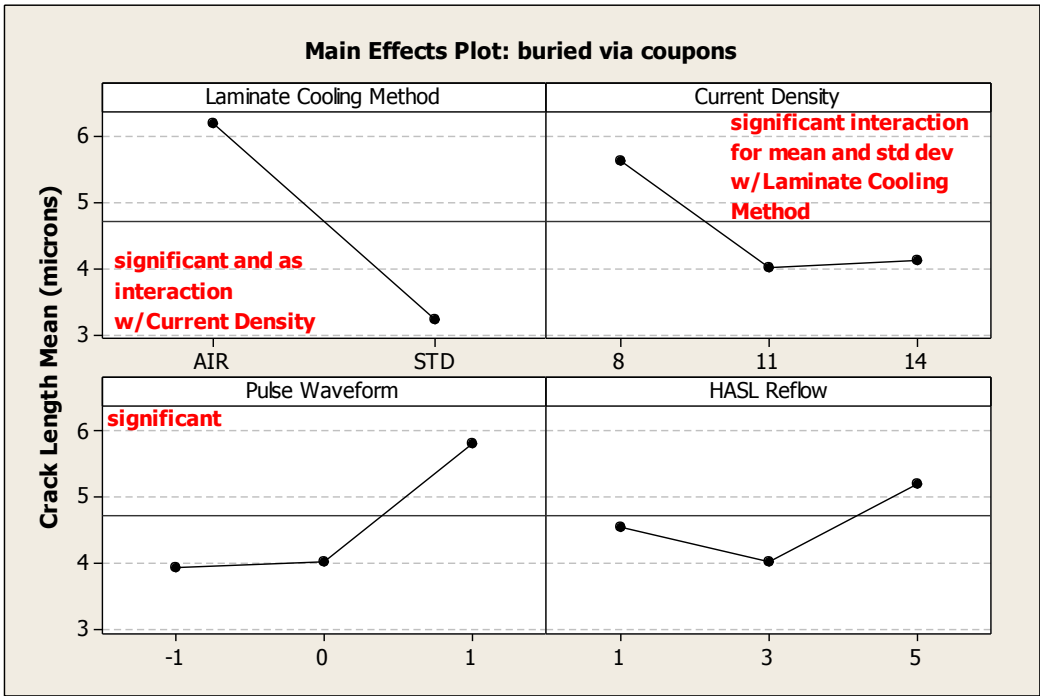

Figure 16 - Main Effects Plot: Maximum Crack Length (buried via coupons)

The laminate cooling method*current density interaction is shown in Figure 17. This interaction also impacted the maximum crack length standard deviation, as shown in Figure 18. For standard cooling, the current density settings (8, 11, 14) are not statistically different. Thus, the optimal recommendations based on all coupon locations, standard cooling with current density 8, as presented in Table 3, remain substantiated.

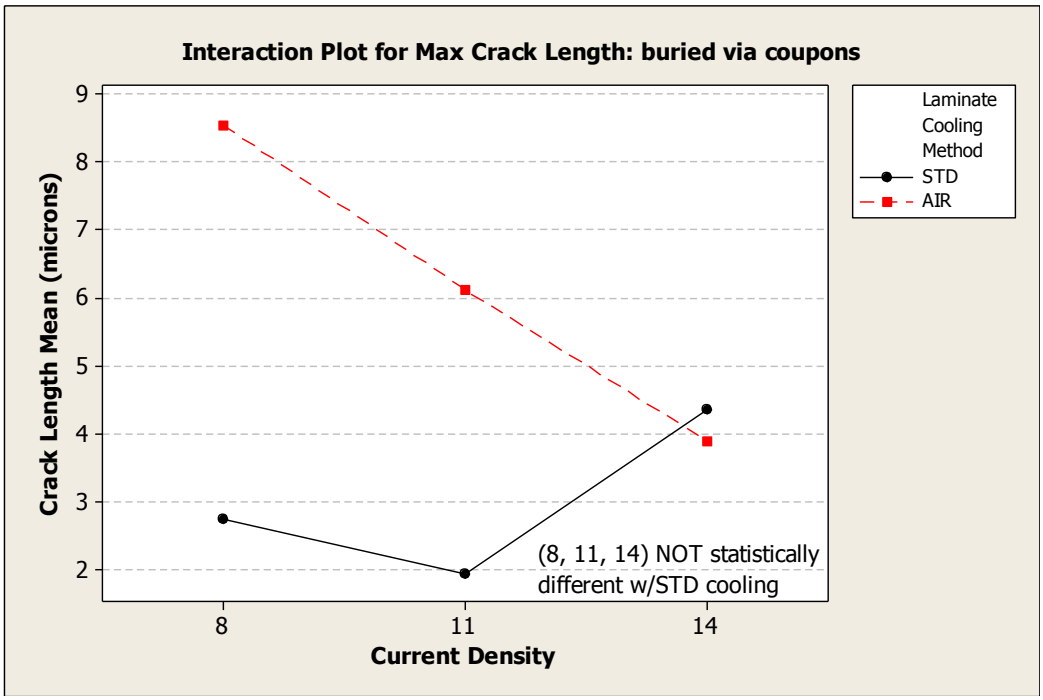

Figure 17 - Interaction Plot (Laminate Cooling Method*Current Density): Maximum Crack Length (buried via coupons)

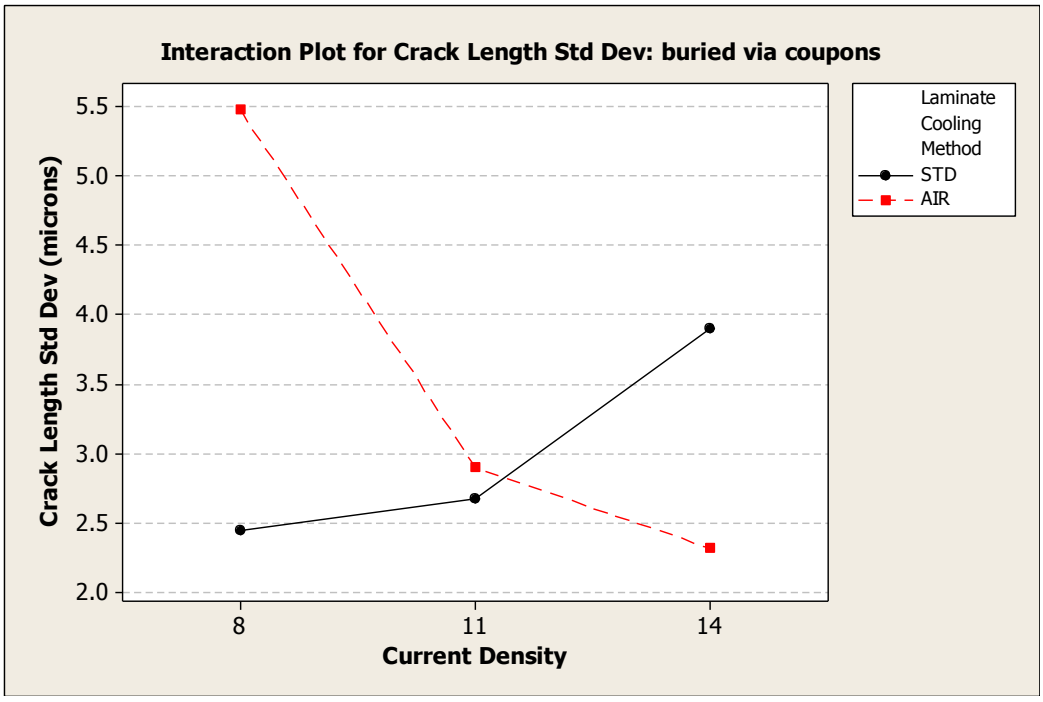

Figure 18 - Interaction Plot (Laminate Cooling Method*Current Density): Maximum Crack Length Std Dev (buried via coupons)

Conclusions and Summary

The research identified PCB fabrication processes that were significant contributors to not only the incidence of cracks but also the length of cracks, in copper plated vias, after exposure to thermal shock excursions. Statistical analyses of the resultant DOE data identified the optimal settings for the four factors selected from the PCB fabrication processes.

The binary logistic regression indicated that the likelihood of cracking increased from 220% to 561% across all via types when changing from water laminate cooling to air cooling within the same number of HASL reflow cycles. Since the plating

is performed after the laminate cooling process, the influence of the laminate cooling process on the likelihood of cracking is not readily apparent. Also, as the number of HASL reflows increased, the likelihood of crack occurrence increased from 25% to 77% across these via types, when holding the laminate cooling method constant. These results support the optimal recommendations of water cooling with HASL reflow of 1, as presented in Table 3.

For 457.2 µm PTH, the only significant factor affecting crack length was the HASL reflow.. For the 635 µm PTH, HASL reflow was also the most significant factor on the length of barrel cracks. Other significant factors included current density and the second-order interaction effect between the laminate cooling method and current density. Figure 3 response slopes suggested a current density setting of 8 would reduce crack length and standard deviation, notably due to the interaction plot shown in Figure 14, where a setting of 14 coupled with standard water cooling should be avoided. For buried vias, laminate cooling method (air) was the most significant factor affecting the length of barrel cracks, even though the plating is performed after the laminate cooling process. Pulse waveform setting of 1 was the second most significant factor. Other significant factors included the second-order interaction effect between the laminate cooling method and current density, shown by Figure 17 and Figure 18, for the crack length average and standard deviation, respectively. This interaction effect further substantiated the optimal recommendations of standard cooling with current density 8, as presented in Table 3.

While the DOE was being conducted, the no-crack thermal shock requirement was reviewed for applicability against service life requirements. Multiple PCB coupon samples underwent close to 100 thermal shock cycles to determine when cracks initiated and to estimate crack growth rates. Engineering models estimated the service life correlating with 100 thermal cycles. This effort resulted in a relaxation of the crack criteria to allow up to 20% crack length of the specified minimum wall thickness.

Future

Based on the results of this DOE, a follow-on experiment is desirable. Specifically, some of the variables under consideration include HASL versus hot oil reflow, conductive versus nonconductive buried via fill, and pulse waveform variation while keeping plating thickness controlled.

Acknowledgments

This work was conducted under funding from the U.S. Navy Strategic Systems Programs Office to The Charles Stark Draper Laboratory under Contract Number N00030-13-C-0005. The authors thank Ted Jones and Matthew McQueen and their team at the Crane Division, Naval Surface Warfare Center for their outstanding contribution in providing input to the design of this experiment, preparation and inspection of all coupons, as well as data recording.. Also, we thank Carl Colangelo of The Dow Chemical Company for his assistance with the DOE and his expertise in interconnect processes. The team at Viasystems Sterling should be commended for their dedication in preparing and executing the details of the manufacturing plan that satisfied the elements of this DOE.