PRACTICAL VERIFICATION OF VOID REDUCTION METHOD FOR BTC USING EXPOSED VIA IN PAD

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ABSTRACT
Void reduction strategies used with different levels of success throughout the industry include managing reflow profile parameters, solder paste deposit volume and solder paste type, stencil aperture cut to different geometries, thermal pad geometries with and without solder mask webs, vacuum assisted reflow, sweep stimulation of PCB substrate, use of solder preforms, tinning of the components pads prior to placement and reflow, I/O aperture design to overprint at the toe of the pad, and exposed via in pad [1-8]. Translation of these methods and their combinations for void control on the thermal pad of bottom terminated components (BTC) has met with different levels of success in volume production.
The method explored in this paper regards the use of exposed via in pad. A dedicated test vehicle was designed for two types of QFN components. The main variables taken into account were the component size, number of exposed via in the thermal pad, via pitch, via size, and solder paste coverage. The responses sought in this experiment include thermal pad void level and solder wicking down the via barrel with resulting solder protrusion on the opposite side of the PCB.
The results indicated that solder will wick down the exposed via in pad regardless of the via diameter and solder paste coverage. Despite this finding, there were no defects recorded like component tilting, skewing, opens, or solder bridging. Specific configurations attained voiding levels in the thermal pad below 25%; however, other configurations did show void level for the thermal pad up to 50%. A discussion will be presented regarding the effect of the board thickness and the geometry of the via array on the thermal pad solder coverage and voiding level.

Key words: BTC, PTH, void, lead free

INTRODUCTION

It has been hypothesized that a small enough (≤10 mils drill size prior to plating) diameter for an exposed via/plated through hole (PTH) would prevent molten solder from wicking down the vias, while allowing volatiles developed during solder reflow to escape and minimize the size of the voids at the thermal pad of BTC. The follow-up questions were if void size would vary when solder is printed intentionally over such exposed via in pad, and how it would compare with the case when the solder paste is deposited between the exposed vias.

Starting from the hypothesis, Figure 1 shows a brief review of the force equilibrium of a finite volume of solder emerging in an exposed via in pad; the height of the solder column turns out to be a function of the contact angle and the size of the finished via. Figure 1 assumes the case of a wettable surface inside the PTH.

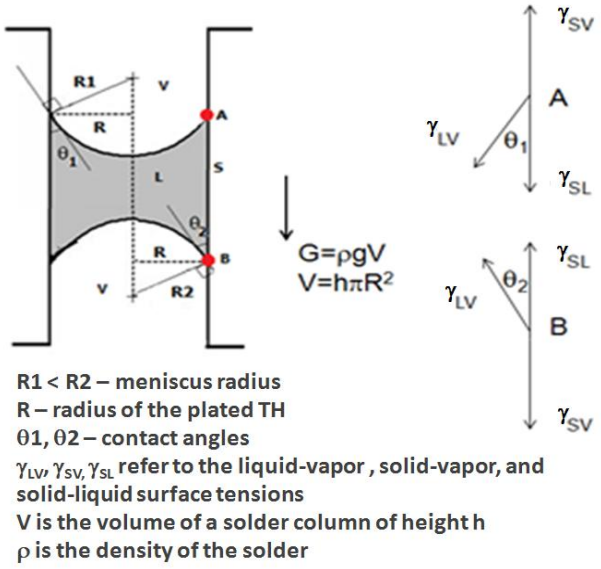


Figure 1: Equilibrium of forces acting on a finite volume of solder inside an exposed via.

At equilibrium, the height h of the solder column is described by the equation (1):

From a soldering application viewpoint, equation (1) has no practical application; when solder reaches the TH exposed via, solder will wick down the via according with the wetting ability, amount of the solder available and heating/cooling conditions. However, it is interesting to use equation (1) and question what conditions would allow the height of the solder column h to be minimized or made zero:

- if the solder does not wet the via (via not plated)
- if $\theta_1 = \theta_2$ (absence of gravity)
- if $\theta_1 = \theta_2 = 90°$ (cannot be a natural solution)

Since these three conditions cannot be satisfied for exposed plated through vias, and due to the relationship between the

supposed height h of the solder column and the radius R of the exposed plated via, it seems unlikely that it is possible to prevent solder from wicking down a wettable plated via for any via size, regardless how small its practical finished size diameter may be.

Back-of-the-envelope calculations aside, a practical verification is required to fully verify the hypothesis. For this purpose, a test vehicle was designed and parameters calculated as described below.

EXPERIMENTAL FINDINGS

Test Vehicle

Experimental approach was to design a test board having various PTH via diameters and via arrays, design the stencils such that solder paste is either printed over vias or between vias, fabricate the boards with different thicknesses, and after assembly tally the vias with solder, void percentage and the solder protruding from vias.
If the hypothesis is proven, then voiding in thermal pad is minimized, heat transfer is optimized and the components will present uniform solder joints stand-off height. Otherwise, the factors leading to solder wicking down the exposed vias could be the following:

- volume and location of the printed solder
- solderability of the finished via
- solder wetting ability
- presence of barriers (solder mask webs)
- temperature values and temperature gradients
- solder availability (surface tension forces equilibrium conditions between TH via, board surface and component surface)

Board outline:

- 224 mm x 170 mm size, 4 layers, ImAg finish
- PTH vias in thermal pad are fully connected with all layers
- 3 different boards thicknesses: 93 mils (2.36 mm), 110 mils (2.8 mm), and 130 mils (3.3 mm)
- 1 type 0.4 mm pitch QFN component and 1 type 0.5 mm pitch QFN component
- 2x2, 5x5 and 8x8 matrix of PTH exposed via in thermal pad
- 2 solder mask designs (w/ and w/o solder mask doughnut around vias)

Via diameters are chosen such that:
Φ1<Φ2<Φ3 are drills outer diameters (OD):

- Φ1 = 0.2 mm ~ 0.00787”
- Φ2 = 0.23 mm ~ 0.00905”
- Φ3 = 0.25 mm ~ 0.0098”

Although two component types populated the board, only the 10 mm x 10 mm, 0.4 mm pitch QFN component is discussed here.

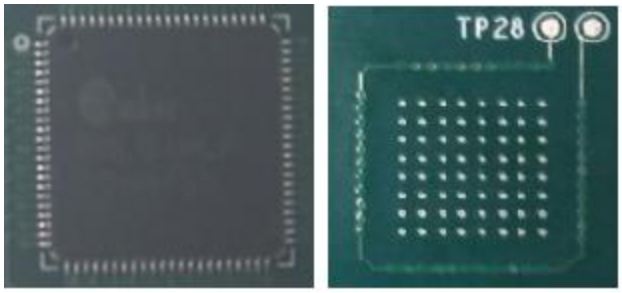


Figure 2: A-MLF88-10mm-.4mm-Sn, top and bottom side view on the board.

Figure 2 diagram shows a component (A-MLF88-10mm-.4mm-Sn) with 88 leads, 177.1 x 177.1 mils die size, 8.3 x 8.3 mm thermal pad size.

The finalized test board concept is described in Figure 3:

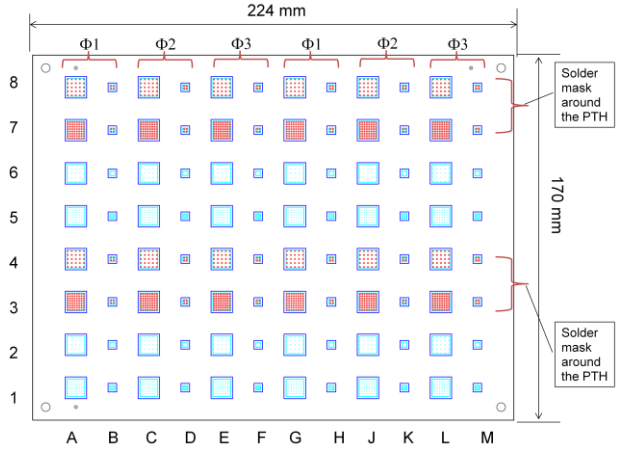


Figure 3: Test board.

Locations with solder mask doughnut around vias are highlighted in Figure 3 and appear at all reference designators in lines 3, 4, 7 and 8 highlighted in red color. The test board has symmetry and each set of characteristics are repeated four times on each board.

Stencil designs

Two stencils were calculated to provide a minimum of 50% solder paste coverage. Stencils used were NiCut with a thickness of 4 mils.

Solder paste coverage was calculated according to IPC-7093 by considering the solderable surface area to not include open, filled or solder mask encroached vias. The calculated and measured solder paste coverage values for the two stencils are given in Table 1. Stencil A was used to print solder paste dots (between vias), stencil B was used to dispense solder paste segments (over vias) – example shown in Figure 4.

Table1: Solder paste coverage.

Reference Designators	Solder mask (Yes-1, No-0)	Solder mask area/via area (mil2)	Number of vias	Stencil A aperture radius (mils)	Stencil A: number of apertures	Stencil B aperture length (mils)	Stencil B: number of apertures	Stencil A: solder paste coverage %		Stencil B: solder paste coverage %	
								calculated	measured (SPI)	calculated	measured (SPI)
A8,A4,G8,G4	1	531	25	34	16	53	25	61	61-63	76	76-79
C8,C4,J8,J4	1	573	25	32	16	53	25	54	55-57	76	77-80
E8,E4,L8,L4	1	616	25	34	16	53	25	62	62-65	77	76-84
A7,A3,G7,G3	1	531	64	17	49	70	16	58	59-64	108	107-113
C7,C3,J7,J3	1	573	64	16	49	70	16	56	57-61	113	113-117
E7,E3,L7,L3	1	616	64	15	49	70	16	55	56-61	117	119-123
A6,A2,G6,G2	0	49	25	35	16	53	25	60	58-63	67	68-70
C6,C2,J6,J2	0	64	24	35	16	53	25	60	59-63	67	68-70
E6,E2,L6,L2	0	75	25	35	16	53	25	60	59-63	67	68-70
A5,A1,G5,G1	0	49	64	20	49	70	16	58	59-64	76	75-79
C5,C1,J5,J1	0	64	64	20	49	70	16	58	59-65	77	75-80
E5,E1,L5,L1	0	75	64	20	49	70	16	59	59-67	77	77-80

Some calculated and measured solder paste coverage values for stencil B show values above 100% for 8x8 via arrays; this is the case where the solderable surface area has a smaller value (due to the presence of more exposed vias with solder mask doughnut) than the total printed area.

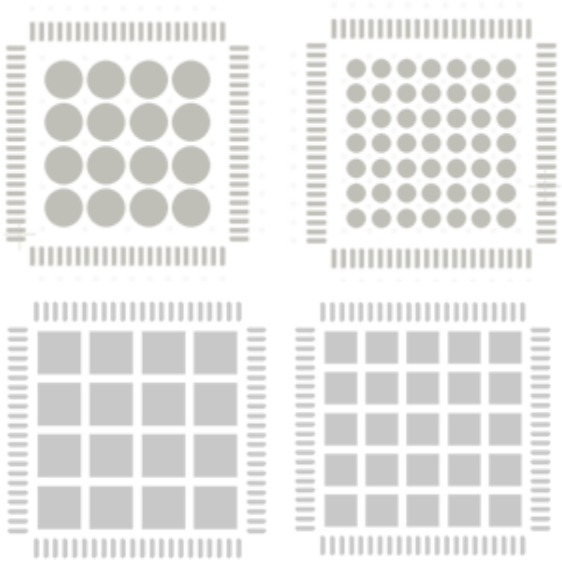


Figure 4: Dot and segmented apertures example.

Experiment design and assembly parameters

18 boards, 9 for each stencil type, 3 for each board thickness were assembled in a lead free process using SAC305 solder paste and reflow profiles according to each board thickness. Table 2 describes the experiment factors. Table 3 lists the assembled boards characteristics.

Table 2: DOE.

Factors	Levels	Values	Response
Board thickness	3	93	- Number of PTH with solder wicked in. - Number of solder protrusions. - Void%
		110	
		130	
Stencil apertures	2	Segmented	
		Dots	

Table 3: List of assembled boards.

Board number	Board thickness (mils)	Stencil number	Aperture type
1	93	B	segmented
2	93	B	segmented
3	93	B	segmented
4	110	B	segmented
5	110	B	segmented
6	110	B	segmented
7	130	B	segmented
8	130	B	segmented
9	130	B	segmented
10	93	A	dots
11	93	A	dots
12	93	A	dots
13	110	A	dots
14	110	A	dots
15	110	A	dots
16	130	A	dots
17	130	A	dots
18	130	A	dots

Reflow profiles

A summary of the reflow profiles parameter ranges measured at 12 different locations for each board thickness is shown in Table 4. The reflow oven parameters (zone temperature, conveyor speed) were adjusted such that the reflow parameters for QFN components were highly comparable regardless of the board thickness. In this case profiling for different thickness boards was not challenging since the boards are populated on one side only.

Table 4: Reflow parameters.

Board thickness (mils)	Rise time (s) (130÷217°C)	Risetime (s) (50C÷T_{peak})	TAL(°C)	T_{peak} (°C)	Negative slope (°C/s)
93	126÷135	274÷284	69÷86	240÷246	-1.6÷-2.1
110	123÷127	285÷293	73÷87	239÷247	-1.8÷-2.7
130	124÷128	277÷288	74÷85	240÷247	-1.4÷-2.3

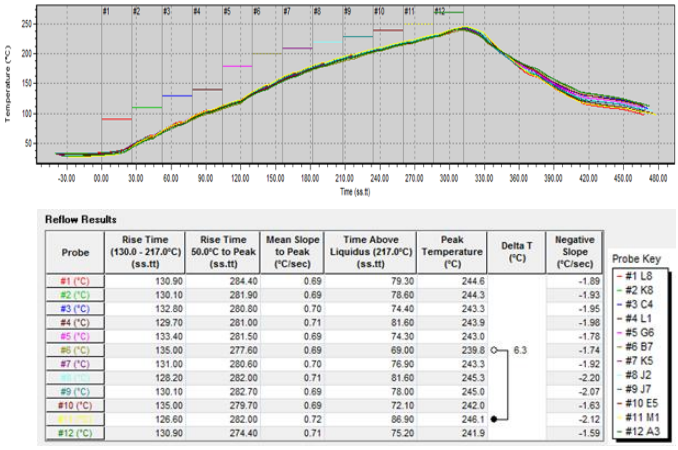
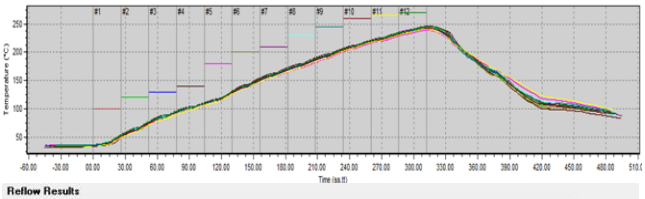


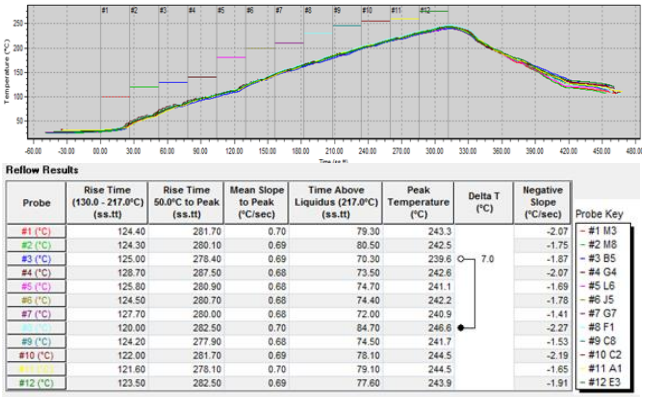
Figure 5: 93 mils thick board – reflow profile.



Reflow Results

Probe	Rise Time (130.0 - 217.0°C) (ss.tt)	Rise Time 50.0°C to Peak (ss.tt)	Mean Slope to Peak (°C/sec)	Time Above Liquidus (217.0°C) (ss.tt)	Peak Temperature (°C)	Delta T (°C)	Negative Slope (°C/sec)	Probe Key
#1 (°C)	126.30	286.40	0.67	81.00	242.9		-1.91	#1 J1
#2 (°C)	126.40	290.10	0.68	81.20	242.8		-2.06	#2 A4
#3 (°C)	126.80	290.30	0.67	78.40	242.8		-1.89	#3 G2
#4 (°C)	123.30	293.10	0.69	87.70	245.8		-2.69	#4 B6
#5 (°C)	127.10	286.00	0.66	73.90	239.3	7.4	-1.67	#5 A6
#6 (°C)	125.60	292.40	0.68	83.20	244.3		-2.65	#6 L3
#7 (°C)	122.10	288.00	0.70	86.60	246.7		-2.37	#7 B1
#8 (°C)	124.70	291.30	0.69	84.60	245.3		-2.31	#8 F5
#9 (°C)	125.30	292.00	0.68	82.60	245.5		-2.83	#9 F7
#10 (°C)	126.50	289.50	0.67	81.60	242.3		-1.88	#10 L5
#11 (°C)	125.00	284.90	0.68	76.80	240.8		-1.80	#11 C7
#12 (°C)	123.80	291.40	0.69	85.40	245.7		-2.24	#12 J8

Figure 6: 110 mils thick board – reflow profile.



Reflow Results

Probe	Rise Time (130.0 - 217.0°C) (ss.tt)	Rise Time 50.0°C to Peak (ss.tt)	Mean Slope to Peak (°C/sec)	Time Above Liquidus (217.0°C) (ss.tt)	Peak Temperature (°C)	Delta T (°C)	Negative Slope (°C/sec)	Probe Key
#1 (°C)	124.40	281.70	0.70	79.30	243.3		-2.07	#1 M3
#2 (°C)	124.30	280.10	0.69	80.50	242.5		-1.75	#2 M8
#3 (°C)	125.00	278.40	0.69	70.30	239.6	7.0	-1.87	#3 B5
#4 (°C)	128.70	287.50	0.68	73.50	242.6		-2.07	#4 G4
#5 (°C)	125.80	280.90	0.68	74.70	241.1		-1.69	#5 L6
#6 (°C)	124.50	280.70	0.68	74.40	242.2		-1.78	#6 J5
#7 (°C)	127.70	280.00	0.68	72.00	240.9		-1.41	#7 G7
#8 (°C)	120.00	282.50	0.70	84.70	246.6		-2.27	#8 F1
#9 (°C)	124.20	277.90	0.68	74.50	241.7		-1.53	#9 C8
#10 (°C)	122.00	281.70	0.69	78.10	244.5		-2.19	#10 C2
#11 (°C)	121.60	278.10	0.70	79.10	244.5		-1.65	#11 A1
#12 (°C)	123.50	282.50	0.69	77.60	243.9		-1.91	#12 E3

Figure 7: 130 mils thick board – reflow profile.

SPI inspection data

Solder paste inspection (SPI) data was acquired for each component. For the thermal pad the apertures were numbered and each solder paste deposit was measured against the calculated target value based on the apertures' sizes.

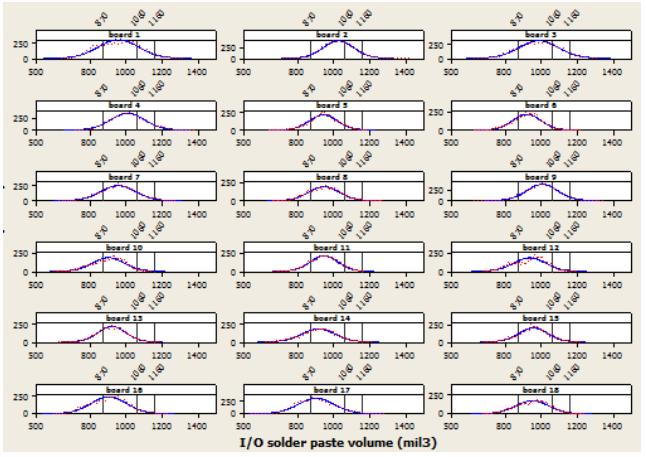


Figure 8: I/O solder paste volume by board.

For the components leads, the apertures were reduced 10%. The I/O were not overprinted so that upon melting and coalescence the solder paste deposits would not lift the component and inadvertently interfere with the experiment hypothesis. The solder paste volume distribution for the I/O is shown in Figure 8. The mean of each distribution is slightly less than the target value of 1060 mil^3 of solder paste.

For the solder paste deposits on the thermal pad is of interest to evaluate the area distributions by aperture for stencil A only to check if any solder deposit intersects the via land.

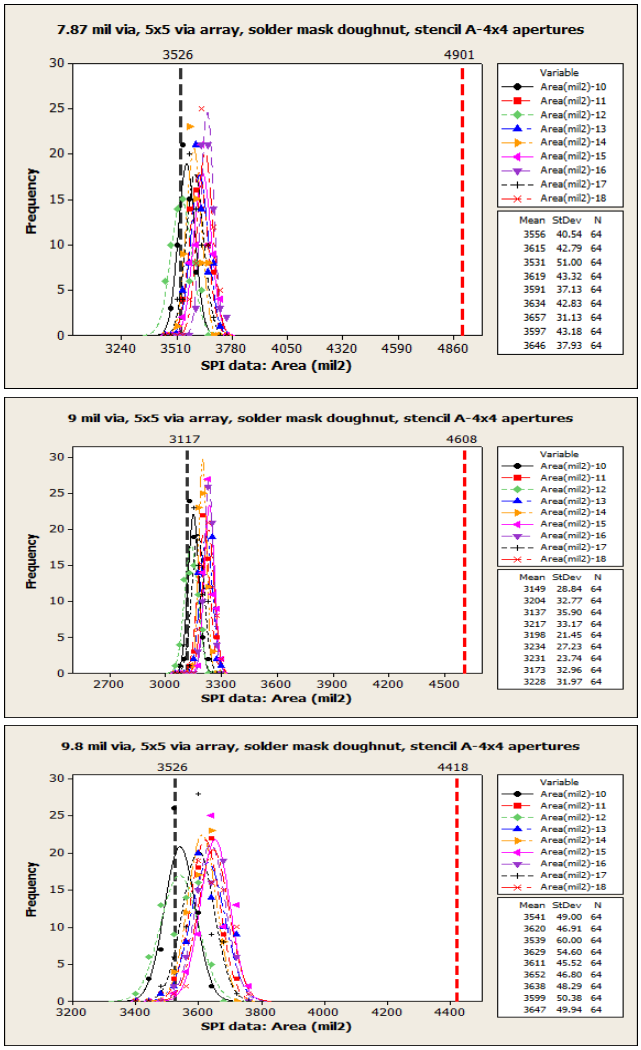


Figure 9: Thermal pad solder paste area distribution/single dot paste deposit – 5x5 via array, with solder mask doughnut.

The distributions in Figure 9 indicate slight overprinting (median is above the target value indicated by the black dotted line), however the solder paste area is well below the value which would indicate contact of the solder paste with any of the via placed in the thermal pad.

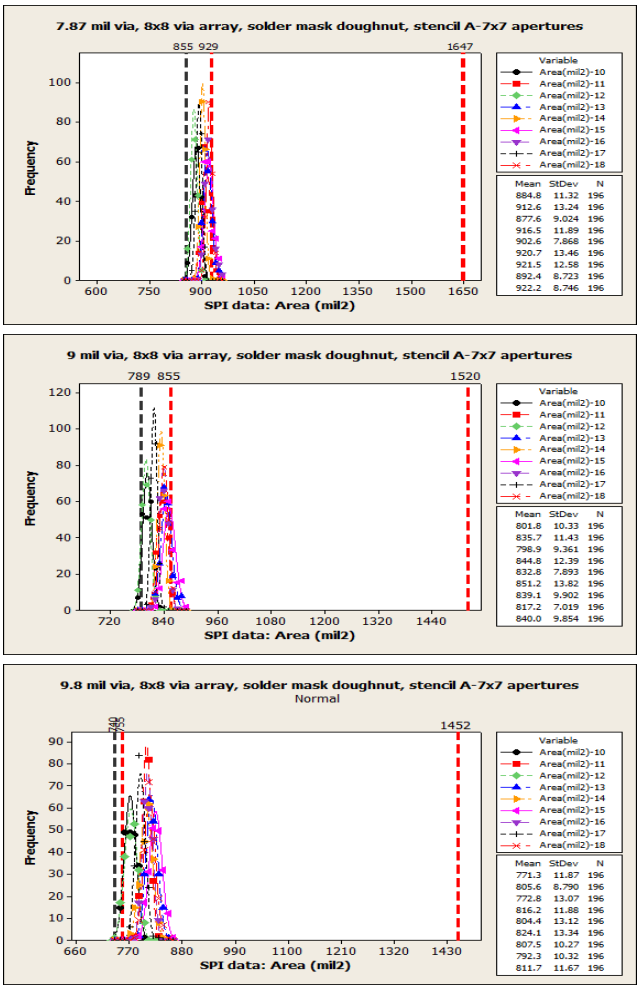
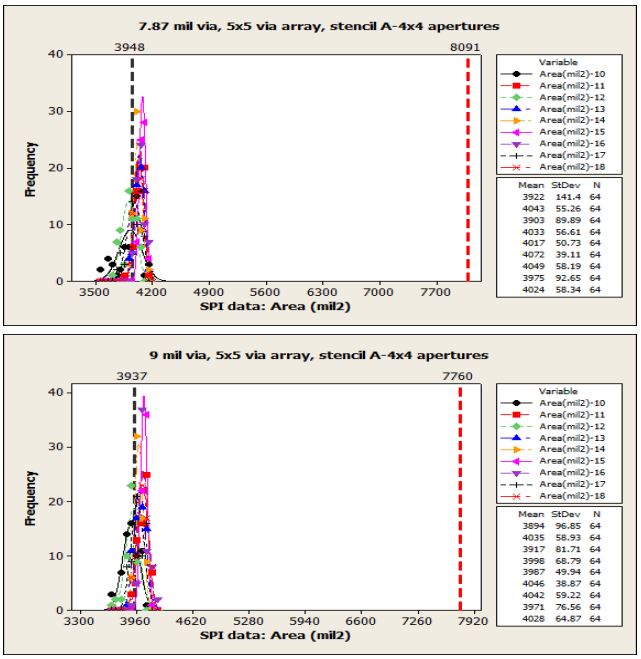


Figure 10: Thermal pad solder paste area distribution/single dot paste deposit – 8x8 via array, with solder mask doughnut.



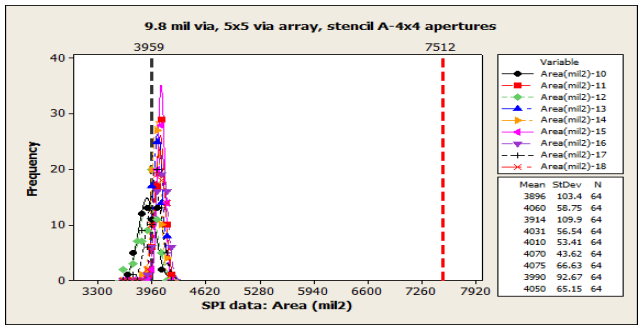


Figure 11: Thermal pad solder paste area distribution/single dot paste deposit – 5x5 via array.

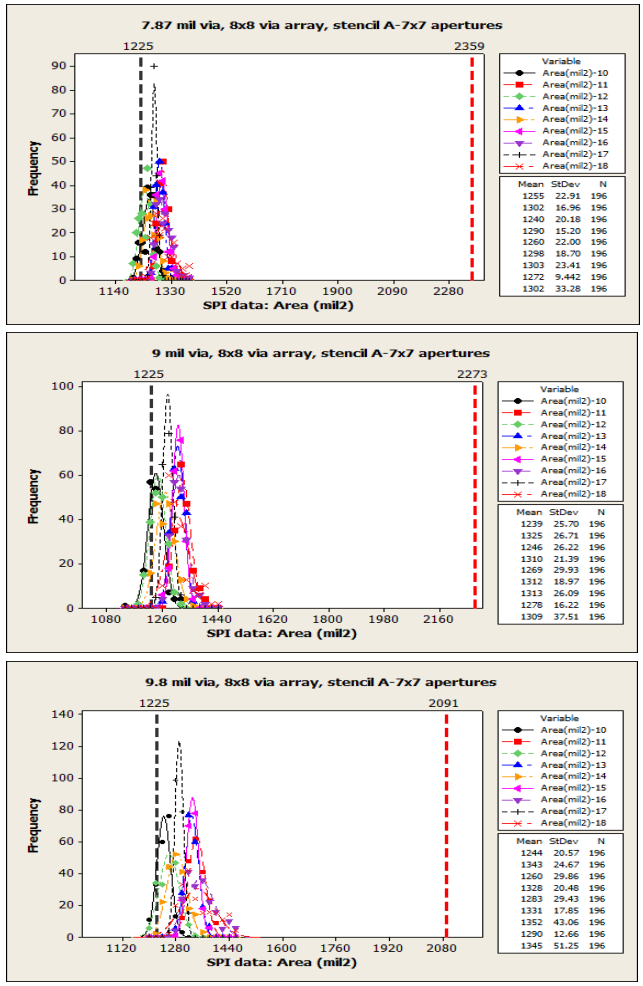


Figure 12: Thermal pad solder paste area distribution/single dot paste deposit – 8x8 via array.

The distributions in Figure 10 indicate slight overprinting (median is above the target value indicated by the black dotted line), however the solder paste area is well below the value which would indicate contact of the solder paste with any of the via placed in the thermal pad. The red dotted line adjacent to the reference line was introduced to indicate that solder area overlaps with the solder mask doughnut around the via, but does not overlap with the via

landing (red dotted reference line at the far right side of the graph).

Figures 11 and 12 show the solder paste area distributions for reference designators that do not have the solder mask doughnut around each via in the thermal pad. These paste deposits also appear to not intersect the via similar to the distributions in Figures 9 and 10. Any solder paste that would wick in the via after component placement and reflow would not be the direct result of the solder printed too close to the via or the via landing when stencil A is used.

The solder paste distributions for the segmented stencil, stencil B) were verified and the values meet the targets. Only one graph was included here because in the case of stencil B the solder paste was intentionally printed over the vias. Details of the solder paste coverage are included for each reference designator in Table 1.

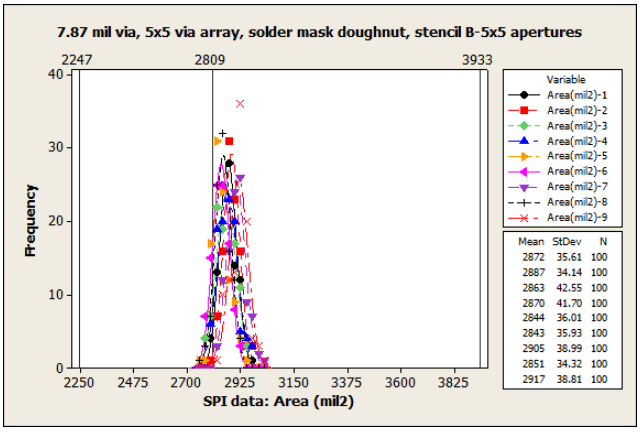


Figure 13: Thermal pad solder paste area – stencil B

AXI inspection data

Automated X-ray inspection (AXI) was done for each board, images were saved for each component, and an automated void % value was provided. Because the via diameter and the total solderable area are variable, the reported void % was adjusted to reflect each case.

Raw void % data did not consider the actual solderable area of the thermal pad, and it removed the plugged via area from under the void. The formula used to correct the raw void % numbers is:

$$\mathbf{Void\%_{corrected}} = \frac{\mathbf{A_{thermal\ pad}} \times \frac{\mathbf{Void\%}}{\mathbf{100}} - \mathbf{N_{empty\ vias}} \times \mathbf{A_{via}}}{\mathbf{A_{thermal\ pad}} - \mathbf{N_{vias}} \times \mathbf{A_{via}}} \qquad (2)$$

- $A_{thermal\ pad}$ is the total area of the thermal pad, in this case 8.3 mm x 8.3 mm.
- A_{via} is the area of via opening, or the solder mask around the via opening, as applies.
- Void% is the as reported value
- $Void\%_{corrected}$ is the void value after the total solderable area is considered.
- $N_{empty\ vias}$ is the number of vias with no solder plugs intersecting a void.

Upon correction, some as reported void% values changed to either increase or decrease the void% depending on the solderable area, number of vias in the thermal pad and the number of vias plugged with solder due to printing and reflow.

An analysis of the main effects interactions shows the average void % dependencies as described in Figure 14.

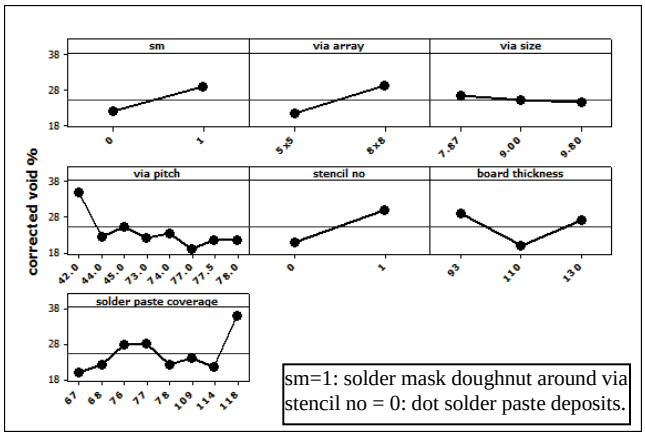


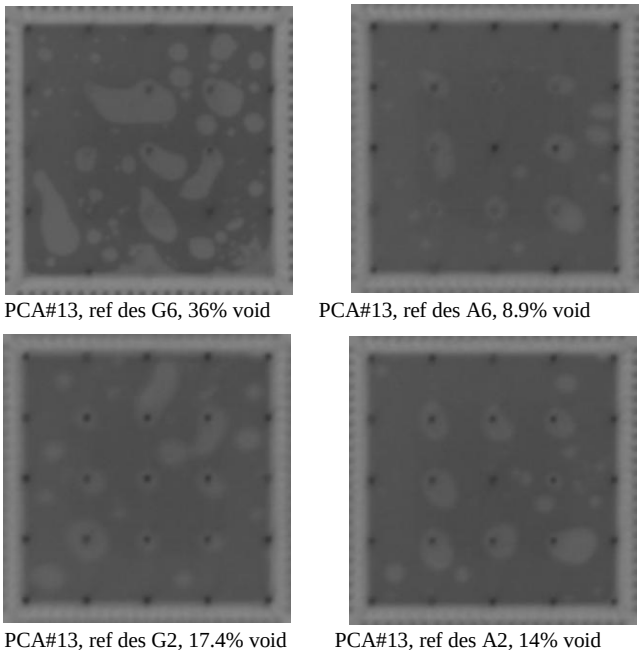
Figure 14: Main effects of solder mask (sm), via array, via size, via pitch, stencil type (dot=0, segmented=1), board thickness and solder paste coverage on the corrected void% means.

In terms of significance, all the factors considered for the main effects interactions are calculated to be significant, including some of the second order interactions. As expected the average void% decreases with increased via pitch, for a lower number of vias, and with increasing via size.

Table 5: Tally of corrected void% range by board (sm=1: solder mask doughnut around via).

	PCA#	Void%<25%		50%>Void%>25%		Void%>50%	
		sm=1	sm=0	sm=1	sm=0	sm=1	sm=0
Segmented solder paste deposits (stencil no=1)	1	3	13	10	11	11	0
	2	4	12	10	12	10	0
	3	4	15	13	9	7	0
	4	6	16	12	8	6	0
	5	8	22	13	2	3	0
	6	6	21	16	3	2	0
	7	5	10	16	14	3	0
	8	9	12	14	12	1	0
	9	5	16	16	8	3	0
Dot solder paste deposits (stencil no=0)	10	13	14	11	10	0	0
	11	9	17	15	7	0	0
	12	14	16	10	8	0	0
	13	24	22	0	2	0	0
	14	24	22	0	2	0	0
	15	24	22	0	2	0	0
	16	14	15	10	9	0	0
	17	13	16	11	8	0	0
	18	14	13	10	11	0	0

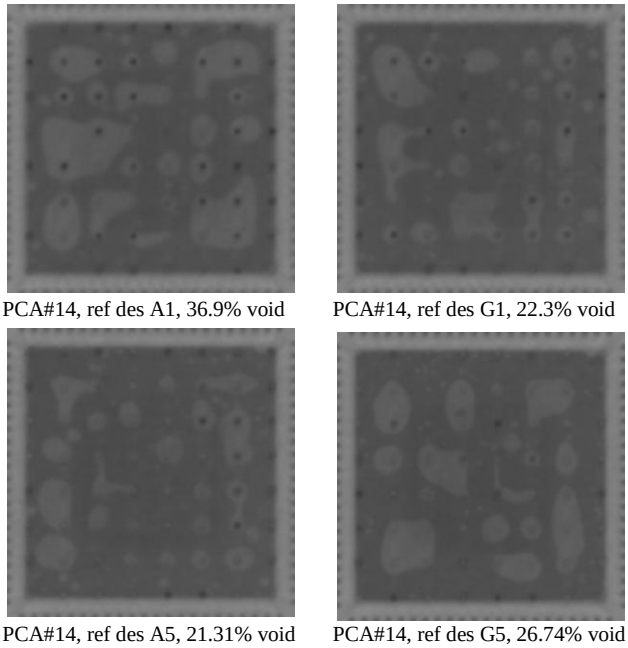
It is less intuitive to see that the average void size increased when solder mask doughnut is present around vias. For this reason a tally by board and void% range was compiled in Table 5 above, which shows that PCA # 13,14 and 15 have the optimized outcomes in terms of voiding: all void on these 110 mil thick boards assembled with dot solder paste deposits is below 50%. For each of these 3 boards only two reference designators show values between 25% and 40% void.



PCA#13, ref des G6, 36% void PCA#13, ref des A6, 8.9% void

PCA#13, ref des G2, 17.4% void PCA#13, ref des A2, 14% void

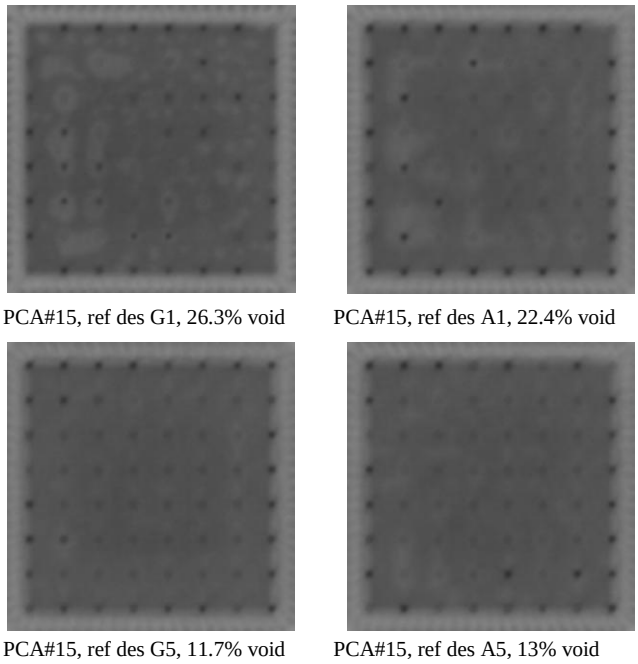
Figure 15: PCA#13 corrected void percentage for reference designator G6 (via diameter Φ1 = 0.2 mm ~ 0.00787").



PCA#14, ref des A1, 36.9% void PCA#14, ref des G1, 22.3% void

PCA#14, ref des A5, 21.31% void PCA#14, ref des G5, 26.74% void

Figure 16: PCA#14 corrected void percentage for reference designator A1 (via diameter Φ1 = 0.2 mm ~ 0.00787").



PCA#15, ref des G1, 26.3% void PCA#15, ref des A1, 22.4% void

PCA#15, ref des G5, 11.7% void PCA#15, ref des A5, 13% void

Figure 17: PCA#15 corrected void percentage for reference designator G1 (via diameter Φ1 = 0.2 mm ~ 0.00787").

These reference designators do not have solder mask doughnut around vias. Figures 15, 16 and 17 show these reference designators, and the other 3 identical locations on each board.

Other inferences based on Table 5 data:

- No solder mask doughnut around the vias allows for void <50% for all cases.
- For void% range of 25% ÷ 50%, and for void % <25% the most favorable case is solder mask doughnut around via and board thickness 110 mils, with solder paste dots.
- For void % < 25%, when solder dot paste stencil is used, the presence or absence of solder mask doughnut is indifferent; same number of components show <25% voiding. Also, there are no cases of void%>50%; the largest void size is 44% for the 9 boards assembled with the dot solder paste deposit stencil.
- For void % < 25%, when segmented solder paste stencil is used, the absence of solder mask doughnut yields at least twice as many components with <25% voiding.

Post assembly, it was observed that solder paste wicked in the vias and some protruded on the back side of the board. An SPI program was developed to measure the solder paste protrusions height. The results of the post assembly SPI inspection, shown in Figure 18, were analyzed based on the main interactions, similar to the void% main interactions analysis.

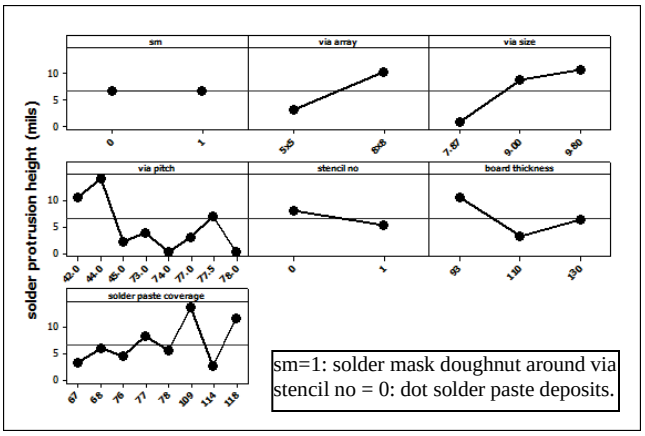
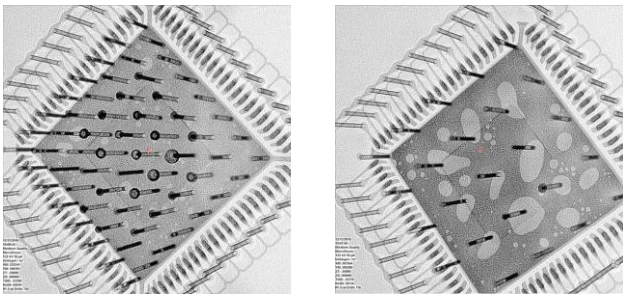


Figure 18: Main effects of solder mask (sm), via array, via size, via pitch, stencil type (dot=0, segmented=1), board thickness and solder paste coverage on the solder paste protrusion height.

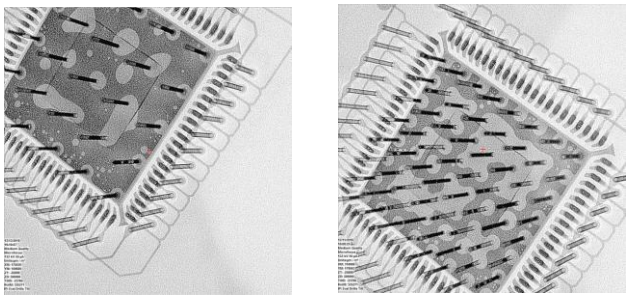
In terms of significance, all the factors considered for the main effects interactions are calculated to be significant (except for solder mask), including some of the second order interactions.
The average protrusion height decreases with decreased via size. Void% and protrusion height responses change in the same direction with number of vias, via pitch, board thickness and solder paste coverage. They differ for solder mask, via size and stencil type.
However, when plotted against each other, there is no correlation found between the void % and the height of the solder protrusions.

Additional X-ray inspection was done for one board only (board #6, 110 mils, assembled with the segmented aperture stencil). Selected images are included in the Figures 19 through 24 below to illustrate the presence of solder protrusions for different size vias, and the wicking of solder inside the vias.



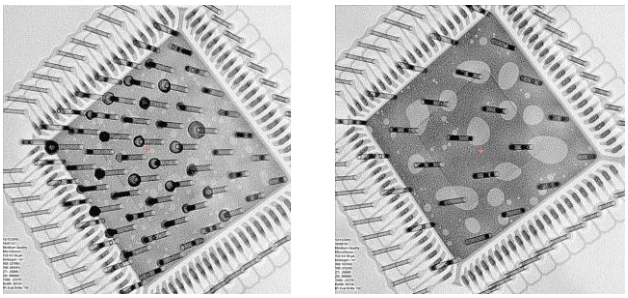
PCA#6, ref des G5, 14% void PCA#6, ref des A2, 24% void

Figure 19: segmented stencil, via diameter Φ1 = 0.2 mm.



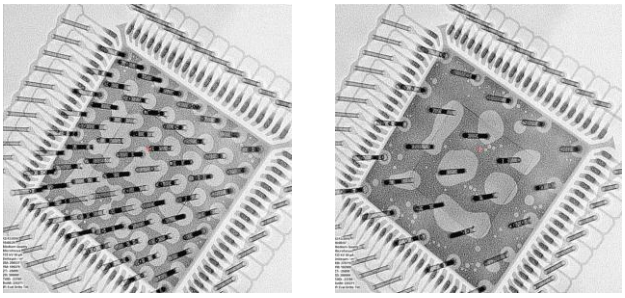
PCA#6, ref des G8, 21% void PCA#6, ref des A3, 45% void

Figure 20: segmented stencil, via diameter Φ1 = 0.2 mm, solder mask doughnut around via.



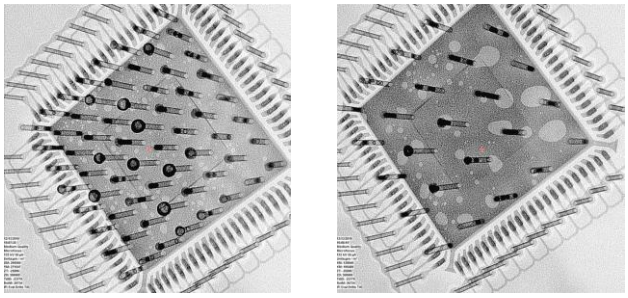
PCA#6, ref des C1, 9.4% void PCA#6, ref des J2, 26% void

Figure 21: segmented stencil, via diameter Φ2 = 0.23 mm.



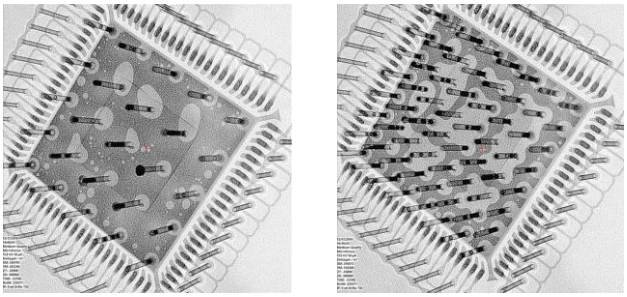
PCA#6, ref des C3, 23.8% void PCA#6, ref des C4, 30.4% void

Figure 22: segmented stencil, via diameter Φ2 = 0.23 mm, solder mask doughnut around via.



PCA#6, ref des E1, 11.4% void PCA#6, ref des L2, 20.7% void

Figure 23: segmented stencil, via diameter Φ3 = 0.25 mm.



PCA#6, ref des E4, 16.9% void PCA#6, ref des E7, 50.4% void

Figure 24: segmented stencil, via diameter Φ3 = 0.25 mm, solder mask doughnut around via.

There are a significant number of cases with no visible solder trapped in vias, like most of the reference designators 3,4,7 and 8 (locations with solder mask doughnut) on the boards assembled with dot apertures stencil. An example is shown in Figure 25. Alcatel/Alcatel-Lucent/Nokia has been using the solder mask doughnuts extensively in volume for more than 15 years and protrusion problems have essentially been non-existent (many millions of PCBA).

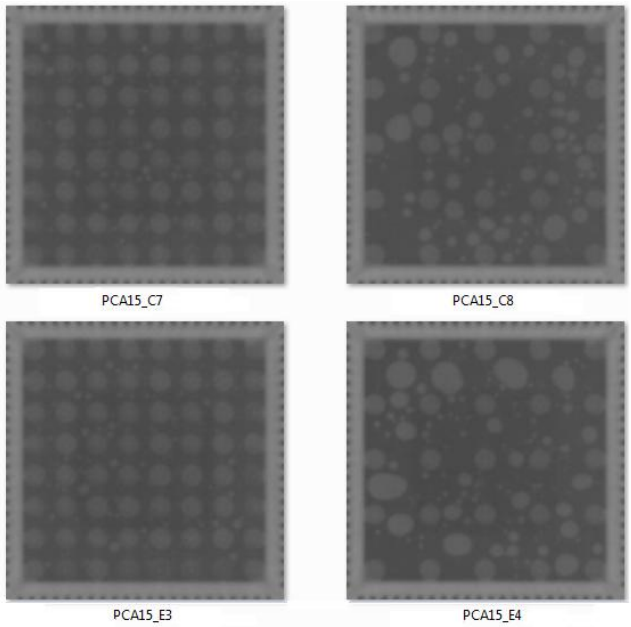


Figure 25: dot stencil, solder mask doughnut around via, via diameter Φ2 = 0.23 mm (above) and Φ3 = 0.25 mm (below); no apparent solder trapped in vias.

A cross-section verification of the PHT via diameter for the smallest via and the highest thickness board was done, and the data is included below in Figure 26 and Table 6.

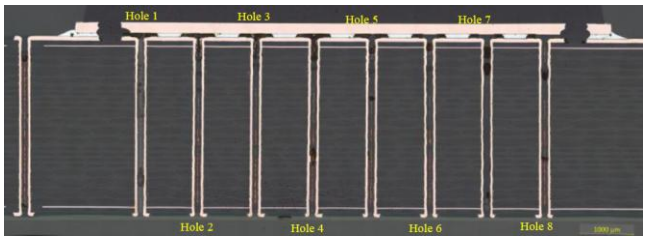


Figure 26: Cross-section at reference designator A7 (Φ1 = 0.2 mm ~0.00787"), PCA#18 (130 mils thickness).

Table 6: PCA#18, A7 via diameter measured at 3 locations along the via.

Via Diameter (mils)							
Via#	Measurement					Expected value	Average
	1	2	3	Nominal	Tolerance		
D1	8.28	7.93	8.31	8.0	±3.0	7.87	8.17
D2	8.21	8.06	8.46				8.24
D3	8.79	7.98	8.37				8.38
D4	8.60	8.38	8.49				8.49
D5	8.79	8.27	8.56				8.54
D6	8.47	8.22	8.40				8.37
D7	8.89	8.56	8.68				8.71
D8	8.68	8.32	8.54				8.51

CONCLUSIONS

A test board was designed to test an isolated set of conditions for void reduction on the thermal pad of QFN. The hypothesis that a small enough via diameter would prevent molten solder from wicking in the via while allowing volatiles to escape and facilitate void reduction was limited to three finished TH via diameters: 0.00787", 0.009" and 0.0098". Only a narrow set of parameters displayed a reduced void%, and limited the wicking of solder inside the via.

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