LOW MELTING TEMPERATURE INTERCONNECT THERMAL CYCLING PERFORMANCE ENHANCEMENT USING ELEMENTAL TUNING AND EDGEBOND ADHESIVE

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ABSTRACT
The adaptation of low melting temperature for solder interconnection comes with significant benefits to less warpage and component defect risk due to the lower assembly temperature. But one disadvantage is inferior thermal cycling performance due to the higher creep rate. Adding to the recent active efforts to improve the thermal cycling performance with maintaining the melting temperature, the degradation mechanism in low melting temperature solder alloys is critical to understand. Since the mitigation of the degradation mechanism will provide the key mechanism improving the thermal cycling performance. In this study, 12x12 mm chip array BGA (CTBGA) components on 62mil thick boards were thermal cycled from -40ºC to 125ºC with Sn based low melting temperature solder with control elements including In and Bi. The microstructure evolution during thermal cycling were observed and the correlation between crack propagation and localized recrystallization were compared in a series of cross section analyses via polarized imaging and Electron–backscattered diffraction (EBSD) imaging. It was found that the elemental impact, of In and of Bi, enhance thermal cycling due to creep rate changes compared to conventional Sn based alloys. To further enhance the performance, an edgebond adhesive was applied and investigated, to determine if it can increase the thermal cycle performance. An improvement of over 140% with dot-cornerbond and 280% with full-edgebond was observed.

Key words: Edgebond, adhesive, Low melting temperature solder, thermal cycling, recrystallization, board level reliability.

INTRODUCTION
In The past 10 years or more, the trend towards electronic devices having multi-functionality has been accelerated. The general package configuration with one Si chip and one substrate per package, dramatically expanded to multi-chip configurations vertically and horizontally. [1] Also multiple Si-dies often placed side by side parallel to dissimilar material layers like Fan-out packages. [2] With the need to keep device manufacturing cost reasonable, while maintaining high reliability, several new challenges became apparent in recent years. The multi-material set per package shows different behavior during thermo-mechanical cycling, during mechanical shock and during multiple surface mount processes. [3] Solder interconnection, used to stabilize the package to board interface, and to carry more signal and power, pose potential risk to the package reliability, stressing the redistribution layer (RDL) in Fan-out WLCSP and building up localized stress points in multi-chip packages. [4] Also, the various materials of a multi-material package have different expansion rates during reflow and thermal cycling, challenging solder joint reliability because of localized package warpage. [3] To mitigate any risk during reflow, design rules in multi-chip packages are getting tighter and it is desired to have a lower reflow temperature with lower level of warpage. [5] One of the solution with Low melting temperature solder alloys were

looked into many variation and alloy design parameters, during the ROHS Lead free conversion. [5,6] Several Sn based alloy systems were developed and well-studied, including Bi-containing alloys. Some low temperature and medium temperature alloys are listed in Table 1 with their melting temperatures. [6] But, when the melting temperature is too low, and too close to the function temperature, the alloy will have stability issues due to a high creep rate. [7]

Table 1. Selected low and medium melting temperature solder alloy compositions and liquidus/solidus temperature. [6]

		Solder Alloy	Liquidus Temperature (°C)	Solidus Temperature (°C)
1		In-32.5Bi-16.5Sn	60	60
2		In--33.7Bi	72	72
3		Bi-26In-16Sn	79	79
4		Bi-33In	109	109
5		In-50Sn	125	118
6	Low Temperature solder	Sn-48In	131	118
7		Bi-42Sn	138	138
8		In-3Ag	143	143
9		Sn-42In	145	118
10		In-5Bi	150	125
11		In-10Sn	151	143
12		Sn-40Bi	170	138
13		Sn-37Pb	183	183
14		Sn-5.5Zn-4.5In-3.5Bi	186	174
15		Sn-20In-2.8Ag	187	175
16		Sn-8.8In-7.6Zn	187	181
17		Sn-9Zn	199	199
18		Sn-10In-3.1Ag	205	204
19		Sn-4.8Bi-3.4Ag	213	211
20	Medium Temperature solder	Sn-10Au	217	217
21		Pb-48Sn	218	183
22		Sn-3.8Ag-0.7Cu	220	217
23		Sn-3.9Ag-0.6Cu	220	217
24		Sn-3Ag-0.5Cu	220	217
25		Sn-3.5Ag	221	221
26		Sn-2.5Ag-0.8Cu-0.5Sb	225	217
27		Sn-4Ag-0.5Cu	225	217
28		Sn-2.5Ag	226	221
29		Sn-1Ag-0.5Cu	227	215
30		Sn-0.7Cu	227	227

In this study, given the fact that most Sn based solder alloy components with 212-217°C melting temperature are board-assembled at around 240-260°C, a target Sn based alloy with 20-30°C lower assembly temperature was considered. The selected Sn based alloy is a Sn-Ag-In-Bi alloy with 197°C melting temperature, which yields good thermal cycling performance. To further enhance thermal cycling performance, a high Tg, low CTE edgebond adhesive was investigated. A corner-dot configuration, which minimized the amount of adhesive used and simplifies the dispense process, and a full edgebond configuration were compared.. The microstructure evolution during thermal cycling was analyzed using polarized optical microscopy and EBSD to identify the degradation mechanism.

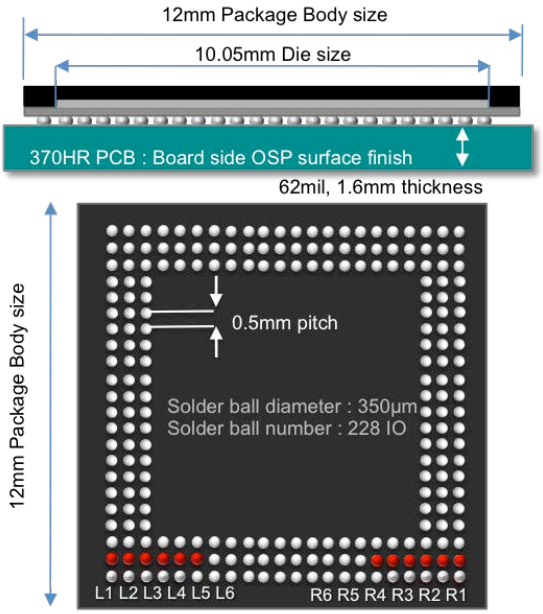

Figure 1. Sample component schematic configuration and board set-up

EXPERIMENTAL PROCEDURE

As shown in Figure 1, the samples used in this study were 12x12 mm body size ball grid arrays (BGAs) with a three-row perimeter array and a total of 228 solder joints. The solder ball diameter was 300µm, and they were arranged in the package with a 0.5 mm pitch. [8] The composition of the solder balls used in this study was Sn-Ag-In-Bi and Sn-3.0Ag-0.5Cu (wt%) (SAC305), Sn-4.0Ag-0.5Cu (wt%) (SAC405) and Sn-1.2Ag-0.5Cu-0.05Ni (wt%) (SAC1205N) for comparison. All BGA samples had a 10.05x10.05 mm silicon die attached, and the package side substrates had electrolytic Ni/Au surface finish on top of the Cu substrate. The packages were assembled onto a 1.65 mm (62mil) high Tg FR4 boards for thermal cycling, which had an organic surface preservative (OSP) surface finish. For thermal cycling, samples were tested with a -40 to 125°C thermal cycle, a ramp rate of 10°C per minute and 10 minutes of dwell time. A continuous resistivity measurement was applied for in-situ monitoring during the test. The failure criterion in this study was a 5-time continuous 20% increase of the peak resistivity compared to the initial value. Twelve data points per condition were collected and plotted using Weibull statistics. For the edgebond-applied samples, a commercially available reworkable edgebond adhesive was

selected, which has a T_g of 134°C and a CTE of 30 ppm/°C. To prevent voiding due to moisture releasing from PCB material during the curing cycle, test boards are pre-baked for 4 hours at 125°C. The edgebond adhesives were dispensed at room temperature using a pneumatic, hand-held dispenser. The board was then cured at 150°C for 30 minutes. [9] Compared to the no-edgebond applied components in Figure 2(a), the dot-cornerbond samples have adhesive at the corners, with 2.0mm of adhesive extending from each corner as shown in Figure 2(b). The full-edgebond components, have adhesive along three full edges and a small opening at the center of the fourth edge, as shown in Figure 2(c).

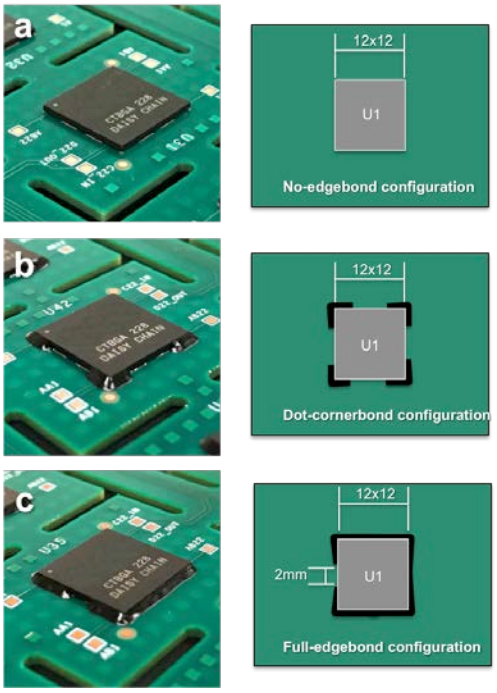

Figure 2. Edgebond sample component picture and schematic configuration

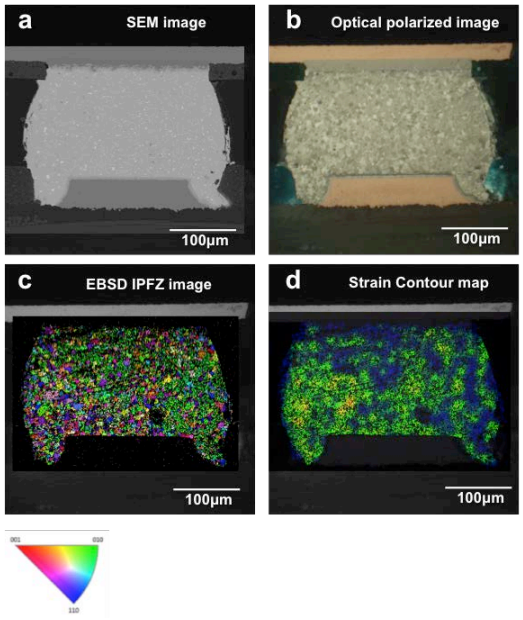

Figure 3. As-assembled Sn-Ag-In-Bi solder joint (a) SEM, (b) Optical polarized image, (c) EBSD IPFX image and (d) strain contour map.

RESULTS AND DISCUSSION

Figure 3 shows the as-assembled Sn-Ag-In-Bi solder joint cross section. The SEM microstructure in Figure 3(a) show well distributed Bi-rich phases inside the Sn matrix with small grain configuration, which can be observed in the optical polarized image in Figure 3(b) and EBSD IPFX image in Figure 3(c). Since the as-assembled joint did not undergo thermal cycling, the strain contour map did not reveal any specific localized strain region compared to strain region after thermal cycling. Figure 4 shows the thermal cycling result of the Sn-Ag-In-Bi alloy compared to conventional SAC alloys (SAC1205N, SAC305 ad SAC405) thermal cycled at the same condition with the same board configuration. As known, the higher Ag contained SAC alloy joints show higher thermal cycling performance compare to lower Ag contained alloys. The Sn-Ag-In-Bi alloy show a slightly higher thermal cycling performance than SAC1205N with a relatively wide spread of the failure cycle numbers and a lower characteristic life cycle number with 1696 cycles. The characteristic life cycle number for SAC1205N, SAC305 and SAC405 was 1634, 1853 and 1881 cycles respectively. In hopes of improving thermal cycling performance, reworkable edgebond adhesive was applied to the Sn-Ag-In-Bi solder samples and Figure 5 is the thermal cycling results with and without edgebond material applied. With edgebond adhesive, the characteristic lifecycle number increased to 2249 cycles when using the dot-cornerbond configuration, and, further, to 4752 cycles with the full-edgebond configuration, an improvement of over 140% and 280% respectively.

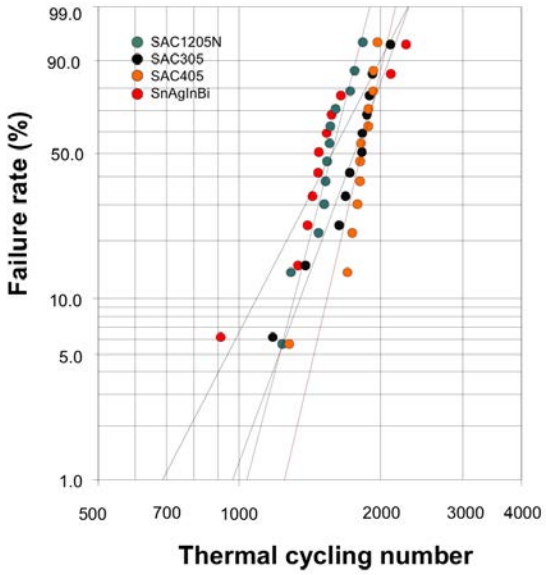

Figure 4. Thermal cycling result Weibull distribution for SAC1205N, SAC305, SAC405 compared to Sn-Ag-In-Bi solder component.

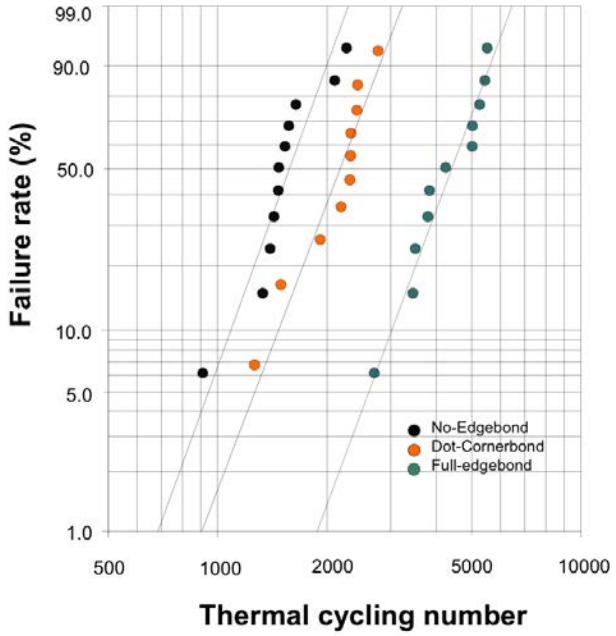

Figure 5. Thermal cycling result Weibull distribution. With and without edgebond applied Sn-Ag-In-Bi solder components.

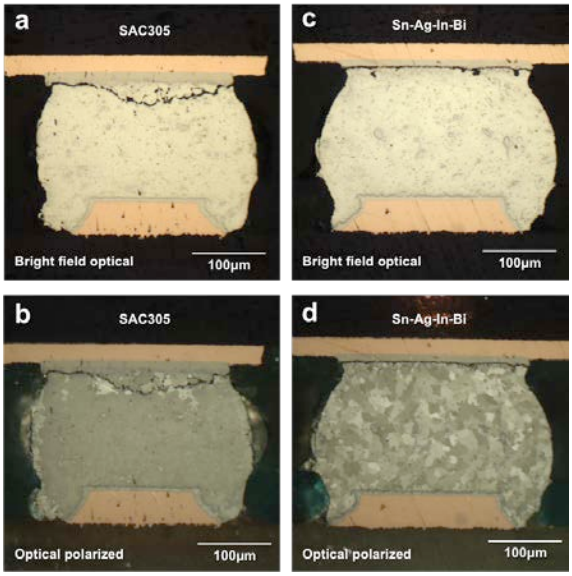

Figure 6. Optical microstructure (a)(b) SAC305 solder joint after thermal cycling (c)(d) to Sn-Ag-In-Bi solder component after thermal cycling

Figure 6 are the cross section microstructure for SAC305 and Sn-Ag-In-Bi alloy components after thermal cycling to failure. Each cross-sectioned solder joint location is indicated in Figure 1. The SAC305 solder joint is from the second row L5 and the Sn-Ag-In-Bi solder joint is from the second row L4. The thermal cycled SAC305 joint in Figure 6(a and b) shows a general crack initiation and propagation near the package side interface with crack propagation into the solder bulk region. The associated polarized image reveals the grain recrystallization along the crack propagation path with the main solder bulk maintained as a single grain structure. Compared to the SAC305 solder joint, the Sn-Ag-In-Bi solder joint in Figure 6(c and d) show crack propagation very close to the interface between the intermetallic compound (IMC) and the solder bulk region at the package side interface. Unlike the single grain structure in SAC305 the Sn-Ag-In-Bi structure show a retained fine-grained structure with slightly enlarged grain size compared to the as-assembled state microstructure in Figure 3 (b and c). Comparing the no-edgebond Sn-Ag-In-Bi solder joints component with the dot-cornerbond components after thermal cycling, it is clear that the fully fractured solder joints are located more at the middle section of the second row solder joints, which are the solder joints under the die shadow area. The no-edgebond samples show crack propagation at from L2 or R2 joint, but dot-edgebond showed crack propagation after reaching L5 or R5.

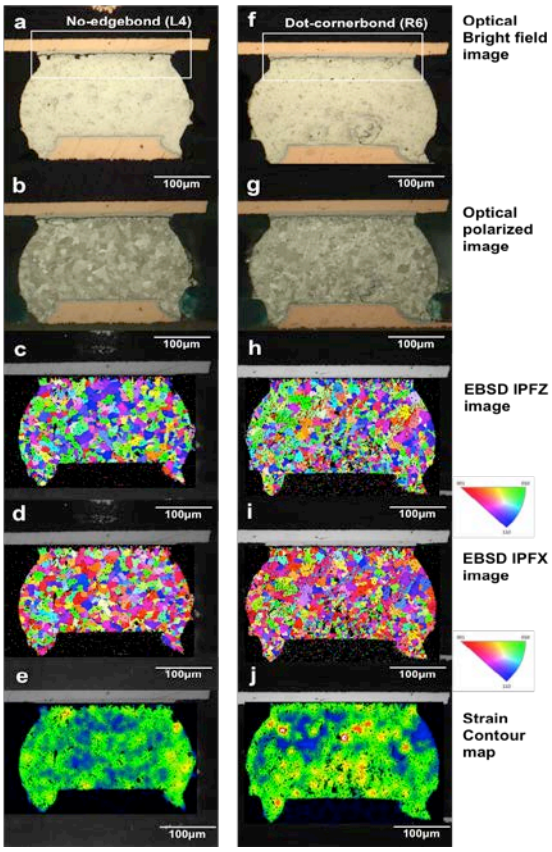

Figure 7. Optical and EBSD microstructure (a)-(e) No-edgebond Sn-Ag-In-Bi solder joint component, (f)-(j) dot-cornerbond component

Figure 7 shows the comparison between the no-edgebond failed joint and the dot-cornerbond failed joint. The Full edgebond sample show a failure phenomenon similar to the dot-conerbond sample ,but after more thermal cycles. Both joints maintained the fine grain structure and have the crack propagation near to the interface not much penetrating into the solder bulk region. The strain contour map based on the EBSD images also show an increase of strain region compared to the as-assembled state solder joint in Figure 3(d). It seems that the stable grain structure from the as-assembled state did not produced any further grain rotation or recrystallization and only pushed the crack propagation path nearer to the interface and prevented crack propagation into the solder bulk material. A higher magnification optical image is shown in Figure 8, which are the areas indicated in a white box in Figure 7(a) and Figure 7(f). As shown in Figure 8, the crack propagation path in the dot-cornerbond sample show a tighter crack opening and with a crack propagation path not only horizontal along the interface but also vertical normal to the interface. This vertical crack path was also observed in WLCSP edgebond samples and conformal coated samples where a compression and tension mode is active which drove the crack propagation to a vertical direction. [9] The associated strain contour map in Figure 7(j) also indicates an overall straining during thermal cycling in the middle of the solder joint, which is another indication of a compression and tension stress and strain inside the solder joint.

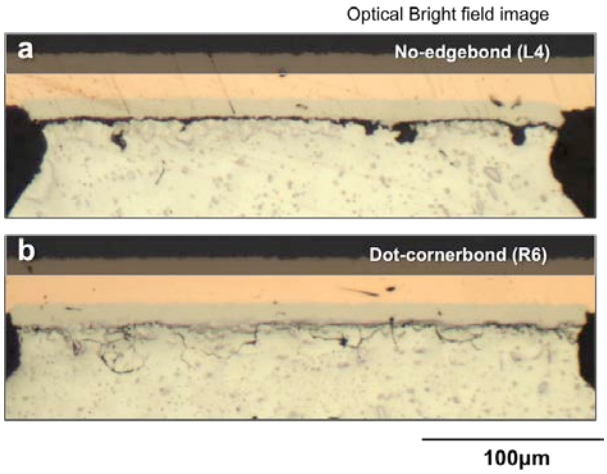

Figure 8. Optical microstructure (a) No-edgebond Sn-Ag-In-Bi solder joint package side interface located at L4 component, (b) dot-cornerbond component package side interface in solder joint R6.

CONCLUSION

12x12 mm chip array BGA (CTBGA) components on 62mil think boards were thermal cycled from -40ºC to 125ºC with Sn based low melting temperature solder with control elements, including In and Bi. The microstructure evolution during thermal cycling were observed and the correlation between crack propagation and localized recrystallization were compared in a series of cross section analyses using polarized imaging and Electron-backscattered diffraction (EBSD) imaging. The Sn based In and Bi containeingd solders show a reasonable thermal cycling performance with a capability to lower the assembly reflow temperature for lower level of warpage during assembly. It was found that the inclusion of In or Bi enhances thermal cycling due to creep rate changes compared to conventional Sn based alloys. To further enhance the performance, a reworkable edgebond adhesive was applied and investigated, to determine if it can increase the thermal cycle performance. Improvements of over 140% with dot-cornerbond configuration and 280% with full-edgebond configuration were observed. The edgebond adhesive can be used to enhance the board level reliability of boards assembled with low temperature solder. The microstructure of Sn-Ag-In-Bi shows a fine-grained structure with lower level of grain rotation and recrystallization behavior, which can be the reason for relatively stable microstructure during thermal cycling.

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REFERENCES

1. Yan Li and D. Goyal (eds), “3D Microelectronic Packaging”, Springer, Chapter 1, pp. 1-15 (2017)
2. J. H. Lau *et al.*, "Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol 7(10), pp. 1729-1738 (2017)
3. Tae-Kyu Lee, Thomas Bieler, Choong-un Kim and Hongtao Ma, “Fundamental of solder and interconnect technology”, Springer, Chapter 5, 132-133 (2014)
4. H. Liu *et al.*, "Warpage characterization of panel Fan-out (P-FO) package," 2014 IEEE 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, pp.1750-1754 (2014)
5. S.Cheng, C.Huang and M.Pecht, “A review of lead-free solders for electronics applications”, Microelectronics Reliability, vol 75, pp.77-95 (2017)
6. Tae-Kyu Lee, Thomas Bieler, Choong-un Kim and Hongtao Ma, “Fundamental of solder and interconnect technology”, Springer, Chapter 2, p.30 (2014)
7. I. E. Anderson, J. C. Foley, B.A. Cook, J. Harringa, R.L. Terpstra, and O. Unal, “Alloying Effects in Near-Eutectic Sn-Ag-Cu Solder Alloys for Improved Microstructural Stability, Journal of Electronics Materials, vol 30(9), pp.1050-1059 (2001)
8. Tae-Kyu Lee, Thomas Bieler, and Choong-un Kim, “Impact of cooling rate-induced recrystallization on high G mechanical shock and thermal cycling in Sn-Ag-Cu solder interconnects”, Journal of Electronics Materials, vol 45(1), pp.172-181 (2016)
9. M. Sheikh *et al.*, "Multi-Axis Loading Impact on Thermo-Mechanical Stress-Induced Damage on WLCSP and Components With Via-in Pad Plated Over (VIPPO) Board Design Configuration," 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, pp. 911-915 (2018)