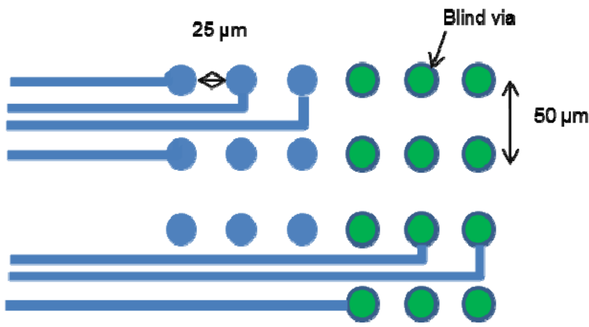

Figure 10. 2-Metal Layer Escape Routing Strategy

ELECTRICAL CHARACTERIZATION

Electrical design and characterization of TPVs and transmission lines were performed, as shown in Figure 11 to obtain S-parameter measurements. Four-metal layer test vehicles were designed and fabricated to form silicon interposers with coplanar wave guide (CPW) lines. The resistivity and thickness of the silicon used was 0.5 Ω-cm and 200µm, respectively, with a polymer-liner thickness of 40µm. The fabricated-CPW lines were 120µm wide. The gap between the signal and ground was 36.5µm. Frequency-domain simulations were carried out for TPVs using full wave EM solvers. The VNA measurement was performed with SOLT calibrations. Low signal loss is a key important parameter for longer RDL lines (4-8mm) that are routed between two dies in the 2.5D interposer. The 7mm signal lines fabricated were characterized to have less than -0.03dB of insertion loss, up to 10Ghz. This lower insertion loss is attributed to the thick polymer liner of very high resistivity. Thus, CPW lines in wafer or panel-silicon interposers are capable of handling high-speed digital signals with nominal distortion.

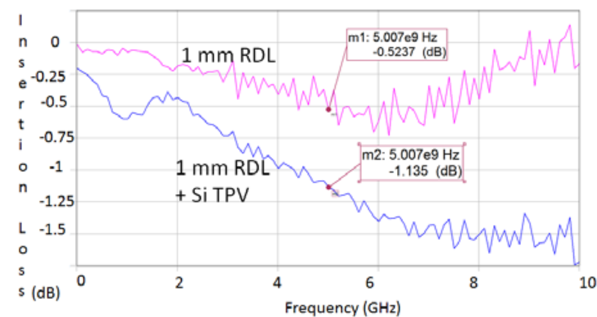

Figure 11. Insertion Loss of RDL Lines in GT's Silicon Interposers

SUMMARY

As organic packages reach their limits in I/Os, thermal and reliability performances, silicon interposers are being developed using BEOL processes in the wafer fabs. But such interposers have two main problems: high cost and low performance. The Georgia Tech approach addresses both these problems as described in this paper.

REFERENCES

[1] Dominique Sarti, Roland Einhaus, "Silicon feedstock for the multi-crystalline photovoltaic industry," *Solar Energy Materials and Solar Cells*, Vol. 72 Nos. 1–4, April 2002, pp.27-40

[2] Masahiro Sunohara, T. Tokunaga, T. Kurihara, M. Higashi, "Silicon Interposer with TSVs (Through Silicon Vias) and Fine Multilayer Wiring," *Proceedings Electronic Components and Technology Conference, 58th*, ECTC 2008, pp. 847-852

[3] K. Zoschke, J. Wolf, C. Lopper, I. Kuna, N. Jurgensen, V. Glaw, K. Samulewicz, J. Roder, M. Wilke, O. Wunsch, M. Klein, M.V. Suchodoletz, H. Oppermann, T. Braun, R. Wieland, O. Ehrmann, "TSV based Silicon Interposer Technology for Wafer Level Fabrication of 3D SiP Modules," *Proceedings Electronic Components and Technology Conference, 61st*, ECTC 2011, pp. 836-843

[4] Kirk Saban, "Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency," *WP380*, Vol. 1 No. 12, October 2011

[5] Katsura Hayashi, Kimihiro Yamanaka, Masahiro Fukui et al., "Advanced Surface Laminar Circuits Using Newly Developed Resins," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, Vol. 1 No. 12, 2011, pp. 1908-1915