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Lead Free Process Development with Thick Multilayer PCBA Density in Server Applications

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Abstract
Although the EU RoHS legislation restricts the use of lead in electronics equipment, many high-end multi layer server printed circuit board assemblies (PCBAs) continue to be built with lead under the server equipment exemption. As the industry prepares to comply with the RoHS directive without the use of exemptions, several studies and research efforts continue to focus on expanding the lead free assembly process capabilities for these types of high density, thick PCBAs. In this space, a different approach is required to mitigate the often encountered technical challenges of a lead free process such as solder hole fill on PTH barrels, copper dissolution effects and reflow thermal profiling.

The additional thermal mass on thick heavy assemblies' further narrows the process windows to achieve the temperature profiles required. On these assemblies the printed circuit board thickness can often extend to over 0.130 inches with layer counts in excess of often 18 or more, comprising of 1 ounce and 2 ounce copper planes. These circuit board stack ups introduce an increased level of PTH solder hole fill difficulty which cannot be addressed by normal process optimization techniques. Furthermore during SMT reflow, the additional thermal mass from the PCB and number of large BGA devices generally increase the overall heat required in producing an optimized reflow profile condition to meet the solder joint attributes, while at the same time be constrained by the thermally sensitive components. These challenges requires new approaches to achieve optimization which will need to be considered at the conceptual stage of board lay out and component selection.

This paper examines the effects of varying surface finishes, temperature sensitive component limitations, process parameters and the resulting interactions that affect the solder attach attributes. The study includes characterization of solder joint attributes from a time zero perspective and extends to accelerated temperature cycling with post stress characterization. Additionally, the intent of this work is to document the need to identify design and process options for applications where density and PCBA functions extends beyond the commercially developed lead free solutions.

Introduction

Industry & EU regulators to date have not established a firm implementation date for elimination of lead (Pb) in solders of server products. Many of these products which contain complex PCBAs that are dense, thick and with number of heavy copper planes, are amongst the most challenging products to convert to a Pb-free assembly process.

In this work, a current OEM product in production and a new product in development are utilized as test vehicles to evaluate the assembly characteristics from different PCB surface finishes and identify the process parameters which optimize the yields for the Pb-free assembly process. The study follows the defined experiment through the primary soldering processes of Surface Mount Technology (SMT) and wave soldering. Solder joint attributes on selected samples are further characterized at time zero and post thermal stress conditioning.

Case Study 1: Pb-free process feasibility on a current OEM product

An OEM product currently in mass production with eutectic tin-lead (SnPb) soldering process was chosen for the initial Pb-free process feasibility study. The main objective of the study was to identify any critical gaps in the current assembly process and product design, as well as to identify areas which need additional investigation through follow-up studies.

Test Vehicle Description

The test vehicle used in this study was a double sided SMT and single side wave assembly which is shown in Figure 1. The assembly process and the raw materials which were based on SnPb metallurgy was converted to Pb-free for the experiment. The printed circuit board was 405 mm x 405 mm x 3 mm, consisting of 8 power and ground plane layers and 10 signal layers. The plane layers included 2 layers with 2 oz. copper while the remaining 6 layers were 1 oz. copper. Table 1 lists some of the Ball Grid Array (BGA) and Plated through Hole (PTH) component technology that were included on this test vehicle.

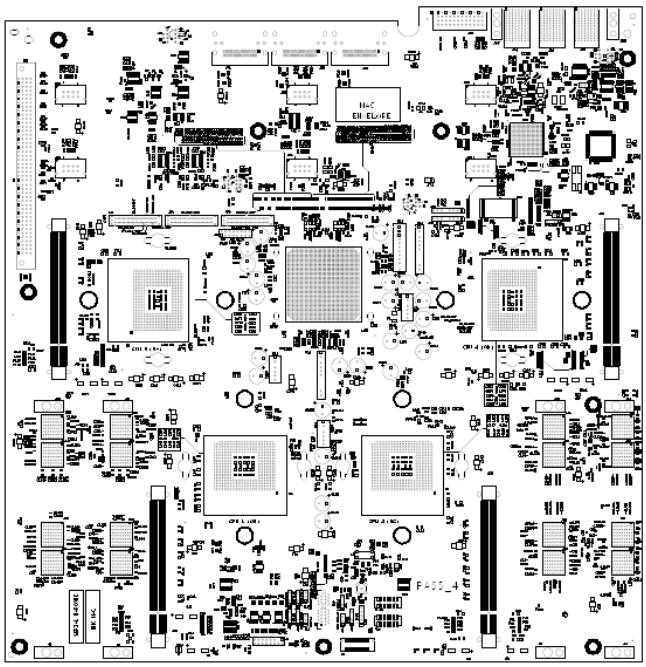


Figure 1 – Top Side View of the Pb-Free Test Vehicle

Table 1 – BGA&PTH Component Technology on the Test Vehicle

Component Type	Description
BGA	PBGA 2092 I/O, 1 mm pitch, SAC305
	PBGA 400 I/O, 1 mm pitch, SAC405
	CPU BGA Socket 603 I/O, 1.27 mm pitch, 96.5Sn3.5Ag
PTH	DC-DC Module, Single In-line Vertical Package
	Electrolytic Aluminum Capacitor
	Headers, Flat Vertical Break Away Style

Assembly Process

The test vehicle was assembled with no clean SAC405 paste in a nitrogen atmosphere using a standard 10 zone reflow oven at SMT. No clean wave soldering flux and SAC405 alloy were used to assemble the boards in a 3-zone, in-line, automatic wave soldering machine. The assembly process flow is shown in Figure 2.

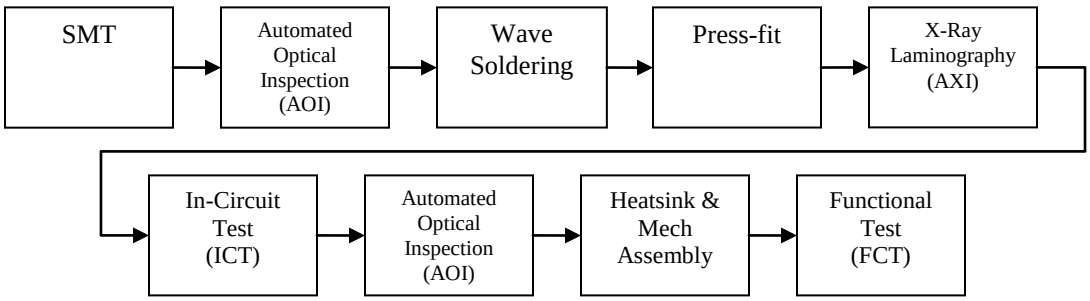


Figure 2 – Test Vehicle Assembly Process Flow

BOM Analysis & Thermal profiling optimization

The bill of materials (BOM) analysis is an essential part of the Pb-free assembly process development. All components listed in the BOM were checked for RoHS compliance status and temperature sensitivity was validated with methods previously followed on other Pb-free and mixed assembly process development studies and industry standards.[1,2] The BOM analysis identified a number of temperature sensitive components which were at risk of exceeding the component vendor's specification and internal IBM specifications. Some of the temperature sensitive parts identified on the BOM included

electrolytic capacitors, oscillators, tantalum capacitors and molded aluminum capacitors. These temperature sensitive parts required detailed monitoring of the component body temperatures during the thermal profile development.

The SMT thermal reflow profile was optimized from the initial Pass 1 state summarized in Table 2 over a number of iterations to a Pass 2 state where the peak temperature of the electrolytic capacitor was reduced. However, the time above liquidus (TAL) recorded for most of the temperature sensitive parts failed to meet the requirements from the Pass 2 profile. To meet these specifications, a thermal shield was required to reduce the heat transfer to the temperature sensitive parts while maintaining the minimum peak temperature requirement on the BGA joints. The resulting profile which was created with the thermal shield is summarized in Table 2 as Pass 3. As observed on the Pass 3 profile, while the majority of the components met all the temperature specifications, the electrolytic capacitors remained beyond the TAL maximum. The team elected to proceed with the experiment at this state, acknowledging the out of the specification condition of the electrolytic capacitor and have since made a recommendation to obsolete the component from the OEM's approved vendor list for future Pb-free product application.

Table 2 - Reflow Profile Iterations to Address Temperature Sensitive Component Constraints

Temperature Sensitive Components	**Component Body Temperature Profiles**							
	Component Limitations		**Measured Peak Temperature (°C) / TAL217 (sec)**					
	Peak Reflow Temperature (°C)	**Time Above Liquidus (TAL), 217°C (sec)**	**Pass 1** Initial Profile		**Pass 2** Optimized Soak Profile		**Pass 3** Optimized with Thermal Shield	
			Peak (°C)	**TAL (sec)**	**Peak (°C)**	**TAL (sec)**	**Peak (°C)**	**TAL (sec)**
Electrolytic Capacitors	< 250	≤ 40	**250**	**92**	248	**86**	246	**65**
Oscillators	< 260	≤ 90	247	**93**	245	**92**	240	67
Tantalum Capacitors	< 260	≤ 90	248	**93**	250	**90**	243	63
Molded Aluminum Capacitor	< 250	≤ 60	**250**	**89**	**-***	**-***	236	50
BGA Components	**Solder Joint Temperature Profiles**							
Coldest solder joint	≥ 230	≥ 35	231	83	231	78	231	54
PCB Laminate	< 245	N/A	244	N/A	244	N/A	238	N/A

* - data not collected during Pass 2 profile run

The Pb-free wave solder profile was also created by following the similar methodology that was used for SMT, which monitored the various temperature sensitive components during the profile. The PTH component body temperature limits did not pose the same challenges as SMT and multiple iterations to develop an acceptable wave profile for temperature sensitive parts were not required. Therefore, the main focus for the wave profile development was placed on optimizing the contact time over wave and establishing the settings to be used in the evaluation matrix.

Evaluation Matrix

The evaluation matrix used in Case Study 1 is shown in Table 3. The main input variables evaluated were the PCB surface finish, PTH barrel plating, and the wave contact time. Selected samples in the matrix were subjected to thermal stress conditioning after assembly to uncover any non-time zero failures. Thermal stress conditioning consisted of 20 cycles Thermal Ship Shock from -40°C to 65°C and 300 cycles of Accelerated Thermal Cycling (ATC) from 0°C to 100°C with 1 cycle per hour. All samples post thermal stress conditioning were functionally retested.

Table 3 – Case Study 1 Evaluation Matrix

Cell	**1a**	**1b**	**2b**	**3a**	**3b**	**4b**	**5a**	**5b**	**6b**
PCB Surface Finish	OSP			Immersion Silver (ImAg)					
PTH Barrel Plating	Yes			Yes			No		
Wave Contact Time	long	long	short	long	long	short	long	long	short
Thermal Stress Conditioning	No	Yes	No	No	Yes	No	No	Yes	No

a) PCB Surface Finish
Two different surface finishes, Organic Surface Preservative (OSP) and Immersion Silver (ImAg) were evaluated as input variables for the experiment. ImAg was selected to evaluate if it would result in an improved PTH barrel fill during wave soldering and whether there were any negative tradeoffs in reliability due to a phenomenon such as micro-voiding or irregular grain structure at the solder joint interface.

b) PTH Barrel Plating
Barrel plating is an assembly process technique whereby a small amount of solder paste is deposited near the PTH annular ring during the SMT assembly process. By coating the PTH barrel with a thin layer of solder, oxide formation on the base metal is prevented and a more wettable PTH barrel is available for wave soldering. This technique has been successfully used on other SnPb assemblies, hence selected as one of the input variables for evaluation.

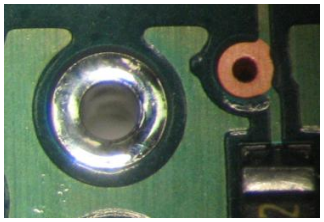


Figure 3 – Example of OSP board plated with SnPb solder

c) Wave Contact Time
The wave profile was developed to evaluate two different contact time settings: high and low. The high limit was derived from internal reliability data and other works which examined the effect of wave soldering contact time from SAC based alloys on the PTH copper dissolution. These studies have shown that excessive contact times while providing increased hole fill for PTH components also increased the copper dissolution effects on the PTH barrel as reflected in pictorials shown in Figure 4.

5 Sec 13 Sec 30 Sec

Figure 4 – Cross Section Images of Copper Dissolution from Contact Times of 5, 13 and 30 seconds [3]

Assembly Process Results and Observations – Time Zero
The test vehicles followed the process flow outlined in Figure 2. No anomalies related to the SMT process were observed during the build and the process yields at the inspection and test steps were comparable to the production cards built with the SnPb assembly process for SMT. However, there were notable differences in the process yields of PTH parts, which were identified during X-ray laminography (AXI) characterization. In general, the PTH barrel fill of the test vehicle was lower than historical performance of these products built on the SnPb process. The effects of the input variables on the PTH hole fill are discussed below.

a) PCB Surface Finish
The surface finish did not have a significant effect on the PTH barrel fill achieved from wave soldering. The PTH barrel fill results of the OSP finish cells 1a, 1b, and 2b from the evaluation matrix were compared with ImAg group 3a, 3b, 4b. Both OSP and ImAg groups had its barrels plated. Although the ImAg group had a slightly higher response for percentage of pins which met the 75% PTH barrel fill requirements, the mean response difference was only 3.36% when a long contact time setting was used and the gap in performance reduced further to 0.64% when the short wave contact time setting was used. The plots as shown in Figure 5 reflect these observations and lack of significance with each line nearly parallel to each other.

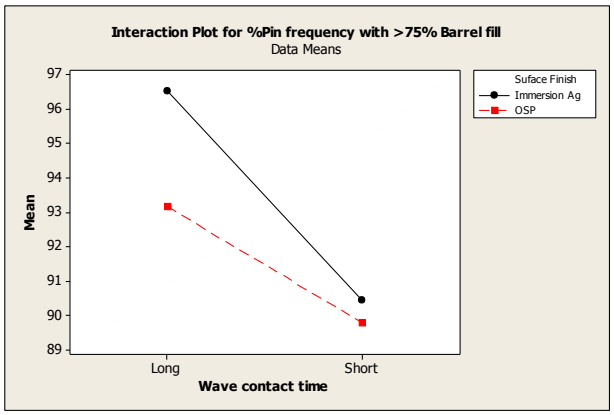


Figure 5 – PTH Barrel Fill Interaction plot between Surface Finish and Contact Time

b) Barrel Plating

The response to barrel plating was analyzed in two parts. First, the effects of barrel plating on ImAg surface finish group (Cells 3a, 3b, 4b vs. 5a, 5b, 6b in Table 3) was reviewed. Its response to the input variable is shown in Figure 6. On samples which were built with short wave contact times, the addition of the barrel plating process increased the percentage of pins which achieved 75% PTH barrel fill from 85.2 to 90.4%. However, the positive effects to PTH barrel fill were negated when the longer wave contact time was used, resulting in virtually identical PTH barrel fill performance on samples with and without barrel plating.

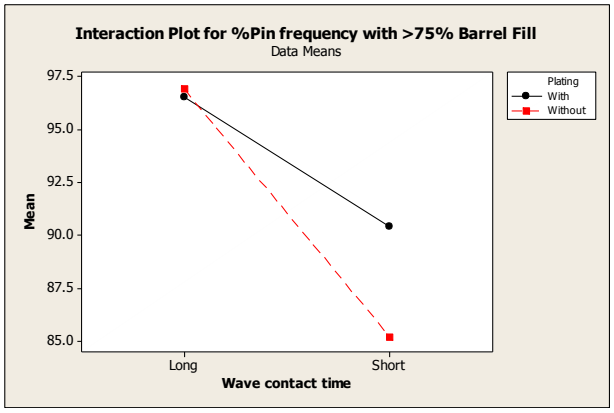


Figure 6 – PTH Barrel Fill Interaction Plot, Barrel Plating and Contact Time on ImAg boards

Second, the relative performance of the OSP surface finish with barrel plating was compared to that of ImAg without barrel plating as shown in Figure 7. In contrast to the commonly reported findings where ImAg surface outperforms OSP for wetting [4,5], barrel plated OSP samples with short wave contact times had better PTH barrel fill than the ImAg samples. However, the trend reversed with longer wave contact times and ImAg samples had a higher frequency of pins with > 75% PTH barrel fill.

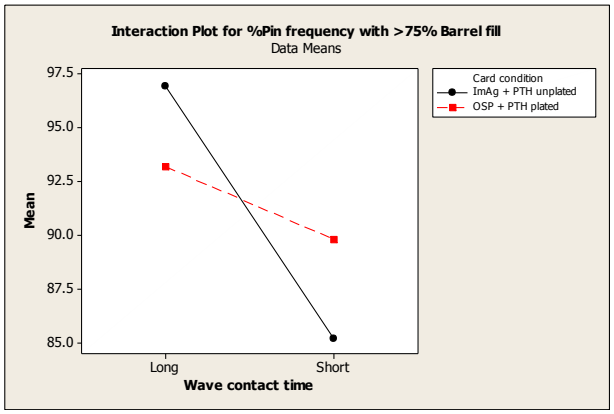
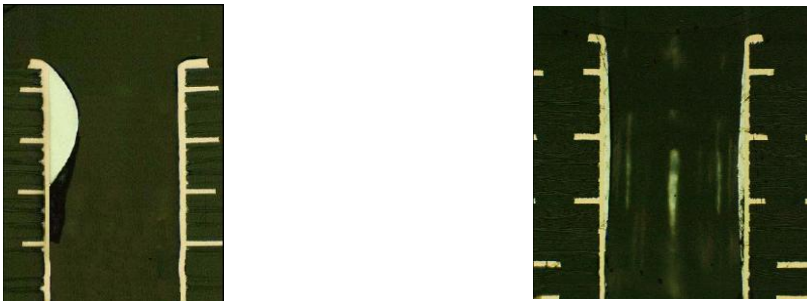


Figure 7 – PTH Barrel Fill Interaction Plot, Barrel Plating and Contact Time on OSP and ImAg Boards

One possible explanation of the inconsistent response to barrel plating is the wetting characteristics of the SAC solder paste. Unlike SnPb solder paste, the Pb-free SAC solder paste does not tend to wet fully and spread along the base metal surface. As a result, solder paste which is applied during the barrel plating process at SMT clumps up near the surface and does not sufficiently flow into the barrel. Thus, the PTH barrel is only partially protected from oxidation and benefit of an improved wettable surface is limited to only a small area of the barrel. Comparing the cross sections of PCBs plated with Pb-free and SnPb solder paste as shown in Figure 8 confirmed the presence of solder clumps near the upper end of the barrel and significant portion of the PTH barrel which remained unplated on the Pb-free samples in contrast to the SnPb samples which were fully plated.



a) Pb-free b) SnPb

Figure 8 – Typical Examples of PTH Barrels Plated with Pb-free and SnPb Solder Paste

c) Wave Contact Time

Of all input variables evaluated in this case study, wave soldering contact time was the most significant variable that affected the PTH barrel fill response. The plots in Figure 9 shows the main effects of hole fill for each input variable. There are small differences in the effects of surface finish and barrel plating, but considerable main effect differences for wave contact time. This is seen in the slope gradient of the plot for wave contact time.

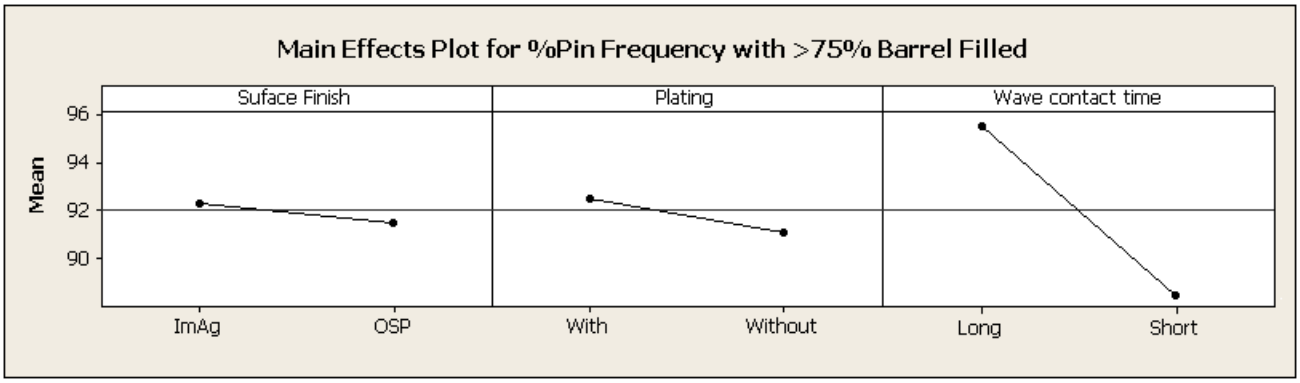
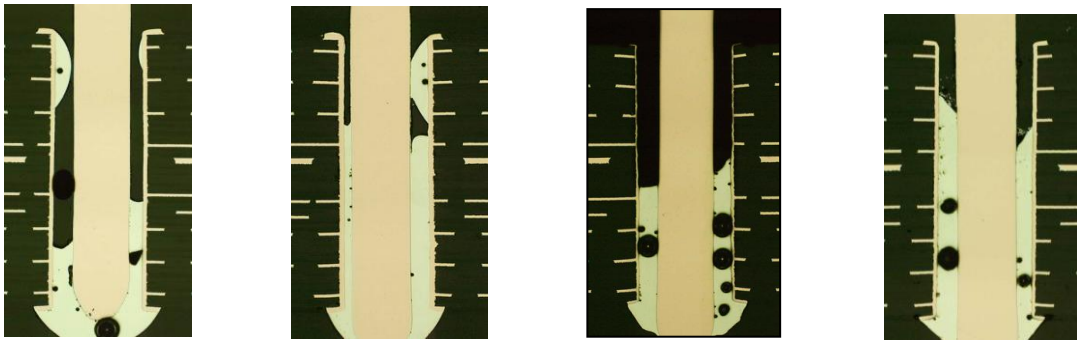


Figure 9 – Main Effects Plot for PTH Barrel Fill

Figure 10 is typical cross section images of the PTH barrel from samples built with short and long wave solder contact times. On both OSP and ImAg samples, higher PTH barrel fill was obtained when longer wave contact time was used. The images of cross sections reveal PTH barrel fill measurement of 31.37%and 64.78% respectively from short and long wave contact times on the OSP finish samples. On the ImAg, PTH barrel fill shown are 48.66% and 68.84% for the short and long contact times. These results confirm that wave soldering contact time is one of the key factors that enable PTH solder joints to meet IPC specifications for thick multilayer PCBA.



OSP, Short OSP, Long ImAg, Short ImAg, Long

Figure 10 – Examples of PTH Cross Section from Short and Long Wave Contact Time

Thermal Stress Conditioning Observations

All samples from the evaluation matrix passed the functional test (FCT) after the initial assembly and post thermal stress conditioning. Sample locations from each assembly were selected for cross sectioning to observe the solder joint and PCB laminate characteristics before and after stress conditioning. The Figure 11 and 12 are some typical examples of cross section images of solder joints at time zero and post thermal stress respectively. There were no notable differences between the cross section images from time zero and thermal stress conditioned samples. No anomalies were observed other than the insufficient barrel fill on some of the PTH locations which had also been detected by AXI during assembly.

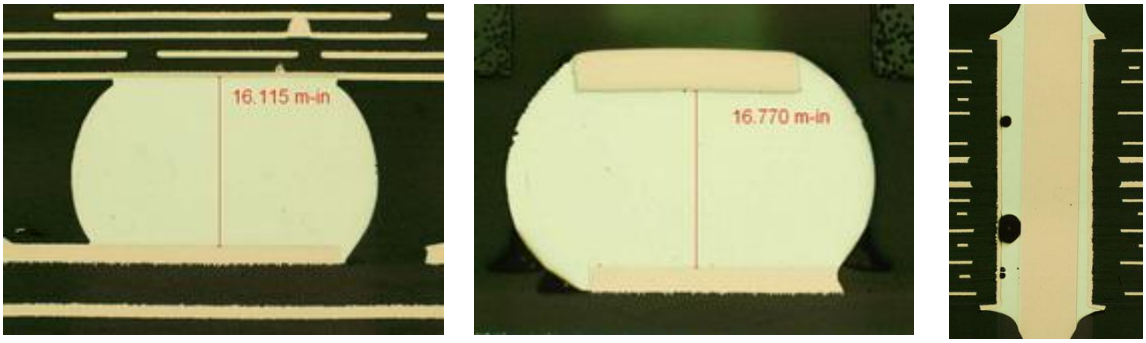


Figure 11 – Cross Section Images of Solder Joints from Time Zero Card

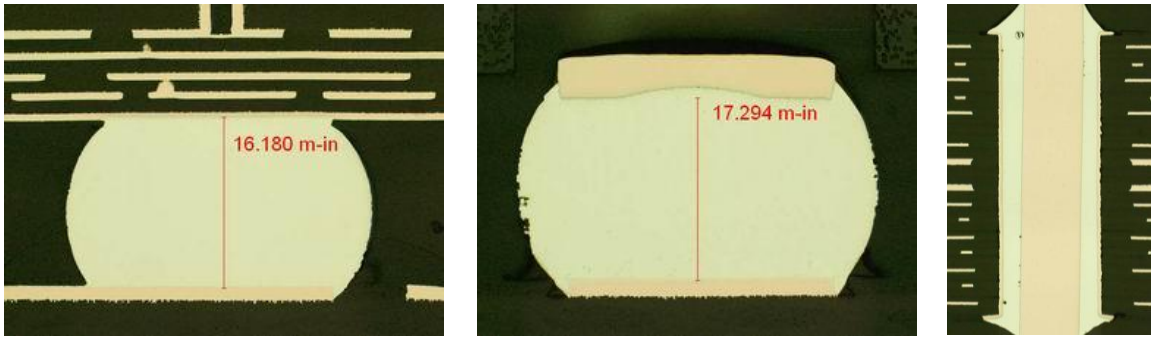


Figure 12 – Cross Section Images of Solder Joints from Post Stress Conditioned Card

Conclusions from Case 1 Study:

From the above case study of an OEM product, several observations were noted which provide insight to the limiting factors of assembling a thick multilayer Pb-free PCBA. Component selection with lower TAL times and peak temperatures affect profile settings for SMT attach. These limitations observed during SMT reflow profile development may extend to rework, creating additional complications and challenges for the manufacturer of these assemblies. Process development for optimum profile condition becomes necessary and a unique solution for each card definition and layout may be required. These activities allows for development of a robust assembly process which is required to achieve the high field reliability expectation of server products.

Achieving the specified PTH hole fill from wave soldering on thick Pb-free assemblies requires additional efforts with emphasis placed on the in depth study of PCB stack up, thermal relief connections, pin to hole aspect ratios and clearance areas around the pin making contact with the wave. The above study shows contact time is a significant process variable that needs to be optimized and characterized during process set up.

Case Study 2: Pb-free process development on a NPI product

The second case study is a continuation of the basic process feasibility efforts from Case Study 1. In this study, a new production introduction (NPI) server product, early in its life cycle was selected to assess the impact from assembly design condition and process variables. The test vehicle chosen was a fully RoHS compliant, Pb-free product. One of the main drivers for selecting this specific product was that the board contained many PTH parts in a similar thick PCBA card density. Based on the finding from Case Study 1, primary focus was placed on analyzing the PTH barrel fill performance during wave soldering.

Test Vehicle Description

The NPI product in case study 2 was 405mm x 284.23mm by 2.45mm thick. The board was constructed of 16 layers of wherein 6 layers were 1 oz. planes and 2 layers were 2 oz. planes. The surface finish of the printed circuit board was OSP. The PCBA was a densely populated doubled sided SMT, single sided PTH assembly. Some of the main component technologies on the board are listed in Table 4 and an illustration of the card layout from the top side is shown in Figure 13.

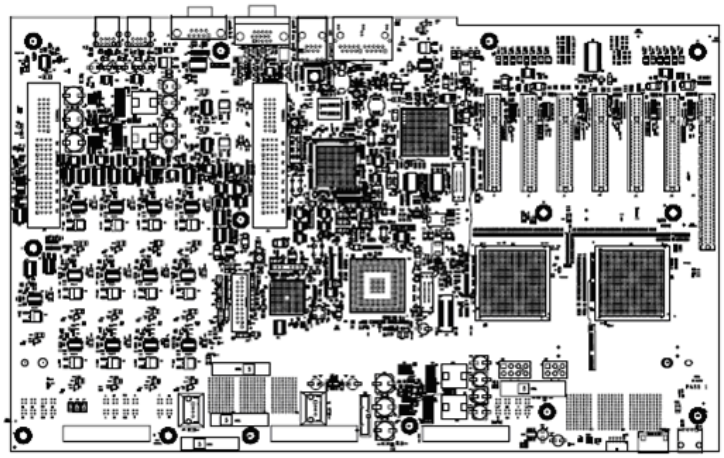


Figure 13 –Top Side View of the Pb-Free Test Vehicle

Table 4 – BGA and PTH Component Technology on the Test Vehicle

Component Type	Description
BGA	PBGA 1295 I/O , 1 mm pitch, SAC405
	PBGA 676 I/O, 1 mm pitch, SAC405
	PBGA 320 I/O, 1 mm pitch, SAC405
	PBGA 484 I/O, 1 mm pitch, SAC305
	PBGA 668 I/O, 1 mm pitch, SAC305
	FBGA 84 I/O, 0.8 mm pitch, SAC305
PTH	Vertical USB Connectors
	Right Angle USB Connectors
	Right Angle Ethernet Jacks
	Battery Holder
	Right Angle D-Shell Connectors
	Vertical Power Connectors
	Header, Flat Vertical Break Away Style

Assembly Process

The test vehicle was assembled with no clean SAC305 pastes in a nitrogen atmosphere using a 12 zone reflow oven for SMT. No clean wave soldering flux and SAC405 alloy were used to assemble the boards in a 3-zone, in-line, automatic wave soldering machine equipped with a nitrogen blanket. The assembly process flow followed is shown in Figure 14.

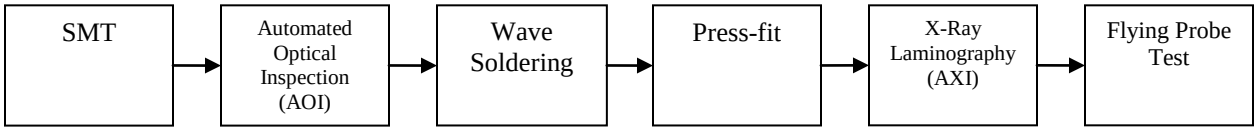


Figure 14 – Test Vehicle Assembly Process Flow

Evaluation of Design and Process Variable

The effects of insufficient thermal relief, insufficient bottom side component clearance, non-ideal pin to hole size ratio and insufficient lead protrusion has previously been studied and the poor PTH barrel fill that results from these Design for PCBA Manufacturing (DFM) violations have been documented.[6] However, in some cases for high end server products, it is not always possible to follow the DFM guidelines mainly due to higher product performance characteristics desired on the final product. The main objective of the experiment was to evaluate the assembly yield on an actual product design and offer alternatives that can be used on future design revisions.

For the manufacturer of PCBAs, there are a finite number of process variables which can be considered to optimize the overall process yields. These may include designing assembly tooling to optimize the selective wave pallet opening, developing a profile to maximize pre-heat and contact time and selecting a wave soldering flux which provides the most optimal wave soldering condition. However for the most part, there are limitations to which these variables can be adjusted. For example, the wave pallet designs are largely constrained by the board design and more specifically the component clearance between the bottom side SMT parts to the PTH barrels. The thermal profiles for wave cannot be optimized to an extent such that it compensates for lack of thermal reliefs in the card design by prematurely burning off the wave soldering flux. Likewise, increasing the contact time to deliver additional heat to the card can have negative effects on copper dissolution of the PTH barrel at the knee. Also, selecting a more aggressive wave soldering flux can increase the risk of electro-migration and dendrite growth if the chemical compatibility is not properly evaluated.

a) DFM considerations

As is the case for many of the very early NPI products in development, there were several DFM issues on the test vehicle design that had not been corrected at the time of the experiment. These DFM issues have been previously known to impact assembly process yields [6]. The Table 5 below lists some of the DFM issues and qualitative classification of the severity of these issues on the board design. The severities of these issues were classified by analyzing the total percentage of pins which had not met Celestica's recommended design guidelines and known industry specifications. Where the majority of the pins in the specific component technology were affected with the DFM violation, the violation was classified as "MAJOR" in Table 5. This breakdown allows for further interpretation of the initial results and provides the necessary data to make design changes early in the product development cycle.

Table 5 – DFM Violations Observed on the Test Vehicle

Component Type	Total # of Leads	Thermal Relief	Bottom Side Component Clearance	Pin to Hole Ratio	Tail Length (Lead Protrusion)
Battery Holder	3	minor	MAJOR	-	MAJOR
Vertical Header	72	minor	minor	MAJOR	MAJOR
RA – D-Shell	28	minor	minor	-	MAJOR
RA – Ethernet Conn	45	minor	minor	-	MAJOR
RA – USB Conn	24	minor	minor	minor	MAJOR
V – Power Conn	14	MAJOR	minor	-	MAJOR
V – USB Conn	12	minor	MAJOR	-	-

b) Wave Soldering Direction

After optimizing most of the process variables such as the wave fixture design and the thermal profile, one additional variable available for the manufacturer is to evaluate the wave soldering direction in which the board is processed. The wave soldering direction is one contributor to the overall PTH barrel fill due to the hydrodynamic behavior of the molten solder and the fixture surface profile which affect the flow behavior of solder during the wave process. As shown in Figure 15, the

wave fixture opening which is limited by the placement of bottom side SMT components, can limit the flow of molten solder in certain directions under the board. Also, the pins positioned close to the edges of the fixture opening may see shadowing effects which will limit overall contact and heat observed by the barrel. To study the net impact, the board design, parts and assembly process tooling were kept as constants for the experiment. Wave soldering direction was chosen as the experiment variable where by two opposing loading directions were evaluated per Figure 15.

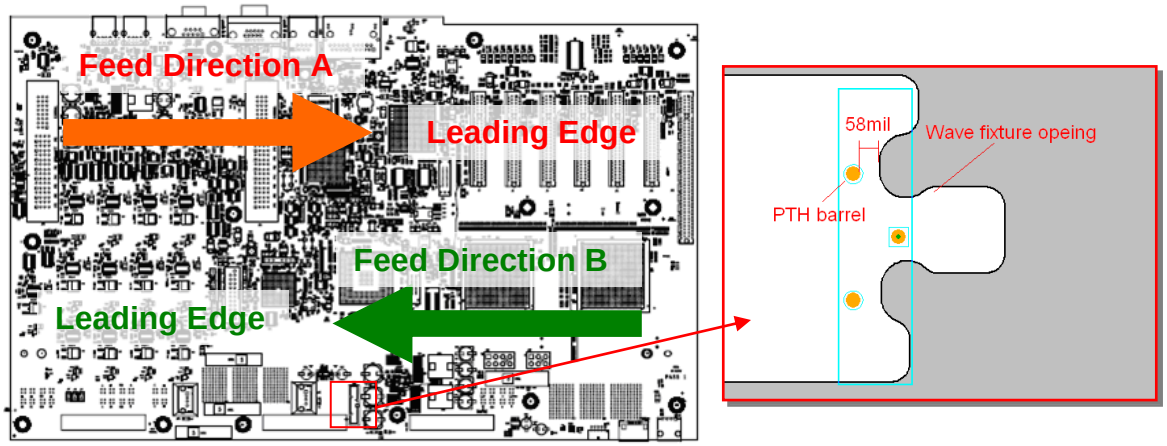


Figure 15 – Wave Direction and Example of Selective Wave Fixture Opening

Results and Observations

PTH barrel fill was evaluated based on IPC 610-D, class 2 [7] requirements using AXI. Figure 16 shows the percentage of pins meeting the PTH barrel fill specification from the two different feed directions for wave soldering.

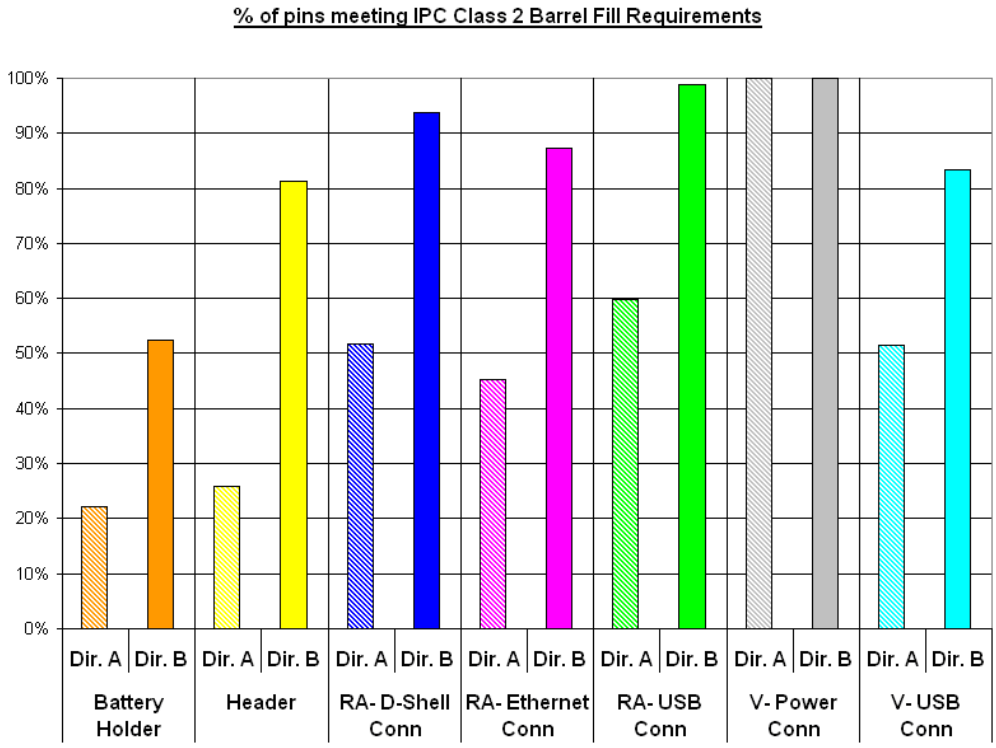


Figure 16 – Comparison of PTH Barrel Fill from Wave Direction A vs. B

a) DFM considerations

In general, a relationship was observed between the DFM violations and the percentage barrel fill; however, it was not possible to quantify the effects of the individual DFM issues due to multiple factors and possible interactions between the different types of violations. For example, the battery holder location on the test vehicle contained several DFM issues including major issues for lead protrusion and insufficient bottom side component clearance near the pins which limited the dimensions of the wave fixture opening. Furthermore, the thermal relieves on inner power and ground planes attached to the pins of the battery holder did not meet the DFM requirements. Analyzing the PTH barrel fill performance by controlling these individual DFM factors would have been ideal; however, the alternate components with the correct tail length were not available and design requirements could not be changed at the time of the experiment to test the effects of individual design factors. However for some of the PTH components where consistently poor barrel fill is observed, it is clear that the process development has reached its limits and further improvements to PTH barrel fill cannot be achieved without changing the design to address the DFM violations.

b) Wave Soldering Direction

As shown in Figure 16, the wave feed direction B provided higher percentage of pins which met the solder fill requirements in almost all cases. Closer examination of thermal profile for direction A and B revealed that the loading direction affected the contact time and the peak temperature of PTH barrel during wave soldering. Table 6 below illustrates these differences for some of the PTH locations on the board. For example, wave direction B created both higher contact times and peak temperatures for the Battery Holder and Right Angle Ethernet Connector, which in turn resulted in higher percentage of pins meeting the PTH barrel fill requirement by 30 and 42% respectively. Similar differences in contact and peak temperatures were also noted on other types of parts.

It was also noted that wave contact time and peak temperatures measured at the PTH barrels with insufficient hole fill were comparatively lower than the other location. Table 6 shows that the vertical power connector which had the best PTH barrel fill had comparatively longer contact times and higher peak temperatures than the other two components. Peak temperature measured at the barrels was one of the key indicators of expected barrel fill.

Table 6 – Difference in Contact Time and Peak Temperature Measured

PTH Connector Type	Direction A		Direction B	
	Wave Contact Time (Sec)	Peak Temp (deg C)	Wave Contact Time (Sec)	Peak Temp (deg C)
Battery Holder	5	178.6	6.5	190.1
RA- Ethernet Conn	6	189.5	6.5	193.8
V-Power Conn	7	218.7	7	211.9

Conclusions from Case 2 Study:

Case study 2 reinforces the need for early DFM involvement, in particular a review of the PTH component selection and elements of the design which can affect the PTH barrel fill. Some improvements to PTH barrel fill are possible with process optimization; however, poor design factors cannot be fully compensated with process development alone. In cases where major DFM issues are identified as contributing to poor PTH barrel fill, every effort should be made to resolve these issues early in the product development lifecycle. In addition to physical layout changes, switching to an alternate functionally equivalent SMT part may be a viable option.

Several design changes have been made to the PCBA from this case study since the experiment was conducted. Many of the changes to the design were directly targeted to improve or eliminate the PTH hole barrel fill issues observed by addressing the various DFM issues on the PCBA. The highlights of the changes are listed in Table 7 and plans are in place to monitor the effects of these changes on the next prototype build.

Table 7 – Design Changes Made on the Test Vehicle Following the Experiment

PTH Connector Type	Initial DFM Issues on Test Vehicle		Changes Made on New Design Revision
	Classification	Issue	
Battery Holder	Major	Bottom Side Component Clearance	Component changed to an alternate horizontal SMT, non-PTH part
		Tail Length (Lead Protrusion)	
	Minor	Thermal Relief	
Header	Major	Pin to Hole Ratio	Component changed to an alternate gull-wing SMT parts or eliminated where possible
		Tail Length (Lead Protrusion)	
	Minor	Bottom Side Component Clearance	
		Thermal Relief	
RA – D-Shell	Major	Tail Length (Lead Protrusion)	Fixed – Longer Tail Length Part
	Minor	Bottom Side Component Clearance	Improved
		Thermal Relief	Improved
RA – Ethernet Conn	Major	Tail Length (Lead Protrusion)	Improved – Longer Tail Length Part
	Minor	Bottom Side Component Clearance	Improved
		Thermal Relief	Improved
RA – USB Conn	Major	Tail Length (Lead Protrusion)	Fixed – Longer Tail Length Part
		Thermal Relief	Fixed
	Minor	Bottom Side Component Clearance	Improved
		Pin to Hole Ratio	No Change
V – Power Conn	Major	Tail Length (Lead Protrusion)	Fixed – Longer Tail Length Part
	Minor	Bottom Side Component Clearance	Fixed
		Thermal Relief	Improved
V – USB Conn	Major	Bottom Side Component Clearance	Improved
	Minor	Thermal Relief	Fixed

Summary

From the above case studies, we note that for thick PCBAs used in server applications, the approach for ensuring product reliability requires a combination of design elements and process development. Each card assembly will have different attributes and technology elements, so it will require customization of process parameters and chemistries to achieve the optimum solution.

Temperature sensitive parts at SMT require active monitoring. Through profile iterations and assembly techniques, a profile which satisfies both the requirements of the component supplier and Pb-free process temperatures may be developed for many temperature sensitive components. However, when all attempts to meet these requirements have been exhausted, alternate components or assembly processes which do not violate the temperature profile requirements must be identified.

Achieving the PTH barrel fill requirements on thick PCBAs is one of the technical hurdles for a full Pb-free product transition and this should be a key focal point during early product design. It was demonstrated that design factors can create conditions on a large thick PCBA which results in low peak temperature in the barrel, resulting in poor barrel fill. Contact time at wave soldering has been identified as an important variable and those working on Pb-free assemblies are encouraged to perform process trials that include variation on wave direction to evaluate temperature conditions and PTH hole fill. Additionally, there exist in the market today newer technology and equipment, as well as alternative lead free alloys, which are worth exploring, as supplements to the ultimate, holistic wave soldering techniques for the often complex design of server PCBAs. The authors and companies involved in this study continue to investigate these through additional collaborative efforts.

Through early involvement with designers, selection of ideal components and optimized design will allow for processes to be developed that optimizes the temperature limits and solder attach properties. It is also suggested that if test vehicles are chosen for experimentation, they should closely represent the actual product so valid inference can be gained from the study.

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