

# INTERMITTENT CONNECTOR FAILURES IN ELECTRONIC ASSEMBLIES

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## ABSTRACT

Connectors are an integral part of any electronic assembly. As a result their reliability is a critical aspect for proper functioning of electronic systems, be it a mobile phone or a high end telecom server. There are a number of papers published on electrical connector failures that focus primarily on contact interface plating issues. From our failure analysis experiences we have identified numerous factors beyond materials or plating issues that can contribute to intermittent failures. Using complex electrical analytical techniques the failures were isolated to specific signals which were then subjected to in depth material analysis. Although in most cases the predominant failure mechanism is contact area corrosion the root causes have ranged from incoming raw material issues to mother board assembly process issues to end customer usage environments. This paper discusses findings from such case studies. It also discusses the corrective actions that were put in place for many of these cases.

Key words: Connectors, memory failures, contact area, electrical contacts.

## INTRODUCTION

The issue of having failures in electrical contacts has been a concern in all computer systems from a long time. Degradation of electrical contacts comes from the loss of the contact points or  $\alpha$ -spots which is critical for proper electrical continuity. There have been several studies to investigate the various mechanisms like degradation due to oxidation or corrosion of the contact interfaces [1]; fretting wear degradation of the contact interface, galvanic corrosion, mechanical vibrations and other mechanisms [2]. Included in this paper are four case studies for intermittent failures where each case deals with a different cause of failure. All of these cases are field failures and first go through electrical fault isolation using tools like the Time Domain Reflectometry (TDR), Input Translator Program (ITP), curve tracer and register probing. In most cases the failures are isolated to the interface between the connector pin and module gold finger for specific signals. Then both non-destructive and destructive physical analysis techniques are used to find the mechanism and cause of failure.

## CASE 1: PLATING THICKNESS AND ATMOSPHERIC CORROSION

This case study is part of the investigation into field failures at the DIMM connector level on mother boards from various customers and from a specific geographical location.

Customers were reporting intermittent memory failures, which in some cases disappeared when shipped or also moved from one location to another within the same work environment. Failures within a location were varied based on the proximity to the outside environment (near to windows and away from them). In order to do any failure analysis, the memory failure was frozen in place using epoxy on the DIMM connectors along with the memory inserted in them within the system at the customer site. Care was taken with the freezing technique to render the boards still useful for electrical failure analysis. These were later shipped back to the lab for fault isolation. The memory modules present on these systems were from two different suppliers (A and B). The connectors used had only one supplier.

Electrical failure analysis isolated the failures to the contact area interface on couple of pins for the memory connector using tools like ITP and TDR. As the systems were already frozen using epoxy, no visual inspection was possible on the gold fingers of memory modules and connector pins. But an observation on the systems which were returned was the amount of dust and dirt present on the backpanel, inside the chassis and on the surface of the motherboard.

Cross section was then performed in a top down direction (memory inserted into connector) on the systems which had the failing pins isolated, to expose the area of contact. This was done very slowly in order to avoid missing the area of contact. At the area of contact there was a corrosion product which formed a layer between the two mating surfaces for the isolated pins. The corrosion product originated from the connector pin side for some systems and from the memory module gold finger side, in other systems. EDX (Energy-dispersive x-ray spectroscopy) dispersive analysis of the corrosion product shown in Figure 2(a) confirmed it to be nickel oxide along with possibly nickel sulphide as shown in Figure 3. Nickel oxide is not electrically conductive and so it leads to the degradation of contact resistance between the two mating surfaces. As seen in the figure 2(a) this layer is around 1-2 micron in thickness and spreads along the interface. This can cause a mechanical separation between the two mating surfaces by pushing them apart.

From figure 2 (b) it is observed that the oxide seems to be oozing out from the connector pin, starting from the nickel layer underneath the thin gold layer. The nickel layer is being attacked by oxygen and is providing a continuous supply of metal to form the thick oxide layer. As it forms

the thick nickel oxide layer, it appears that there is a separation caused between the nickel and phosphor bronze layer of the connector pin. This in turn lowers the normal force leading to higher contact resistance.

The thickness of the gold layer on the connector pin is small. Supplier data indicated this gold thickness ranged from 2-10 microinches and therefore be classified as flash gold. Flash gold is generally known to be porous based on where the thickness lies in the range provided. If it is in the lower end of the range, less than 5 microinches, then it could be porous, non- uniform and can easily be removed after a few insertion cycles leading to exposure of underlying nickel layer. Nickel diffusion to the surface through pores in the gold layer can lead to oxidation. It is known that environment plays a role on contact resistance. Figure1 shows the effect on contact resistance of the growth of oxides on nickel, copper and silver surfaces[1]. High pollution (corrosive gases like sulphur dioxide SO<sub>2</sub> and hydrogen sulphide H<sub>2</sub>S) coupled along with high humidity levels can increase the rate of corrosion of nickel. Synergistic chemical reactions between the base metals with the corrosive gases and water lead to the formation of solid corrosion products that grow and creep out of the pores and spread along the contact area surfaces [3]. At ordinary temperatures nickel is not affected by H<sub>2</sub>S, but SO<sub>2</sub> can affect it above certain relative humidity (RH) values. This RH level can be reduced by the presence of dust & other hygroscopic materials [4].

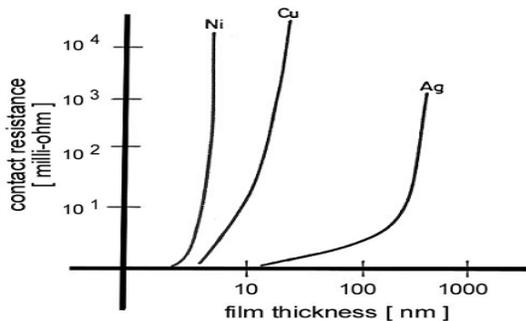


Figure 1 Effect of oxide thickness vs. contact resistance [1]

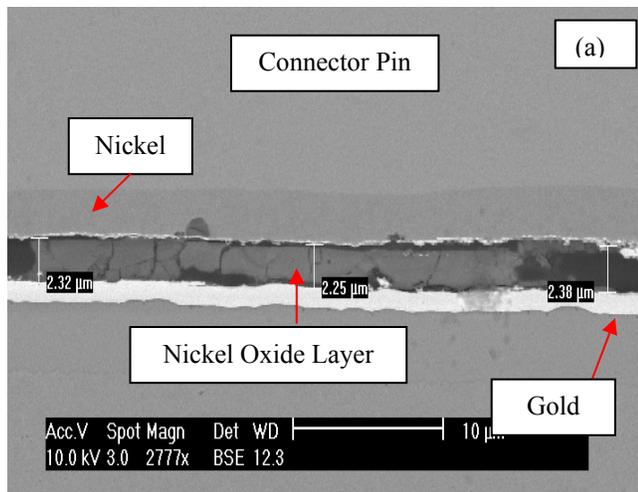


Figure 2(a)

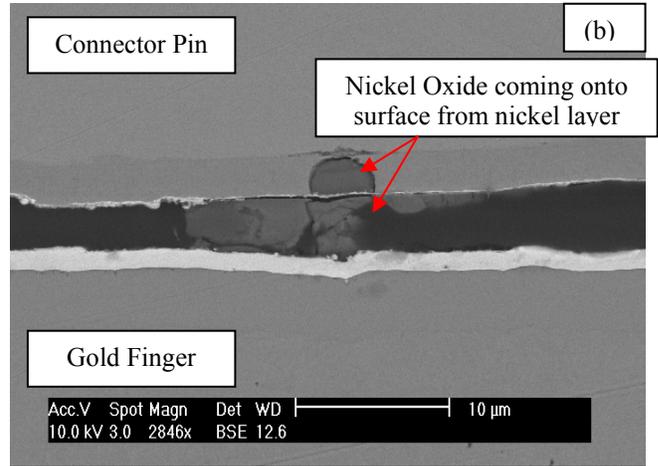


Figure 2(a) SEM image of the area of contact for one of the failing pins with Nickel Oxide layer between the mating surfaces. Thickness of oxide layer greater than two microns (b) High magnification SEM image of the area of contact for one of the failing pins with pore corrosion on the connector pin. Also note the separation in the intermetallic between nickel to phosphor bronze layer

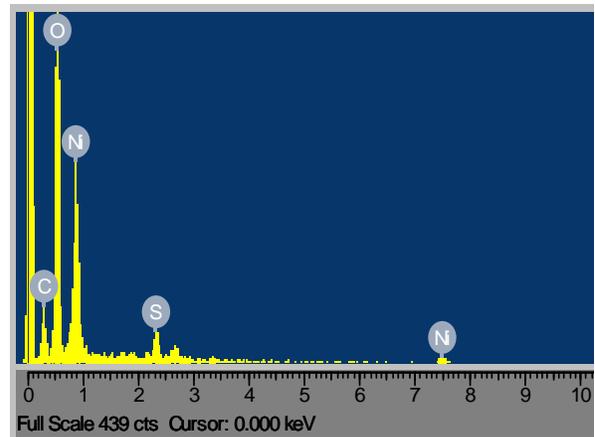
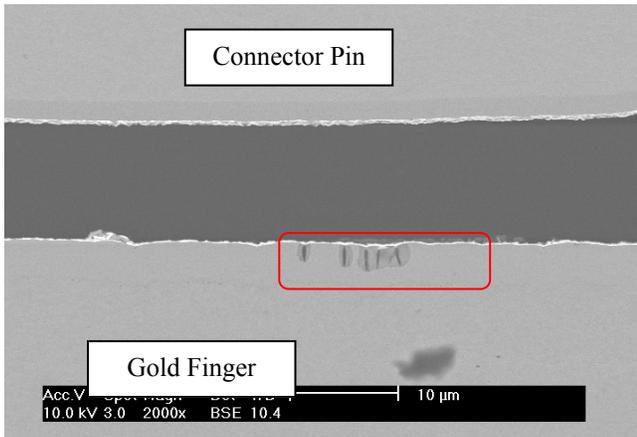


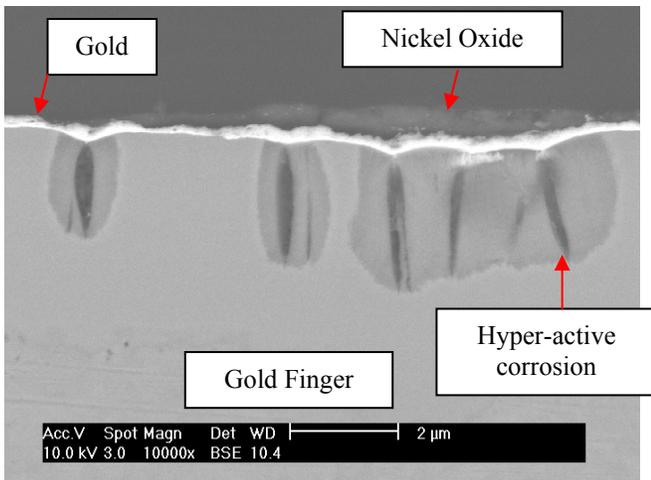
Figure 3. EDX spectra of the corrosion product between the mating surfaces indicating nickel oxide and possible sulphide.

Figure 4 shows the corrosion product forming from the gold finger of the memory module at the contact area interface. Nickel oxide is forming and coming onto surface where there is hyper corrosion of gold as seen in figure 5.

Hyper-active corrosion of gold is a phenomenon generally attributed to gold plating process on nickel plating with high phosphorous content. It causes non uniform plating and increases porosity locally at that location. The thickness of the gold layer on the gold fingers is less than or equal to one micron (~40 microinches). In order to check for porosity of the gold fingers, modules from both suppliers were subjected to five days Mixed Flow Gas (MFG) test. Post five days testing, the memory module from supplier B failed the porosity test as seen in Figure 6 whereas supplier A passed the test.

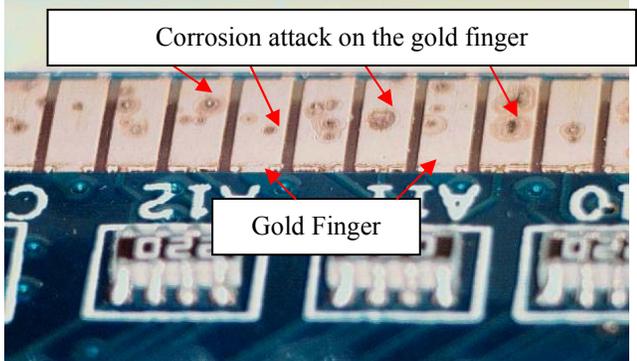


**Figure 4.** SEM image near the area of contact for one of the failing pins on a different board with memory module from supplier B.



**Figure 5.** Hyper-corrosion of gold on the gold finger and Nickel oxide forming on the surface

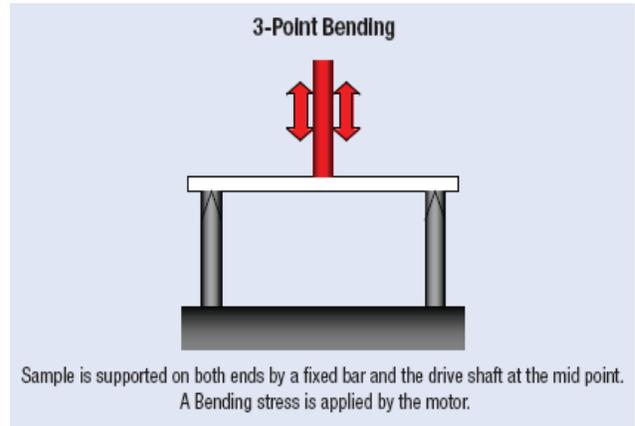
The corrective actions for this case involved using 15 microinches of electroplated gold on the connector pins for better reliability in medium harsh environments. Supplier B for the memory modules was asked to improve process control over their nickel and gold plating.



**Figure 6.** Optical image of gold fingers for memory module from Supplier B post 5 days MFG test showing a lot of pores

**CASE 2: CONNECTOR HOUSING MATERIAL**

This case deals with boards that were exhibiting intermittent video failures when they were in use continuously after a period of time. The failure was isolated to the interface of the graphics card to PCIe connector mating surface. The graphics cards used on these cards seemed heavier than those used on regular desktop boards. They were greater than 350 grams, seemed to produce quite a bit of heat and also was putting some stress on the connectors. So the investigation was focused on evaluating the connector housing viscoelastic property variation during operating temperature regimes that might result in any deformation of the pins leading to contact issues. Further investigation into history of the boards revealed that these boards were made with low temp nylon (LTN). In order to understand the property variations between high temp nylon (HTN) and low temp nylon materials, we also tested 2 unassembled connectors made of HTN. Using a Dynamic Mechanical Analyzer ( DMA) as shown in Figure 7, the viscoelastic properties of the materials were studied via a temperature sweep from 25C to 120C at a frequency of 1Hz under 3 point bend setup (cantilever set up was also tried but was abandoned due to sample flatness issues) as shown in Figure 8. The plastic housing of the PCIe (HTN and LTN) was cut and grinded to make it a solid thin strip around 1mm in thickness. The experimental data generated is expected to match intrinsic material property to a greater extent.



**Figure 7.** Schematic of 3-point bending [5] DMA analysis of the solid thin strips shows higher stiffness for HTN across any temperature range when compared to LTN as seen in Figure 8 & figure 9. The storage modulus values collected here are comparable to literature data points [6] as shown in Figure 10.

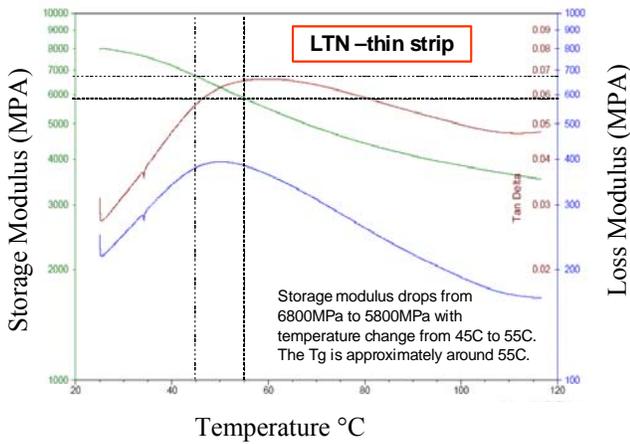


Figure 8 DMA data from LTN thin strip

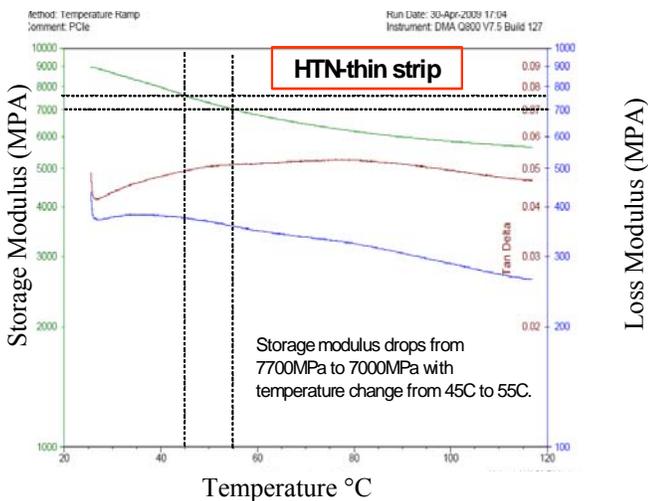


Figure 9 DMA data from HTN thin strip

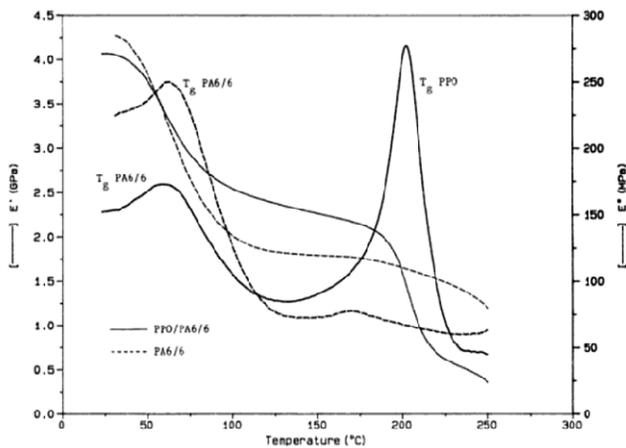


Figure 10 Literature data point collected from research published by Sepe et al [6]. Here PA6/6 refers to Nylon 6/6 where as PPO refers to an alloy of nylon 6/6 with PPO.

Based on the type of LTN used it was recommended to use additional solderable reinforcements to prevent plastic deformation. It was also recommended to change the connector housing material from low temp nylon to high

temp nylon for heavier graphics cards and also for boards that were being used for extreme graphics like gaming applications.

**CASE 3: Mechanical Damage at Line Integration**

Systems were exhibiting memory failures throughout the products early life cycle from integration to field failures. The systems prior to failure condition had passed all testing and verified as fully functioning. When a system failed during boot up it was found that up to half of the installed memory in these systems had been disabled. This failure condition adversely effected the operation of the system. The initial response at many end customers was to fix the systems by removing and reseating all DIMMs that were installed in the system. Although this reseating remedied the failure no understanding of the root cause was determined. In addition there is a possibility of systems failing again at a later date. Systems that were verified as having the above stated failure condition at end customer locations when shipped lost the failure signature. This information along with the fix that was implemented revealed that the failure condition was very fragile or intermittent.

A local customer in United States reported having failures corresponding to same reported failure mode and reported that they had 6 systems failing on a new installation of a large number of servers. All of the systems had failed for loss of various amounts of memory. It was found during electrical fault isolation that one system had a DIMM that had failed BIST (Built In Self Test) and the other systems had a DIMM that was not seen as being present in the DIMM slot. As there were 16 DIMM connectors close to each other, there was no room for probing [7]. Using ITP and register probing the failure was isolated to a pair of signals on 2 of the 6 failing boards by freezing the failure using a lock method which involved very little epoxy just at the latches and the keying hole.

Visual inspection was performed on the memory modules and DIMM slots of the systems which lost the failure signature. Most of the connectors showed mechanical damage to the connector housing body as shown in Fig 11.

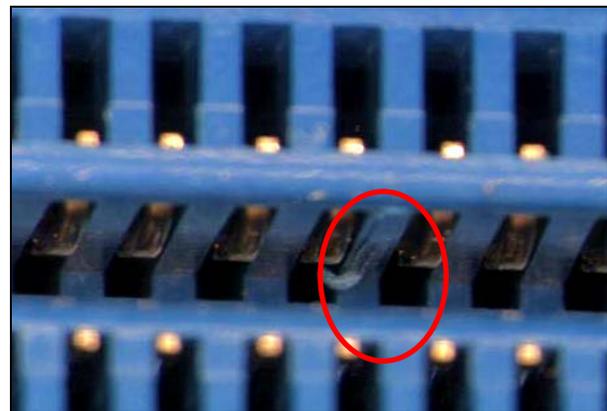
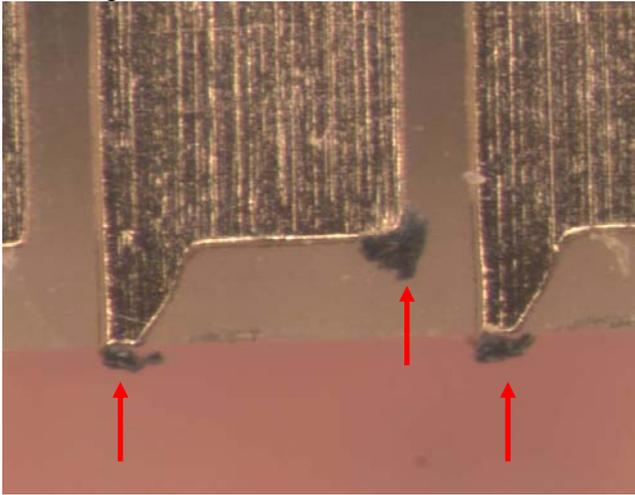


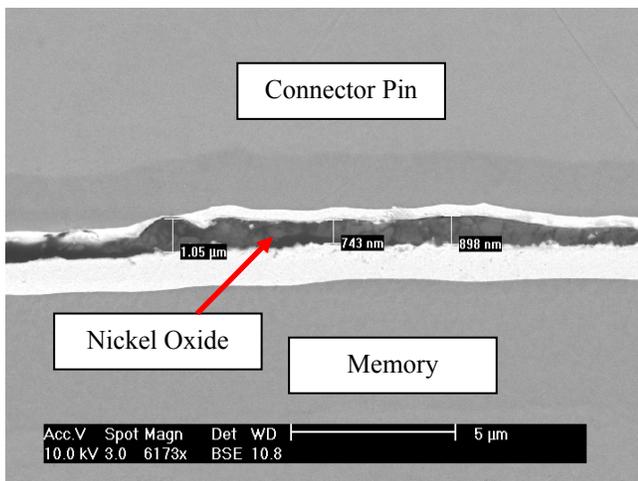
Figure 11. Optical microscope image of the connector showing scraping of the connector housing as indicated by the red circle above.

Inspection of the memory modules indicated deep wear marks and also connector housing debris at the bottom of the tie bar of the gold fingers on the memory modules as seen in Figure 12.



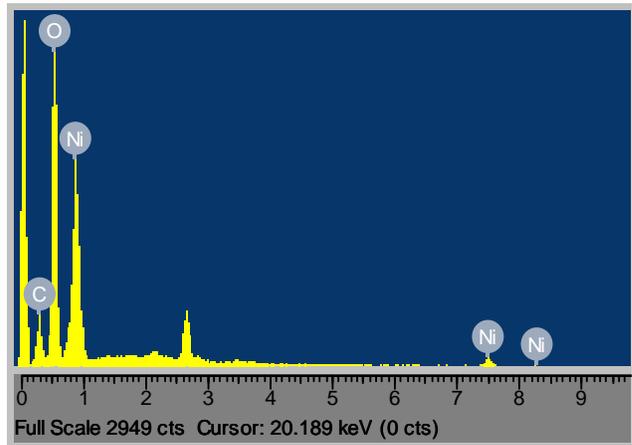
**Figure 12.** Optical microscope image showing connector housing debris on the memory module as indicated by the red arrows

Based on the visual inspection and intermittent failure mode, three hypothesis were put forth, i) plastic debris between the mating surface, ii) misalignment, iii) Contact surface issues. Data was collected by non- destructive and destructive methods to prove or disprove each of the hypothesis. Finally the data collected proved that it was a contact area corrosion issue. Corrosion product found between the mating surfaces in cross section was the failing mechanism for these systems as shown in Figure 13 below. It appeared from the two cross sections that the oxide layer was coming from the connector side.



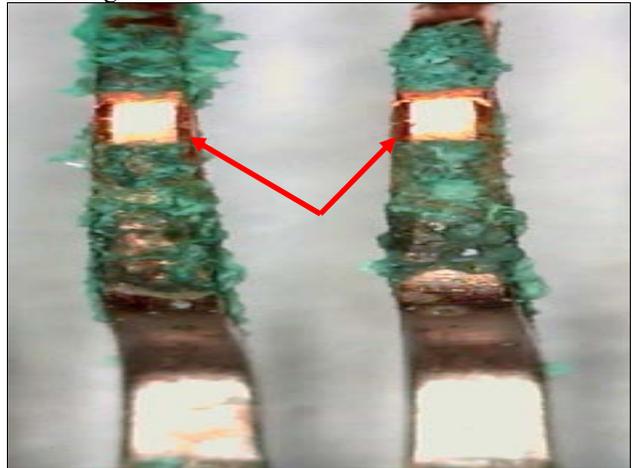
**Figure 13.** High magnification scanning electron microscopy image showing the presence of nickel oxide at the interface

EDX analysis for the corrosion product indicated it was nickel oxide as shown in Figure 14.



**Figure 14 .** EDX data indicating the product at contact area is nickel oxide

As the gold thickness on both mating surfaces looked acceptable, a nitric acid vapor porosity test as per EIA 364-53B was done on the connector pin to check for plating porosity. No porosity was found at the area of contact as seen in figure 15.



**Figure 15** Image showing the plating porosity test on the connector pins indicating no attack at the contact area

With less of a porosity concern, but deep insertion marks on gold fingers and connector debris on the tabs of the gold finger, the cross sections were inspected in detail to see for signs of any damage. As observed in Figure 16(a), (b), the gold was being displaced at the wear track region and pushed aside forming valleys and hills. Thus nickel exposure at those sites followed by oxide formation lead to the failure of the system. The connector pins of some of the recovered systems was inspected using SEM which indicated the wear mark was getting deeper as it went down from the top of the connector to the area of contact as seen in Figure 17(a), (b) below. Further investigation into the memory modules indicated the lack of a chamfer for the PCB (Printed Circuit Board) and so the gold or copper tabs were in direct contact with the connector housing and the connector pins. The next step was to understand how the memory modules in the systems were inserted into the DIMM connector. The factory indicated a manual process

for insertion. As there are 16 connectors close to each other, the memory modules would have been inserted in an angle thus having housing debris at bottom of the gold fingers and also the debris on the connector housing.

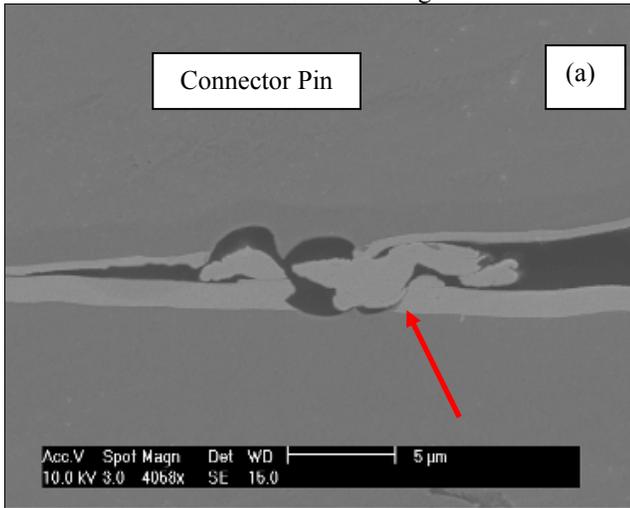


Figure 16(a).

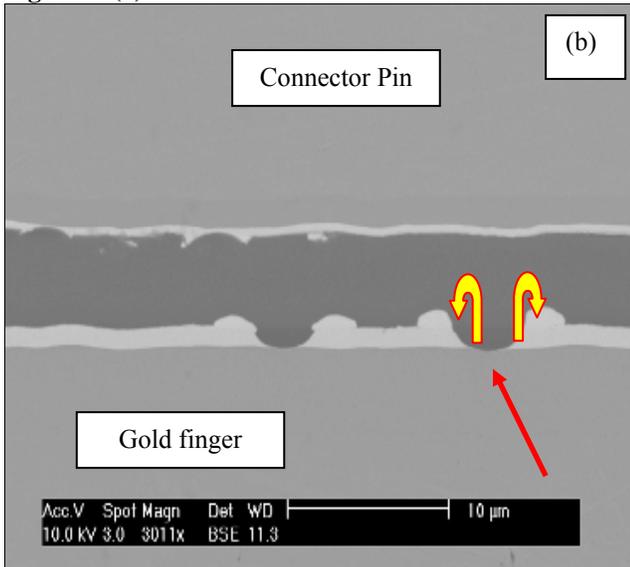


Figure 16(a). Scanning electron microscope image near the edge of contact area showing damage to the gold layer on both interfaces and the gold trapped in between.

(b) Scanning electron microscope image showing wear marks causing displacement of gold on both interfaces, making a hill and valley, thus exposing underlying nickel layer. The cross section is a top down one and so you are looking at the wear marks

The corrective actions implemented for the issue was to have the factory follow the JEDEC specification to insert the memory modules straight down, factory to investigate getting modules with chamfer to reduce any further reliability risk.

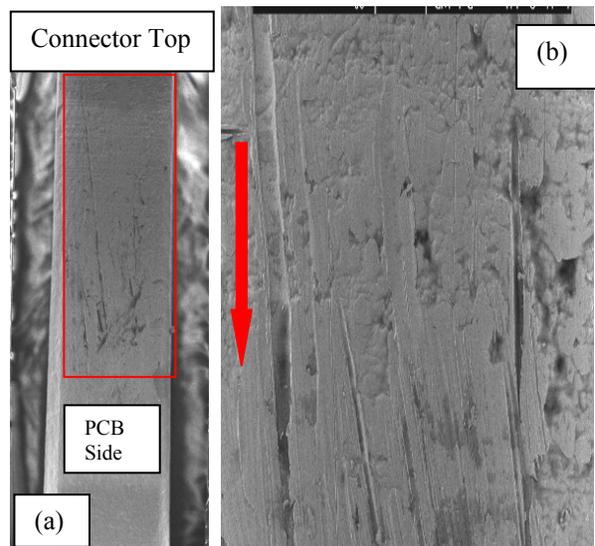


Figure17(a) Low magnification scanning electron microscope image of contact area for a pin. (b) High magnification scanning electron microscope image of the

#### CASE 4: PROCESS CONTAMINATION

This section includes cases where the intermittent failures were found on systems in the line integration stage. These failures are mainly due to contamination on the riser card gold fingers during motherboard assembly process. The case involved no display during POST and boards would not boot up. Visual examination of the riser cards indicated some excess solder on the back of the boards with some contamination on the PCB surface and visual contamination on pins as shown in Figure 18(a) and 18(b).

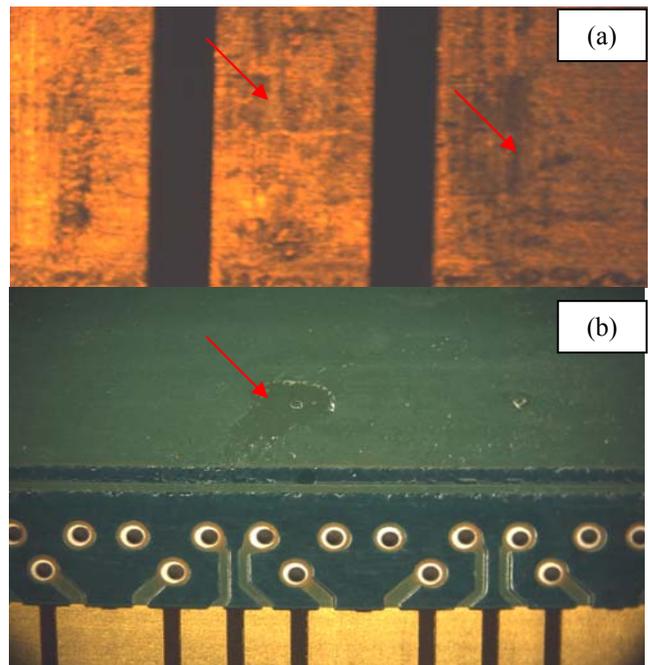
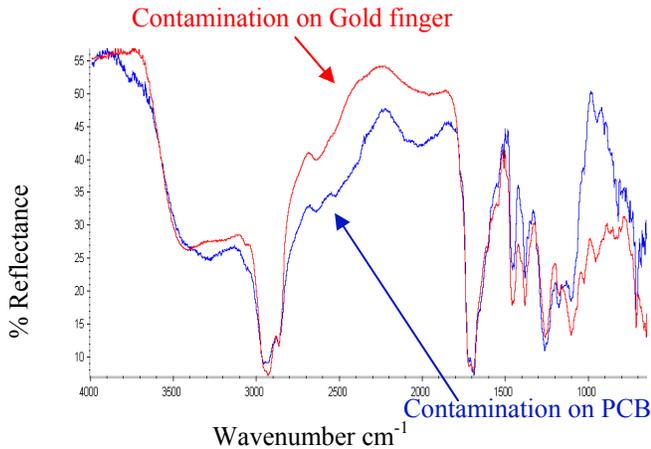


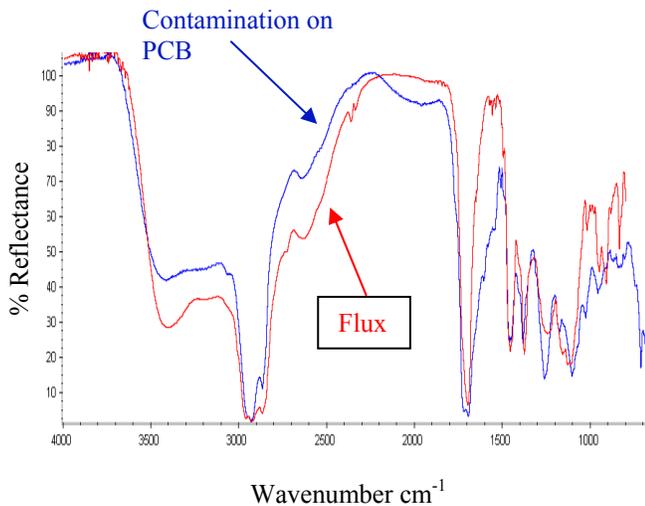
Figure 18 (a). Optical image of the gold fingers on the riser card showing contamination. (b) Optical image of PCB surface with the contamination

Upon cleaning the gold fingers the failure disappeared and the board became functional. Fourier transform infrared spectroscopy (FTIR) was used to analyze the contamination on both the printed circuit board and the gold fingers. The spectra for both the spots were collected and they matched very closely indicating the same contamination was present on both the locations as seen in Figure 19. The spectra were then compared to the flux spectra used in wave soldering for motherboard assembly.



**Figure 19.** Overlay of FTIR reflectance spectra of the gold finger contamination and contamination on PCB indicates it is the same contamination.

There is a decent match in the fingerprint region between the flux spectra and the contamination found on the board as seen in Figure 20



**Figure 20.** Overlay of FTIR reflectance spectra of the gold finger contamination and spectra of flux indicating a good match between the two in the fingerprint region

The corrective action in this case was a detailed cleaning process for the gold fingers after assembly. Using tape on the gold fingers during soldering was recommended. The type of tape used should not leave any residue behind.

## CONCLUSIONS

Connector reliability is extremely important to all electronic assemblies due to the constant changes in end customer usage conditions, and the heavy competition for better and cheaper products. As described in the four case studies which deal with connector raw material properties, damage induced contact area corrosion, corrosion due to plating issues and contamination based failures, intermittent connector failures are not necessarily related to contact area corrosion just due to plating issues. In all the four cases we observe that there is degradation of contact resistance at the mating surfaces due to various reasons. In order to resolve the issue and take proper corrective actions it is critical to understand and take into consideration materials, process, handling & integration issues as well as customer usage conditions.

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