INNOVATIVE BGA DEFECT DETECTION METHOD FOR TRANSIENT DISCONTINUITY

Steven Perng, Weidong Xie, Tae-Kyu Lee, and Cherif Guirguis
Cisco Systems, Inc.
San Jose, CA, USA
sperng@cisco.com

ABSTRACT
There have been extensive studies on large ASIC BGA warpage due to CTE mismatch. The resulting defect modes include solder bridging around corner pins, and Head-In-Pillow (HIP) joints around corner pins or under die shadow area.

As the increasing trend on higher routing density and transfer speed, VIPPO and back drill are becoming common features on high-end products. The interactions among these features and/or other features, i.e. the traditional dog-bone pad design, could induce a new failure mode that is different from what was abovementioned. Instead of the CTE mismatch on package material set, this new failure mode is induced by the CTE mismatch among the neighboring material, stack-up, as well as pad designs.

Recent studies on fine pitch memory devices showed, in some extreme cases, the interaction between PCB, solder joint, and package may introduce solder detachment on package side in the area of VIPPO and non-VIPPO mixed design. Since the detachment can be transient during the reflow process, the traditional post-reflow continuity testing will not be able to detect the defects. To detect the existence of solder detachment defect with transient nature, an innovative in-situ, real-time monitoring methodology is introduced. Utilizing specially design daisy chain test vehicles with data logger, the proposed methodology can effectively monitor the continuity of solder joints in real time during reflow or rework process. The methodology with proto type apparatus has been verified on fine pitch memory devices with VIPPO and non-VIPPO mixed design, and all VIPPO design.

This paper summarized the development of this innovative in-situ, real time methodology, which is capable of detecting BGA transient discontinuity. The potential of expanding this detection methodology for other applications is also touched briefly.

Key words: BGA, warpage, solder detachment, transient discontinuity, reflow simulator, liquidus, solidification timing, CTE mismatch, VIPPO

INTRODUCTION
Surface Mount Technology (SMT) is a Printed Circuit Board (PCB) level assembly process that primarily uses solders, previously eutectic tin-lead now lead-free solders, in forming interconnects between components and PCB. As the demand for higher performance within same or smaller form factor, the integration density on PCB increases dramatically over the years. The interactions between SMT components and PCB due to, such as, the mismatch of Coefficient of Thermal Expansion (CTE,) or uneven temperature distribution are amplified by the increasing complexity. These interactions may cause solder joint detachment from the pad and result in a defect solder joint.

Traditionally the solder interconnect quality can only be analyzed post assembly, using electrical testing and/or destructive failure analysis such as cross-section and dye-and-pry. The major drawback of such analysis is the difficulty of pinpointing the exact timing of when the failure or defect happened, which is one of the crucial information in root cause analysis, finding a mitigation solution, and subsequent implementation.

The current study proposes an innovative monitoring methodology, which utilizes specially design daisy chain test vehicles to monitor the robustness and healthiness of solder joints in real time during assembly and rework process.

MOTIVATION AND INITIATION
During the process development of a 0.8mm pitch memory device on a 0.147" thickness double sided board with OSP surface finishing, it was found solder detached from the pad on package side, as shown in Figure 1.

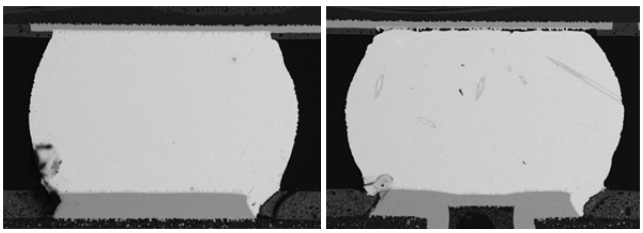

Figure 1. Comparison of with (left) and without (right) Solder detachment from the pad on package side

The detachment can be either a completely detached or partially detached. As the SEM image shown in Figure 2, the Inter-Metallic Compound (IMC) was formed properly on the package side. While on the ball side, the solder forms a smooth contour. Since there is no zigzag counter

fingerprint of the IMC layer on the ball contour, it suggests the detachment was occurred during the liquid phase, either during melting or during solidification.

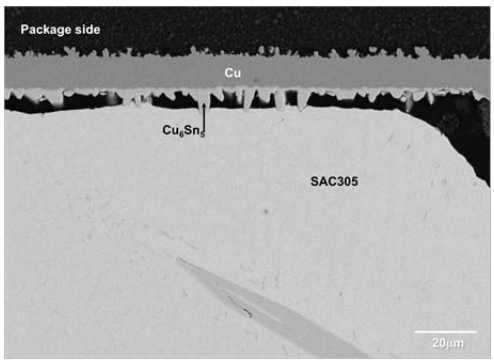

Figure 2. SEM image of solder detachment from the top right corner of Figure 1, the image on the right

Further analysis on the top surface of separated joints from samples went through second reflow showed numerals pinching marks. Broken IMC tips were observed in some of those marks (Figure 3). These pinching marks suggest the solder joints detached from package side and reconnected in liquid phase.

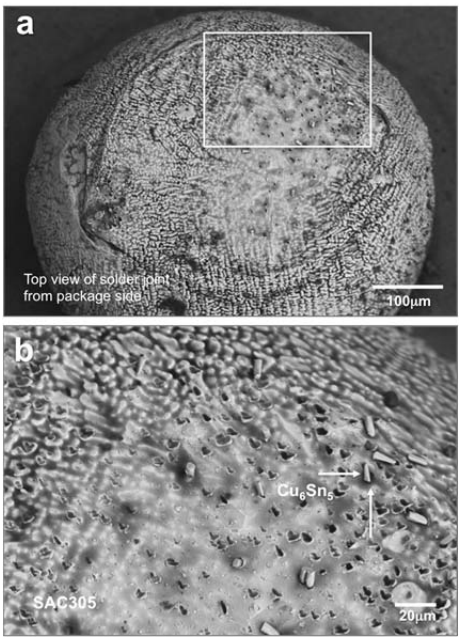

Figure 3. SEM images of (a) the top surface of the solder joint and (b) higher magnification on the surface with broken IMC tips

The Critical Factors Analysis

A DOE was conducted for root cause analysis. It was found the solder detachment only occurred during the second reflow cycle. In other words, the memory device must pass through two reflow cycles in order for the solder joint detachment to occur. The finding suggests solid solder joint has to be formed first, in order for the solder to detach from the package side.

It was also found the solder detachment occurred on VIPPO pad design only. As shown in Figure 4, the red arrows indicate solder joints with solder detachment. For those solder joints without VIPPO pad design, there was no solder detachment observed on either cross-section or dye-and-pry.

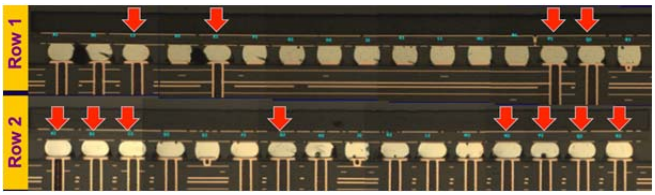

Figure 4. Solder detachment only at VIPPO pad design

To better identify the key factors, a reflow simulator was used to study the solder joints' behavior during reflow. Two memory devices were polished to the edge row (Figure 5) and placed in the reflow simulator to study the dynamic behavior of solder joint throughout the reflow cycle. It should be noted that the reflow simulator uses IR heating element; while the reflow oven is convectional. And, the temperatures referred are the chamber temperature of the reflow simulator oven.

Figure 5. Memory device polished to the edge row to be used for reflow simulator

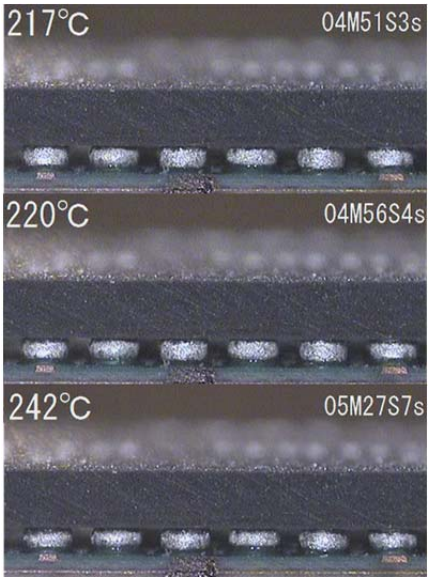

Figure 6. Still images from the reflow simulator video

From the recorded video clip, the completion of phase change of solder joint can be observed by a sudden change of surface texture. It is noted that the standoff of solder joints changed significantly before and after phase change. Shown in Figure 6 are some still images taken from the recorded video. The VIPPO joint was marked on the PCB

side with dark marker. It was also observed from the video that the liquidus temperature and timing between VIPPO and non-VIPPO joints were slightly different.

Since the sample has been polished to the edge row, the thermal behavior of the solder joints may have been changed. Further study is needed for more in-depth understanding and accurate prediction.

The Impact of CTE Mismatch in Combination With The Liquidus Timing Difference

At room temperature, Cu has CTE of 16 ppm/°C; while a typical PCB material has z-axis CTE around 45~70ppm/°C. However, as the temperature going above the glass transition temperature (Tg) around 180°C, the z-axis CTE of PCB can increase to the 250 ppm/°C range.

In summary, the questions need to be answered are

- Based on numerical modeling, liquid solder between two pads can be stretched up to 25mil before necking and breaking into two pieces. With warpage much less than 25mil, instead of stretching, what causes the liquid solder to detach from the pad on package side?
- What is the timing of the liquid solder detaching from the pad? Is it during heating up or during cooling down?
- Will some of the detached joints coalesce again? Will the coalescence results in a self-cured solder joint? Or, it just has contact without forming a joint?
- Is there an existing analysis tool to monitor the continuity of solder joint, which can pin point the time and temperature when solder joint detached or coalesced?

To address these questions, a methodology capable of detecting solder joint continuity in-situ and in real time has to be developed. A test vehicle with 0.8mm daisy chained memory devices is, therefore, designed.

CONCEPT OF THE METHODOLOGY

The idea of daisy chain test vehicle is to design the circuitry to loop all or partial interconnects together, such that the transient electric discontinuity (open/short) can be monitored in-situ and in real time. To correlate the electric transient discontinuity with the dynamics of soldering process, the goal is also to have resistance vs. time overlaid with solder temperature.

When a particular chain is connected to a data acquisition system, such as data logger or event detector, the resistance over time can be recorded then be analyzed to determine whether an open occurred. Collaborative with certain failure analysis such as dye-and-pry, the defects or failures then can be confirmed.

The resistance-time history can also be used to pin point the exact time of failures. During SMT, the chain may consist of solid metal wires, solid solder interconnects, and/or nonsolid solders form (paste or molten solder). Since the resistance of liquid metals is about twice of their solid form[1], the continuity of the daisy chain can be monitored during the entire process of assembly.

EXPERIMENTAL APPARATUS AND PROCESS

The effectiveness of the method has been verified with a board level daisy chain test vehicle. The test vehicle consists of four 0.8mm pitch Ball Grid Array (BGA) components, which have been assembled onto a 125mil thick 16-layer PCB (Figure).

Figure 7. Daisy chain test vehicle

It is understood that the thermally induced stress on solder joints are primarily driven by the CTE mismatch, resulted from mixing of PCB pad designs. To ensure the occurrence of solder joint detachment, two test vehicles are designed. One test vehicle has a mixture of Via-In-Pad Plated Over (VIPPO) pads and regular dog bone pads; while the other test vehicle has all VIPPO pads. The all VIPPO design is expected to have no solder joint detachment on package side.

Both test vehicles were assembled by regular SMT process with 4 memory devices. After inspected by X-Ray to ensure no anomalies being observed, the test vehicles were reflowed again using SRT rework machine.

Through out the rework process, as shown in Figure 7, a data logger is used to monitor the resistance of the daisy chain of each component. The daisy chain is routed with 4-wire configuration to eliminate the resistance noise induced by wires and connections.

In parallel, a profiler with thermocouples is set up to record the temperatures. It should be noted that the thermocouple was inserted underneath the component, without drilling into the solder joint. It is to minimize the impact due to destructive drilling. Measurement may deviate from true solder joint temperature slightly.

To confirm the finding from daisy chain resistance monitoring, both test vehicles were dyed and pried for any evidence of dye penetration and solder detachment.

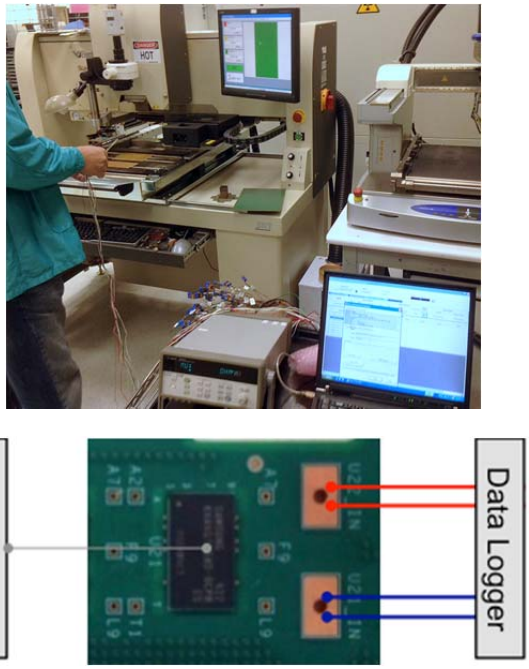

Figure 7. Data logger and profiler setup

RESISTENCE TEST RESULTS

VIPPO and non-VIPPO Mixed Pad Design

As shown in Figure 8, the resistance over time of each component is overlaid with the reflow profile, which is temperature over time (with respect to the second vertical axis on the right).

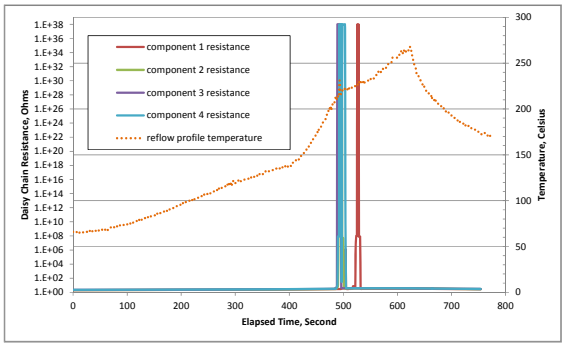

Figure 8. Resistance over time overlaid with reflow profile of the mixed pad design

For the mixed pad design, it is clear that all four daisy chains opened, during the solder joints were melting in the ramp-up stage. It should be noted that the vertical axis on the left hand side was capped by the cut off resistance values of the data acquisition system.

As the zoom-in view in Figure 9, the exact timing and temperature for a specific daisy chain to open could be determined.

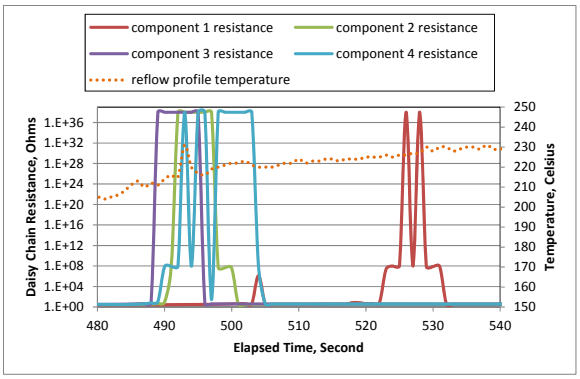

Figure 9. Zoom in view of the daisy chain resistance value, overlaid with reflow profile of the mixed design

The daisy chain of Component 3 opened first at 488 seconds with temperature at 212°C, followed by Component 2 and Component 4 within 2 seconds.

8 seconds later, the daisy chain of Component 3 reconnected at 496 seconds with temperature at 215°C. Similar trend was observed on Component 2 and Component 4.

With unknown reasons, Component 1 opened 34 seconds later than others, at 224°C. And, the daisy chain reconnected 10 seconds later at 230°C.

All four components exhibit discontinuity or solder open during the heating up stage around the melting temperature. And, after 8~10 seconds, the chain reconnected with 3~5°C temperature increasing.

ALL VIPPO Pad Design

As opposed to the mixed pad design, the ALL VIPPO pad design kept the continuity thought out the rework cycle, as shown in Figure . No sign of discontinuity is observed. The increasing of resistance from solid phase to liquid phase can be explained well by N.F. Morr [1].

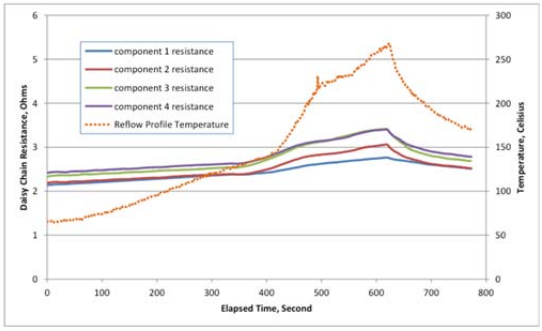

Figure 11. No discontinuity on resistance value for All VIPPO pad design

DYE-AND-PRY RESULTS

To confirm the finding from daisy chain resistance monitoring, dye-and-pry analysis was performed.

All VIPPO Pad Design
For the All VIPPO pad design, as expected, there was no dye penetration observed (Figure 10).

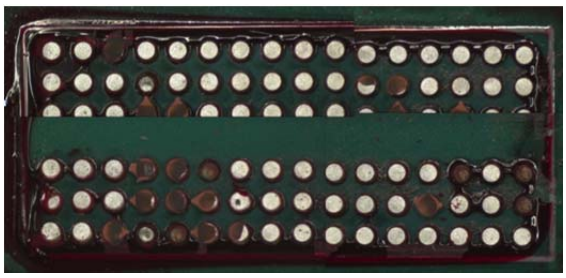

Figure 10. No dye penetration on All VIPPO pad design

VIPPO and non-VIPPO Mixed Pad Design
As shown in Figure 11, multiple full dye penetrations were observed on the solder joints with mixed pad design, indicating solder joints detachment occurred during reflow.

On the other hand, based on the Resistance-Time chart, the continuity of all four components reconnected few seconds after detachment. However, from the dye-and-pry images, some solder joints still exhibit dye penetration on the break away interface. It suggests, even the continuity been reconnected, the solder joint did not recover entirely. It either formed a partially connected joint or has contact for electric continuity without coalescing into a solder joint.

These solder joints are not reliable. It can be a latent defect. Which means, when under certain mechanical or thermal stress, it may fail in the field.

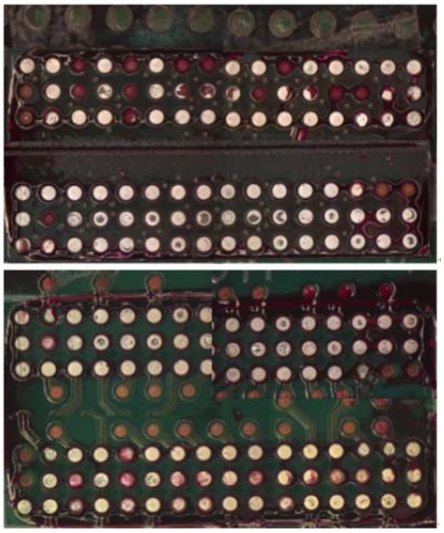

Figure 11. Dye penetration on mixed design, package side (top) and board side (bottom)

SUMMARY
An innovative detection method for BGA transient discontinuity using daisy chain circuit is developed. The detection method has been tested on a 0.8mm pitch memory device test vehicle with two pad designs, including VIPPO/non-VIPPO mixed pad design and All VIPPO pad design.

All four memory devices with mixed pad design exhibits solder joint discontinuity during the ramping up stage. The joints reconnected after few seconds consistently among the four devices.

The devices were put into dye-and-pry analysis. Dye penetration was found in multiple locations. Which suggests, after detachment, the solder joint either reconnect partially or has contact without forming a joint. These solder joints may pass electric test. However, it is not a reliable joint and will eventually fails in the field.

Since the solder joint discontinuity is a transient phenomenon, any post reflow electric test won't be able to detect the unreliable joint effectively. This category of solder joint is considered as having high-risk latent defect. More effort is needed for product level non-destructive detection method.

FUTURE WORK
The proposed detection methodology for BGA transient discontinuity can be implemented on a rework station only. It is not ready for being used in reflow oven, mainly due to the data logger used for resistance over time recording cannot withstand the temperature of the reflow profile.

The next phase is to develop a recording device, which can be sent into reflow oven to record temperature and resistance over time. This will provide an insight of transient soldering mechanism based on the different nature of reflow oven and rework station.

The study is limited to few samples. The finding so far may not include all the critical factors for solder detachment. With the detection methodology for both reflow oven and rework station, it is expected to have a more conclusive result in the near future.

ACKNOWLEDGEMENT
The authors would like to acknowledge Joseph Lee at Foxconn/San Jose and Paul Ton at Component Quality and Technology of Cisco for their contribution. And, Sanyo Saiko Co. Ltd. for the work of reflow simulator.

REFERENCES
1. N.F. Morr, "The Resistance of Liquid Metals", Proc. of the Royal Society of London, Series A, Containing Papers of a Mathematical and Physical Character, Vol. 146, No. 857, pp. 465-472, September 1934.