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iNEMI LEAD FREE WAVE SOLDERING PROJECT: AN INVESTIGATION OF THROUGH-HOLE ELECTRICAL INTERCONNECTS

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ABSTRACT

Today's wave soldering processes solder electronic assemblies within the large eutectic tin lead processing window. The issues surrounding the conversion to lead free assembly are multiple and varied. Logistics, cost, material selection, and equipment choices/options are some of these challenges that require planning and organization. However, at the core of lead free assembly is soldering. The iNEMI lead free wave soldering team embarked on a multi-tiered project that focuses specifically on two aspects: identifying the impact of critical parameters on the development of a reliable, robust lead free wave soldering process as well as characterizing the performance of the electrical interconnect.

While previous investigations of lead free wave soldering as well as standards development focused on process optimization, material selection, through-hole fill, coverage requirements, few, published investigations focused on the reliability of both SMD and Through-Hole solder joints assembled with various board finishes and thicknesses, component types, and alloys. This iNEMI collaboration studied and is reporting on identifying the impact of critical parameters on the development of a reliable, robust lead free wave soldering process as well as determining the behavior and performance of the various solder joints.

The team specifically designed a test vehicle for testing the norms of tin lead wave soldering and to address component and board types specific to various industries. The result of this investigation is to provide the electronics industry valuable information pertaining to the relationship between through-hole penetration and solder joint performance as a function of thermal cycling, and subsequent failure analysis.

Overall, this investigation looks to bring an understanding of how critical wave soldering parameters correlate to performance and provide the reader with the information necessary to make educated decisions in selecting process parameters, material sets, and acceptability standards.

Key words: Pb Free, wave soldering, process, solder, alloy, thermal cycling, joint performance.

INTRODUCTION

The 2009 iNEMI roadmap identifies several trends and transitions that are currently taking place in the electronics manufacturing industry. As a result, there are many challenges identified in today's electronics assembly. These challenges are identified as critical to assembling today's high volume electronics as well as the cutting edge technologies. The focus is assembly utilizing new materials, emerging assembly technologies, as well as meeting quality standards and cost constraints. The 2009 roadmap identifies specific gaps in the liquid soldering assembly area. The information, research and standards development relating to lead free liquid soldering processes and reliability is still in its infancy and the need for robust

information and standards is evident from the degree implementation of lead free compatible materials. [1,2,3] The Lead Free Wave Soldering project was developed in order to characterize and quantify the impact caused by the transition to lead free solder on the liquid soldering process itself as well as the impact on the performance and reliability of lead free solder joints. The 2009 iNEMI Roadmap board assembly chapter details both the progression of the integration of lead free materials Table 1 and also quantitatively provides the technology forecast for wave soldering and is listed in Table 2.

Parameter	Metric	2007	2009	2011
Solder Pastes	Lead-free % US	30%	50%	75%
	Lead-free % WW	60%	80%	85%
	Halogen-free	85%	90%	95%
	Low Temp. Assembly	<5%	<5%	5%
	Recycle ratio	<5%	10%	25%
	Alloys	SAC	SAC/Modified SAC	SAC/Modified SAC/Low Temp
Bar Solder	Lead-free % US	30%	50%	75%
	Lead-free % WW	75%	90%	95%
	Recycle ratio	5%	10%	25%
Wave Solder Flux	VOC free	15%	20%	30%
	Halogen free	70%	90%	90%

Table 1. The 2009 iNEMI Soldering Materials Forecast.[4]

Table 1 clearly illustrates two distinctive and nontrivial trends. The first challenge is that the integration of lead free materials in electronics assembly is not complete and will continue to increase for the next 5 to 8 years. The second and concerning trend is the drive to utilize alternative alloys for soldering. This latter trend is driven by economics as well as the desire to drive down operational soldering temperatures. This results in a lack of standardization, research efforts, and overall understanding. This challenge has been and continues to be addressed by the iNEMI Alternative Alloy project.

Parameter	Metric	2007	2009	2011	2013	2019
Wave/Selective Solder Flux	VOC free (%)	20	25	30	40	60
	Halogen free (%)	35	50	70	80	90
Wave/ Selective Lead-Free Alloy	Utilization % LF	50	60	80	90	95
	% SAC vs. other LF alloy	75/25	70/30	60/40	50/50	40/60
Minimum feasible PTH pitch in wave/selective soldering	Mil [mm]	80 [2.00]	60 [1.50]	50 [1.27]	40 [1.00]	40 [1.00]
Conventional/Selective Wave Soldering	Utilization % (conventional/selective)	80/20	75/25	70/30	65/35	65/35
SMT paste in hole/Wave Soldering	Utilization %	5	5	5	5	5
Pre-heat Process Temperature	0C	100-130	100-140	100-160	100-160	130-160
Wave pot Temperature	0C	260-275	260-275	260-280	260-280	260-280
Wave/Selective solder contact time	Seconds	3-7	3-7	3-9	3-9	3-10
Environment process	N2/Air	50/50	50/50	60/40	60/40	40/60

Table 2. Wave and Selective Soldering Technology Global Forecast. [4]

This updated table provides increased resolution on alloy composition, component pitch, contact time, and atmosphere compared to the 2007 iNEMI Technology Forecast. It is also the cumulative analysis of global liquid soldering situation. The technology forecast is also broken down by the following regions: Asia, Europe, and N. America. While the differences between the regions are material and board complexity based, all reflect similar patterns in most parameters listed.

The technology forecast continues to provide consistent data on the nature of the liquid soldering landscape. The issues today continue to be led by the enduring changes in materials and their maturity combined with a significant effort to minimize cost. Alloys containing silver adversely affect cost thus pressuring assembly houses to find alternative cheaper materials. Another pressure is the complexity of board technology. Today's high end board designs are quickly migrating to increased layer count, thicknesses, and complexity, thus exacerbating the challenges already associated with developing and maintaining a robust and reliable wave soldering process. This results in an overall situation where materials are pushed to the limits of their respective specifications in terms of exposure to elevated temperature for extended times. As the lead free implementation progresses, various questions have arisen.

This project was designed to address many of the challenges aforementioned.

For these and other similar reasons, the iNEMI Lead Free Wave Soldering Project focused on three critical areas:

1. Materials Selection
2. Process Optimization
3. Solder Joint Performance
4. Standarization

In order to achieve these goals the project participants developed a two-phase approach.

The companies supporting this project throughout Phase II included:

Figure 1. iNEMI Lead Free Wave Soldering Project Companies Supporting Phase II

The first phase of the project focused on characterizing process-related challenges and optimization of a lead free wave soldering process for various factors including: fluxes, alloys, and board thicknesses. Characterizing the window of opportunity for various materials specifically designed for lead free assembly and its impact on wave soldering process is based on the quantification and analysis of specific defects. The research performed in Phase I accomplished the aforementioned goal by investigating various levels of two factors:

- First, selection of a broad variety of materials allows for the determination of specific interactions. Alloys, fluxes, board laminate and finishes, component types and metallurgy, board design including thickness, thermal tie design, finish, and component orientation exert individual restrictions on the wave soldering process that results in an overall window of opportunity.
- The second factor is the flexibility allowed in developing the robust soldering process. Development of the wave process requires selection and control of various parameters including flux amount, atmosphere, preheat temperature, contact time, alloy temperature, and wave configuration.

The findings provide insight into the optimization of the wave soldering process for given material combinations. Confirmation of the data analysis was achieved by soldering boards utilizing the optimized parameter settings for the respective material combinations. The focus of this latter effort was to provide a data driven solution for the optimized wave soldering process which is an essential part of a robust and reproducible lead free assembly process. The scope of the project included accomplishing this goal for three different lead free alloys as well as for tin lead on three different board thicknesses.
The goal of the iNEMI lead free wave project is to ultimately characterize solder joint performance. Phase I provides the optimized settings that result in IPC class 3 acceptable through-hole fill for specific material combinations. Phase II of the project focuses on standardizing the lead free wave assembly process based on the Phase I process development and optimization so that only solder joint performance will be evaluated. The intent of Phase II is to provide the electronics assembly industry with timely and statistically backed understanding of lead free wave soldered joints.

In order to achieve this goal, the team designed and fabricated a test vehicle that aims to understand future assembly requirements and consequently develop new standards and best practices for lead free wave soldering assembly. This board's call name is "GTLO", Get The Lead Out! As shown in Figure 1.

It is with this board and component mix that the project derived solutions and specifications to the challenges posed in the technology forecast.

Figure 2. The Populated GTLO Board

EXPERIMENTAL
In the design of this experiment a subset of carefully selected materials were fixed for assembly. Criteria for the selection of these materials was based on the findings in Phase I so that assembly the only variable was board attributes and alloy. Wave soldering equipment use and setup was determined based on common industry practices, basic configuration and operation.

Materials
Fluxes
Soldering fluxes are known to exert a significant influence on the resulting solder joint. As a result, a single flux was selected and the process was optimized with this flux. Unlike in Phase I, the goal of Phase II was to achieve the best possible through-hole penetration and minimal amount of bridging.

Alloys
The various, available lead free alloys on the market today consist of tin in excess of 95%. As a result, the melting behavior of the alloys will be dominated by the melting point of tin, 232°C. In this experiment three lead free alloys were selected based on project interest at the time the experiment was executed. Tin lead was also included to provide a benchmark to the majority of today's production lines.

1. SAC 305
2. Sn100C
3. SACx
4. SnPb

Board
The test vehicle used in Phase II was a project designed board referred to as the "GTLO" board. The fabrication included the use of Polyclad 370 HR laminate with a 175°C T_g and a high T_d.

The layout of the GTLO required the use of 29 different components divided amongst through-hole and surface mount components. The GTLO board totally populated consisted of 356 components. Figures 2 and 3 illustrated populated top and bottomsides.

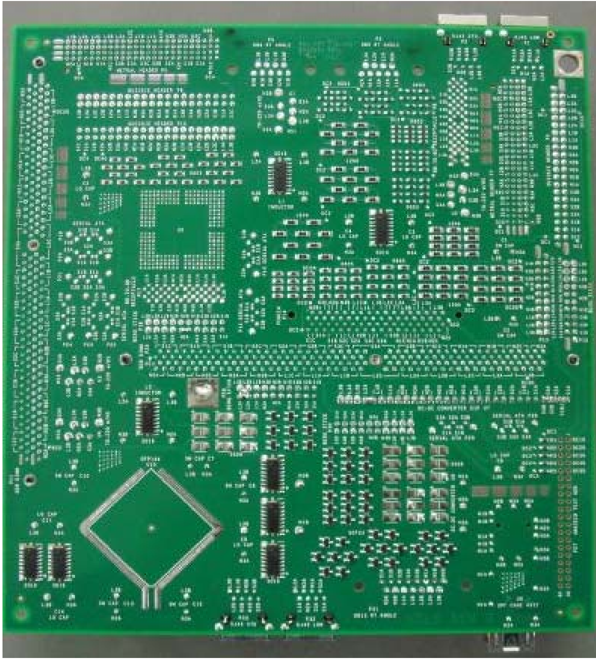

Figure 3. A Bottom Side View of the Populated GTLO Test Vehicle

The board dimensions were 185 mm x 203 mm, with two thicknesses: 1.6 mm (64 mil) and 2.3 mm (93 mil). The 1.6 mm thick card consisted of 4 layers of 2 oz copper and the 2.3 mm consisted of 6 layers of 2 oz copper.

The board finishes utilized in this test are listed below:

1. Cu OSP
2. Alloy Specific HASL
3. NiAu
4. Imm Ag
5.

For each of the three lead free alloys and tin lead, the respective board finish was applied. ie, In the experiments where SAC 305 alloy was used, the board finish was also SAC 305 HASL. The OSP applied was Entek Plus HT.

The board design also included variation in the following attributes and is dependent upon component type:
Drill Hole: 1 – 3 levels
Gap (hole:pin): 1 – 3 levels
Annular ring: 1 – 3 levels
Pad size: 1 – 3 levels
Orientation to wave: 1 – 2 levels
Thermal connection: 1 – 3 levels

The boards were soldered in an open pallet.

Components
The components assembled onto the GTLO board are Electrolytic Capacitor, Heat Sink, Power Inductor, RJ45, Header, DDR DIMM, Berg Stik, PCMCIA Header, Metral Header, TO-220, SIP DC-DC converter, SPF Cage Assembly, QFP144 0.65mm, SO16, SOT23, 0603, 0805, 1206.

Daisy Chains
There are 5 daisy chain circuits on each board. Each of the daisy chains has a number of probe pads built in to allow for electrical test. The 5 daisy chains were labeled as DIMM 1, DIMM 2, Metral 1, Metral 2, Surface Mount and are illustrated in Figure 4.

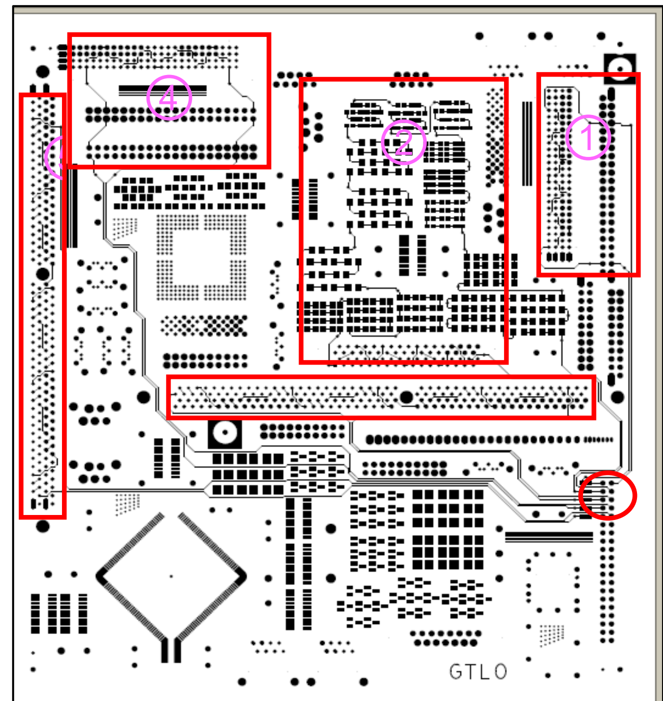

Figure 4. Illustration of the 5 Daisy Chains on the GTLO board.

Equipment
A Vitronics Soltec Delta 6622 wave soldering machine was used to assemble the boards for Phase II. The wave soldering machine was configured with a dual head spray fluxer which was operated with a pump system and delivered each flux with specifically designed nozzles. The preheat technology and configuration for the three zones of preheat consisted of forced convection modules in the first two preheating zones and a calrod module in the last preheating zone. The wave configuration consisted of a chip wave and main wave. The chip wave is designed to deliver a turbulent flow of solder and the main wave is designed to deliver a laminar flow of solder. The nitrogen inerting system works on the blanketing concept and was operating at the following N_2 flow settings of 30,50, and 80 l/min.

Parameter settings for each subsystem were controlled as required by individual runs in the design of experiments. Further, all systems, including transport, were calibrated to deliver directly comparable outputs. ie, The flux amount delivered was calibrated by flux type and conveyor speed so that a low amount of flux delivered to a board traveling at slow or fast speed was identical regardless whether the water based no-clean flux or the alcohol based flux was utilized. This was accomplished by measuring the mass, volume, and through-hole penetration of flux delivered to the board at all potential experimental conditions.

All alloys were contained in individual solder pots that were switched out as needed to complete the DOE. This was done in order to eliminate any possible cross contamination issues.

Design of Experiment

The premise of Phase II was to ascertain the impact of through-hole penetration to joint performance. To achieve this objective, the process was optimized for each board thickness based on visual inspection of through-hole penetration and minimal bridging. While the IPC 610D Class 3 or 75% hole-fill specification was utilized for guidance, the goal was to achieve 100% through-hole penetration. Once the quality of the product process was determined to be optimized all parameters were fixed and all boards were processed.

Profiles

Characterization of the temperature profile and contact time was accomplished by using the ECD Mole© profiler and the ECD WaveRider©. In the assembly of the GTLO board, two profiles were developed and utilized. One for the 1.6 mm card and a separate optimized process for the 2.3 mm card. Figure 5 illustrates a typical profile used to quantify topside preheat temperature and peak temperature on the Skate test vehicle.

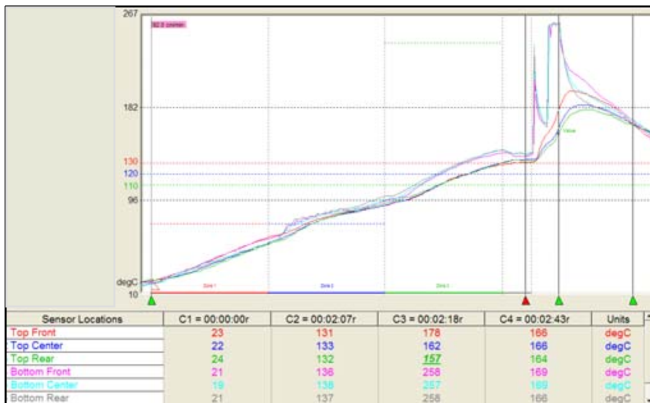

Figure 5. Typical Lead Free Wave Profile.

Analysis

Various forms of analysis were employed in Phase II. The reporting in this research is based on visual characterization of shorts and skips as well as x-ray analysis of hole-fill.

5 DX X-Ray Analysis

Hole-fill was determined by using a programmed Agilent 5DX x-ray instrument. The data collection of barrel hole-fill was based on the acquisition of data for 10 slices of the through-hole. Data on through-hole penetration was reported for the following slices; 0%, 30%, 40%, 50%, 60%, 70%, 75%, 80%, 90%, 100%.

Cross Sectioning

Select samples were cross sectioned to perform various analyses including hole-fill, barrel integrity, board integrity, and intermetallic formation. The procedure used to make these cross sections has been documented previously.[5]

Accelerated Thermal Cycling

The thermal cycling chambers were capable of conducting thermal cycling according to the specification given in the table below. IPC 9701 has been used as a guideline in terms of the Temperature Tolerances at the peak temperatures and the maximum allowable ramp rate between peak temperatures. Table 3 lists the required temperatures and ranges at board level that were recorded during the thermal testing.. The criteria for acceptable ramp rates are ≤ 20°C/min for the heating process or ≥ -20°C/min for the cooling process.

Criteria	Mandated Conditions
Cycles Conditions	(a) -40 to +125°C and (b) 0 to +100°C
Low Temperature Dwell Temperature Tolerance (preferred)	Minimum 10 minutes +0/-10°C (+0/-5°C)
High Temperature Dwell Temperature Tolerance (preferred)	Minimum 10 minutes +10/-0°C (+5/-0°C)
Ramp Rate	≤20°C/min

Table 3. Temperature Cycling Requirements (ref: IPC 9701)

Table 4 details the criteria for chamber setup, monitoring, electrical calibration, and event detection limits and error logging.

Test Parameter	Mandated Conditions
Temperature (Chamber Characterization)	▪ Characterization studies using representative sample loads and fixturing should be conducted prior to testing to ensure meeting the required thermal profile. ▪ Thermocoupled boards should be both at the perimeter and center of chamber.
Temperature (Chamber Test Monitoring)	▪ Continuous monitoring of temperature at board level, on at least two boards (at center and perimeter), as well as chamber ambient, throughout test.
Temperature (Procedure)	▪ Boards should be placed with respect to the air stream so that there is no obstruction to air flow across and around the boards.
Electrical (Zero time Set up)	1. Prior to testing, the 5 daisy chains on 5 different boards will be measured, at each intermediate probe point. 2. These values are then recorded and averaged to establish a zero time resistance value for the testing.
Electrical Test Monitoring	▪ Continuous Monitoring or periodic scanning with data logger
Electrical Failure Definition	▪ 1000 ohm threshold and sustained for 10 consecutive events.
Electrical Failure Logging	1. After a failure is noted, the board is removed for probing. 2. The exact location on the daisy chain is recorded. 3. Board is returned to testing.
Test Duration	▪ 6000 cycles.

Table 4. Criteria for ATC Chamber Setup and Event Detection.

RESULTS AND DISCUSSION

The execution of Phase II included the fabrication of the test vehicle, applying the correct finish onto the defined board thicknesses, procurement of the components, surface mount assembly and glue cure, flux procurement, and equipment setup. Once this was in place, a total of 501 boards were assembled per the fixed optimized processes for each board thickness. The boards were visually inspected on site, followed by the characterization of through-hole solder penetration by 5DX. As explained in the Experimental section, the criteria employed to determine the output response was hole-fill greater than 75%.

The major input factors and respective levels selected in this study are;

» Alloy - SACx, SAC305, Sn100C
» Coating - CuOSP, NiAu, HASL
» PCB Thickness - 62 mil, 93 mil
» Component
» Pin number - component determined
» Pin dimension - component determined
» Pin Configuration - staggered, parallel
» Pin Shape - Round, Rectangular/Square
» Pin Pitch – component determined
» Lead Length – both component determined and controlled
» Drill Hole Diameter - lumped into small/normal/large
» Annular Ring - lumped into small(1)/medium(2)/large(3)
» Pad Size – component determined
» Orientation - 0, 90, 180, 270
» Thermal Connection Type - none, type 1, type 2

Through-Hole Penetration Analysis

The results of though-hole penetration were organized utilizing best manufacturing practices as well as per IPC 610D requirements for Class 3. Table 5 lists the grouping of all soldered through-hole joints.

Coating	PCB Thickness	Total Boards	Total pins	percent with 100% hole fill	percent with hole fill >/= 75%	percent with hole fill < 75%	
NiAu	62	38	38038	83.6%	99.8%	0.2%	highest hole fill
HASL	62	17	17017	83.4%	99.8%	0.2%	↓
HASL	93	18	18018	97.6%	99.5%	0.5%	
HASL	62	16	16016	94.9%	99.5%	0.5%	
CuOSP	93	41	41041	97.0%	99.4%	0.6%	
CuOSP	62	40	40040	83.9%	98.9%	1.1%	
NiAu	62	23	23023	83.9%	98.6%	1.4%	
CuOSP	62	24	24024	79.9%	98.6%	1.4%	
HASL	62	16	16016	77.3%	98.5%	1.5%	
NiAu	93	23	23023	96.4%	98.3%	1.7%	
CuOSP	93	23	23023	94.0%	98.3%	1.7%	
NiAu	93	23	23023	94.5%	98.2%	1.8%	
NiAu	62	22	22022	67.4%	97.9%	2.1%	
NiAu	93	33	33033	94.0%	97.2%	2.8%	
CuOSP	62	23	23023	83.3%	97.0%	3.0%	
CuOSP	93	23	23023	73.0%	87.8%	12.2%	lowest hole fill

Table 5. List of Through-Hole Penetration for All Alloys, Board Finish, and PCB Thickness.

The goal was to first determine the overall through-hole penetration for all the combinations. Organizing the raw data into three categories: 100%, greater than or equal to 75% and less than 75%, it was possible to characterize the results of the GTLO assembly. In all cases except one, a through-hole penetration of 97.0% was achieved. The last cell containing only 87.8% through-hole penetration was an anomaly and cannot attributed to the materials but most likely to a manufacturing issue.

Further analysis of the SAC305 NiAu assembly returns the following results illustrated in Figure 6.

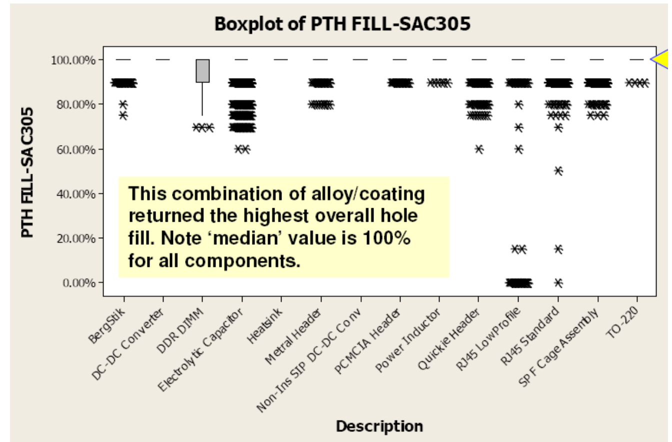

Figure 6. Boxplot of Through-Hole Penetration for the SCA305 NiAu Cell.

While the Median for through-hole penetration is 100%, the graph illustrates those vias that did not have the 100% fill based on component type.

The impact of board finish is illustrated in Figure 7. The analysis clearly shows that the HASL finished soldered the best as compared to CuOSP and NiAu. The resulting process window for CuOSP and NiAu are smaller.

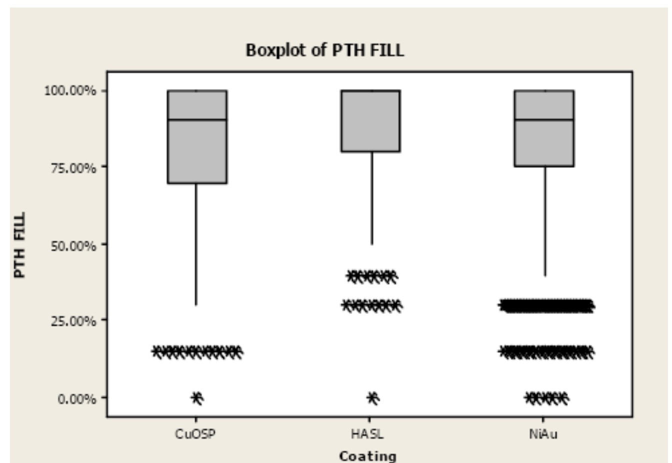

Figure 7. Impact of Board Finish on Through-Hole Penetration

The resulting interpretation of the through-hole penetration analysis can be summarized by a binary system where best or worst combination of factors are ranked in achieving 100% through-hole fill. In order to do this, the factors were divided into main and style factors. The main factors include board finish, board thickness, and component orientation. The style factors include hole size, annular ring, and thermal connection. The results are illustrated in

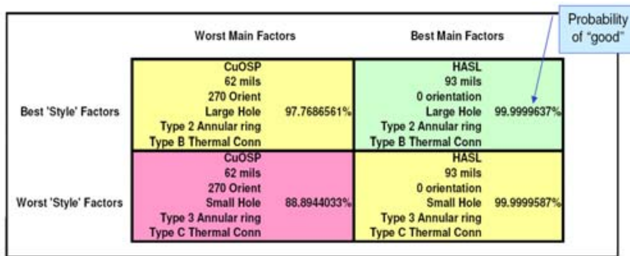

Figure 8. Probability of Achieving 100% Through-Hole Penetration Based on Board Design Factors.

The best main factor of board thickness returned that the thicker board was better. In general this is counterintuitive especially since two additional layers of 2 ounce copper were added. In this case, it can be accounted for by the fact that the two thicknesses were soldered utilizing two different processes in which the soldering process for the thicker board was optimized to a higher degree.

Overall, this data can be used as a guideline for board design in those cases where the designer has control to implement specific attributes. This upstream "best practice" will assist in achieving the best possible quality.

Accelerated Thermal Cycling

At the time of this paper, all accelerated thermal cycling of the 133 GTLO boards completed 6000 cycles as per the project's requirement. While most of the PTH solder interconnects passed the complete regimen of cycling, there were some interesting observations made. However, not all of the data has been analyzed at time of publication and will be published at a later time. The data illustrated in Figures 9 and 10 graphically illustrates the analysis of the passive component surface mount chain for SnPb and Sn100C alloys. Both exhibit quasi normal distribution of failures but over different timeframes.

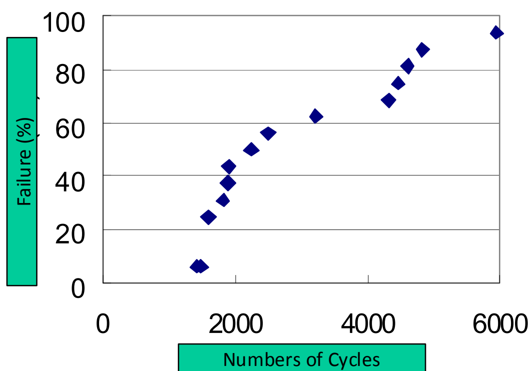

Figure 9. Passive Component Failure as Function of ATC for Sn100C.

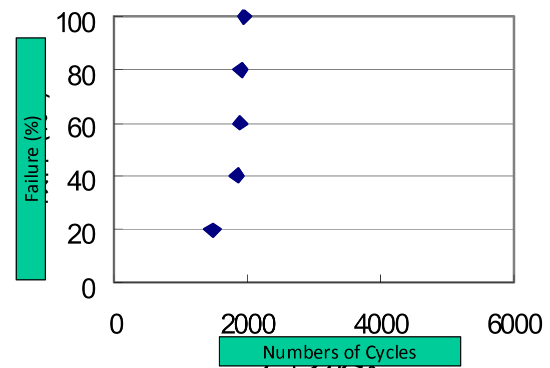

Figure 10. Passive Component Failure as Function of ATC for SnPb..

CONCLUSION

This research provides insight into several of the key questions and challenges observed in today's lead free wave soldering process. The iNEMI lead free wave soldering team embarked on a multi-tiered project that focuses specifically on two aspects: Identifying the impact of critical parameters on the development of a reliable, robust lead free wave soldering process and determining the process that achieves the optimized soldered joint.

This collaborative effort investigated the relationship of board design factors to through-hole penetration and joint integrity/performance.

Addressed in this study are inspection criteria, failure definition and measurement, followed by root cause analysis and ultimately optimized process confirmation. The result of this investigation was to lay the foundation of a broader effort to characterize the performance of through-hole solder joints on a test vehicle specifically designed for testing the norms of tin lead wave soldering.

Overall, this investigation looks to bring an understanding of how critical wave soldering parameters influence the various outputs. It also attempts to provide the reader with the information necessary to make educated decisions in selecting board attributes and materials in this ever changing environment. It is critical to understand, identify and control various process parameters in order to execute a rational implementation strategy for a reliable and robust lead free wave soldering process that results in the highest quality product.

ACKNOWLEDGEMENTS

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