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IMBEDDED COMPONENT/DIE TECHNOLOGY (IC/DT®): IS IT READY FOR MAIN STREAM DESIGN APPLICATIONS?

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ABSTRACT
Military and aerospace electronics providers continue to push the technological envelope to design and manufacture leading edge electronics for today's DOD users. Current design problems are not driven by circuit design capabilities but by an inability to reliably package these circuits within size and weight requirements (SWAP) outlined by the system level specifications. Innovative packaging techniques are required in order to meet the increasing size, weight, power, and reliability requirements of the DOD without sacrificing electrical, mechanical, or thermal performance. Emerging technologies such as those imbedding components within organic substrates have proven capable of meeting and exceeding these design objectives for meeting size, weight and power requirements. The ability to design smaller, lighter and less power circuit board assemblies that are more robust than conventional SMT boards has a future in the electronics of tomorrow. Imbedded Component/Die Technology (IC/DT®) addresses these design challenges through imbedding both active and passives into cavities within a multi-layer printed circuit board to decrease the surface area required to implement the circuit design and increase the robustness of the overall assembly. This paper discusses the design methodology, and validation / test data gathered during the implementation of IC/DT® in a mixed signal prototype. The prototype designed and assembled using IC/DT® processes was subjected to reliability testing and ultimately demonstrated in a test flight. The results from this testing as well as the future designs utilizing IC/DT are presented.

Key words: Size, Weight, Power, Reliability, Hi-Rel, 3D Assembly, Cavities, Thermal Core, Imbedded Components, IC/DT, and SWAP

INTRODUCTION
The electronics industry has seen an explosion in development of new materials and processes to support the demand for "smaller, lighter, faster, and better" products [12]. In the high reliability electronics sector, military and aerospace electronics providers continue to push the technological envelope using these new materials and processes to design and manufacture leading edge electronics for today's users. These advanced electronic assemblies are necessary to enable the leap-ahead that is required of today's military hardware to better equip our nation's defense.

Current design limitations are not driven by circuit design capabilities but by an inability to reliably package these circuits within the space constraints. As system designers continue to integrate more capabilities on a single platform, packaging engineers are tasked with the responsibility to ensure reliable electrical, mechanical, and thermal performance in the field. Innovative packaging techniques are required in order to meet the increasing form, fit, and function requirements of this industry without compromising reliability and robustness.

Over the last decade, packaging technologies have seen a shift in pursuit of achieving these requirements through the use of 3D integration [1]. Whereas most new products have defined X and Y dimensions, added capability is left confined to integration within these boundaries, forcing engineers to rely on miniaturization that can only be achieved through using the smallest form and fit factor components and interconnection in the Z direction. Packaging technologies are being employed that integrate bare die of both actives and passives into package designs such as Multichip Modules (MCMs), System-in-Package (SiP), Chip-on-Board (COB), and emerging system-level designs such as Imbedded Component/Die Technology (IC/DT®), which imbeds actives (bare die) and passives in cavities within the printed circuit board (PCB) [2].

In a paper presented at SMTA's Pan Pacific Conference in 2004, the features and advantages of imbedding active and passive components were presented [3]. Over the last 4 years, STI has since completed development of an imbedded die manufacturing process and patented [4] this unique packaging technology coined Imbedded Component/Die Technology or commonly referred to as IC/DT®. Imbedding unpackaged components, i.e. bare die, enables the miniaturization of electronics hardware that current packaging technologies, such as SMT, cannot provide.

Today we have achieved a TRL 8 on this IC/DT technology after successfully demonstrating successful flight of a SM-2 MISSILE utilizing IC/DT designed hardware as well as kicking off a number of new designs utilizing this design concept. The answer is yes main stream design engineering is ready for the integration of IC/DT® into future designs needing the ability to meet SWAP - SIZE, WEIGHT AND POWER REDUCTION to meet future system level requirements requiring SWAP initiatives.

TECHNOLOGY DESCRIPTION

This Imbedded Component/Die Technology (IC/DT®) packaging approach addresses miniaturization, thermal management, performance, reliability, and system capability requirements through innovative design guidelines and materials selection in order to meet form, fit, and function requirements [12]. Elimination of external component packaging not only reduces circuit card assembly (CCA) size, weight, and electrical and thermal parasitics, but it enables the 3D assembly of multiple components facilitating the design integration of key subsystems, i.e. multiple CCAs, into a single high-density module.

Miniaturization is achieved fundamentally due to the elimination of external component packaging. IC/DT® utilizes unpackaged components, known as bare die, for design with the smallest form and fit factor available. Component geometries can be reduced up to 85% through the removal of external lead frames, package substrates, and overmold encapsulants. These die are then imbedded in openings/cut-outs of the PCB, commonly referred to as cavities (Figure 1). Imbedding die in cavities in the substrate facilitates Z-integration through imbedding die on tiers, or exposed layers, within the substrate.

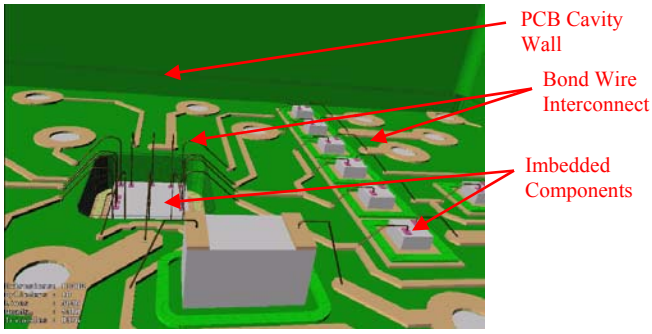

Figure 1. Active and passive components are imbedded in a cavity on a laminate substrate.

With the available real estate on the PCB provided by reduced component footprints, additional systems or capabilities can be added to an electronics assembly. System capabilities can be increased through the integration of additional features and functionality and/or redundant system within the same envelope. For example, processing architectures, such as those implemented in field programmable gate arrays (FPGAs), may be easily scaled to increase the number of processing elements (increased capability and system functionality) within the same PCB envelope due to component-level miniaturization.

Elimination of secondary packaging materials plays a significant role in the overall weight reduction achieved through imbedding unpackaged die. Interconnect materials that physically and electrically connect the integrated circuits (ICs) die to the circuitry are eliminated. In addition to the reduction in component packaging mass, there is also a reduction in the mass related to the electrical interconnect material. A significant mass savings is achieved by using wire bonds rather than solder because of the decreased volume of material per connection, as well as the lower density of typical bonding wire alloys compared to solder.

Reliability of the end product is improved not only by a reduction in interconnect material mass (translates to less applied force [F=ma] under load), but also through the increased flexibility of the electrical attachment. Through the use of wire bonding technology as the electrical interconnect process, very flexible light-weight interconnects are created. This flexibility is exploited during operation in demanding thermal and mechanical environments such as high temperature, vibration, and/or mechanical shock. In contrast to a soldered connection, which localizes the applied stress, the IC/DT® concept distributes the applied stress producing a more robust and rugged electronics product.

IC/DT® improves long-term signal reliability by eliminating unnecessary failure opportunities and utilizing reliable electrical interconnects. All first level component packaging is eliminated. This eliminates two to four possible modes of electrical failure associated with component-level packaging. Due to the removal of external packaging, electrical parasitics and thermal resistance are reduced improving overall system performance as desired in high speed, high I/O systems such as those found in missile defense systems.

Conventionally, a high power CCA would dissipate heat through convection or radiation from the component and substrate surfaces, often including package-level heat sinks or cooling fans. However, advanced handheld applications inhibit the use of these passive and active cooling devices. Therefore, IC/DT® provides a solution through relying on passive cooling via conduction to a single, central cooling core to remove heat from high power devices and to evenly distribute the thermal energy along the interface. Through creative thermal management, die junction temperatures (T_J) are reduced which increases the performance and longevity of the electronic components and further increases system-level reliability [3].

TECHNOLOGY PROTOTYPES

STI has recently completed testing of two prototype vehicles to serve as a technology demonstration of the design guidelines, materials, and manufacturing processes used to imbed passive and active devices in laminate substrates [12]. Environmental stress testing was conducted on these prototypes to evaluate the robustness of imbedded bare die in an organic laminate substrate in conventional military and aerospace environments (harsh environments).

Test Vehicle 1

A test vehicle was designed to evaluate the effectiveness of assembly materials in harsh environments when imbedding bare die (silicon die) in organic laminate substrates. The test vehicle consisted of multiple imbedded die (Figure 2) wired to inner layer tiers for monitoring fluctuations in

resistance during/after environmental testing. The imbedded test die consisted of daisy-chain components with peripheral bond pads for interconnecting to a test substrate. Test patterns on the high temperature FR4 (HT-FR4) laminate substrate enabled in-situ resistance monitoring of the assembly during testing. A conformal coating, encapsulant, and lid were used (Figure 3) to protect the imbedded die from physical damage (handling/transportation) and the environments (ionic contamination, moisture ingression, and vibration dampening).

Test Coupon Parameters

- Substrate: 4.0 x 6.0 inch HT-FR4, laminate PCB, three tiers
- Imbedded Core: copper core, Ni/Au plating
- Die: 0.248 x 0.240 inch silicon die, daisy-chain design, peripheral wire bond pads
- Die Attach: compliant epoxy, thermally conductive, electrically insulative
- Interconnect: Al/1%Si wire
- Conformal Coating: Parylene C
- Encapsulant: silicone gel
- Lid: laminate with top/bottom copper plane layer

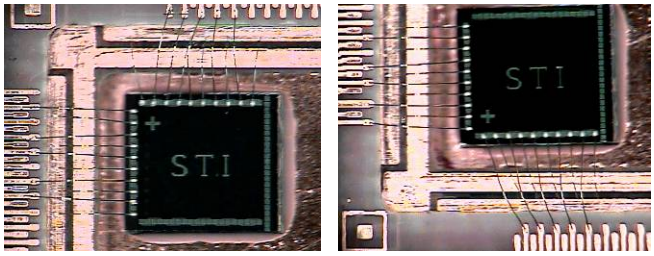

Figure 2. High-resolution images of daisy-chain die imbedded in the central cavity: upper left die (left) and lower left die (right).

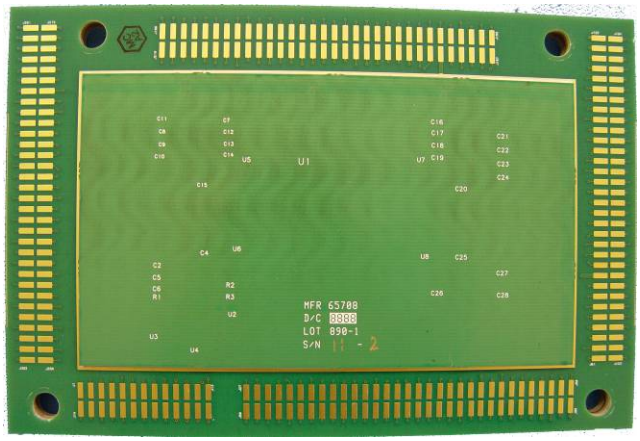

Figure 3. High-resolution image of the test coupon final assembly.

Material properties found on the technical data sheets were reviewed prior to selection of die attach, conformal coating, and encapsulant candidates to include in the test matrix. Materials were identified that minimize coefficient of thermal expansion (CTE) induced stress on the devices and interconnects and to reduce the thermal resistance between the die junctions and substrate/heat sink. Certain characteristics are desirable for all materials comprising the assembly. Materials with a glass transition temperature (Tg) outside the fielded environment range are desired in order to minimize thermomechanical stresses induced by a material's state change from glassy to rubbery. Die attaches, underfills, and encapsulants with low ionic contaminates are desired to minimize opportunities for corrosion in harsh environments. Thermal and electrical performance of the materials are equally as important in order to meet system-level performance requirements. Materials meeting the following specifications were selected to be included in the test matrix.

Critical Material Properties

- Cure temp – The type of cure (snap cure versus a step cure) and cure temperature affect the cured material properties including the glass transition temperature. The glass transition temperature should be significantly above the upper operating temperature range of the assembly to decrease expansion/CTE of the material over a wider temperature range [5].
- Material purity - Low ionic contaminants and alpha particles emitted will aid in increasing the reliability of the bare die. Industry recommends chloride (Cl-), sodium (Na+), potassium (K+), and fluorine (F-) levels of less than 5-10 ppm in order to decrease the opportunity of corrosion [6]. Industry recommends less than 0.001 particles/cm^2/hr in order to minimize irradiating particles found in encapsulants that can cause soft errors in logic and high-density memory devices such as DRAMs and SRAMS [7].
- Voiding – Voids, or air pockets, in the material result in increased localized stresses which can lead to premature delamination, or loss of adhesion to the die and/or substrate. The material is no longer an effective stress buffer with voids present, and the material's thermal resistance is increased due to air's poor ability to transfer heat.
- Moisture Absorption – Due to use of organic substrate materials, a hermetically sealed assembly cannot be achieved. Thus the materials selected should be hydrophobic or 'water repelling' in nature [8].
- One-part system – One-part materials are easily integrated into the manufacturing and assembly process. All components of the material (resin and curing agent) are premixed and eliminates handling by the operator to ensure product uniformity and quality. The material is supplied in a syringe for use on automated dispensing equipment and is typically stored at -40ºC to prevent changes in the material performance.

Thermal cycling fatigue or overstress failures are detected through alternating exposure of the assembly to extreme temperatures with short transition times between extremes. The test vehicle was placed in a thermal shock chamber to evaluate the resistance to temperature excursions of the

assembly materials and process parameters used to manufacture the test vehicle. The assembly was placed on a tray that transitions from a cold chamber to a hot chamber (air-to-air) within a specified time. Test conditions were changed periodically during the thermal shock test. Test conditions included: 1000 cycles from -55°C to 85°C, 250 cycles from -55°C to 125°C, 200 cycles from -55°C to 85°C, followed by 4200 cycles from -55°C to 125°C. The test vehicle was subjected to over 175 days of thermal shock cycling. Critical materials evaluated during this analysis included the following.

Critical Packaging Materials

- Die Attach Adhesive - determine effect of stress-related cracking of silicon die due to mismatch in CTE of die and laminate/copper core
- Conformal Coating – determine aging characteristics of Parylene after repeated exposure to extreme temperatures
- Encapsulant – determine warpage and stress due to modulus and CTE differential of encapsulant and assembly (silicon die, laminate substrate, metal core, aluminum wire bonds)

Continuity testing was performed prior to cycling to establish a baseline resistance for each of the daisy-chains and at periodic intervals to monitor resistance fluctuations. Five daisy-chain die were imbedded within the test coupon thus providing 30 daisy-chains, equivalent to 60 wires (120 bonds), for monitoring. A 3.0 Ω increase in resistance constituted a failure with the cycles-to-failure data noted in Table 1. The first failure/high resistance bond occurred after exposure to 3000 cycles with a lapse of 1500 cycles till the second noted failure. Only 23% of the wires had failed after 5500 cycles when the test coupon was pulled from cycling.

Table 1. Thermal shock failure data for the daisy-chain test vehicles with imbedded die.

Daisy-Chain Wire Group	Cycles	Wire Group	Cycles
1	3,057	16	none
2	4,507	17	none
3	4,507	18	none
4	4,947	19	none
5	5,102	20	none
6	5,656	21	none
7	5,656	22	none
8	none	23	none
9	none	24	none
10	none	25	none
11	none	26	none
12	none	27	none
13	none	28	none
14	none	29	none
15	none	30	none

The failure data gathered from this test vehicle is indicative that the material properties selected will provide the long-term reliability solution for critical military electronics hardware. Compliant die attach adhesive enables stress relief from thermal induced stress in the silicon die-to-substrate interface while the wire bonds, coupled with a compliant encapsulant, provide the stress relief from environmental induced stress (thermal movement, mechanical shock, and vibration). This material set for packaging electronics, in conjunction with the IC/DT® design guidelines, enables the manufacturing of robust, reliable electronics assemblies.

Test Vehicle 2

A mixed-signal test vehicle (Figure 4) was designed and assembled to serve as a technology demonstration for the Navy's Standard Missile-2 (SM-2) program. The Navy's SM Program Office used this prototype in a flight test to support a technology demonstration of the Imbedded Component/Die Technology, validating the electrical and mechanical performance of this new and innovative electronics-packaging concept. An IC/DT® prototype was designed with a mix of analog and RF circuitry using imbedded design practices with wire bondable devices. The prototype circuit design was selected to demonstrate the IC/DT® packaging technology's capability to address miniaturization, thermal dissipation, component obsolescence, and reliability.

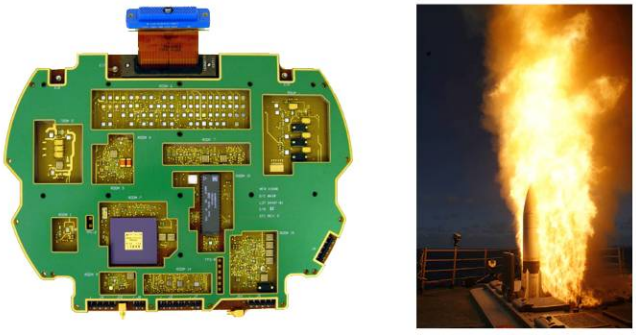

Figure 4. Mixed-signal prototype to demonstrate IC/DT® packaging technology's capabilities (*left*) and successful test flight of prototype on SM-2 missile (*right*).

Miniaturization objectives were largely achieved due to the ability to locate wire bondable components for the circuit. All ICs were procured as unpackaged components (wire bond face-up die), and passives with gold metallization were procured for imbedding into the prototype. Through elimination of the secondary packaging, a 66% reduction in surface area was achieved. This reduction enables the integration of future CCAs into a single assembly module (increased form, fit, and function through added capability within the same footprint).

All components, both actives and passives, were imbedded into cavities (Z-direction) in the laminate substrate. Multiple tiers were exposed in the substrate with strategic placement of components to decrease interconnect length

(component-to-component bonding and component-to-substrate bonding) and address power dissipation. High-power devices were bonded with thermally conductive adhesive directly to an imbedded thermal core in the substrate. This eliminates the need for external heat sinks and lowers the devices' junction temperature, thus increasing device performance and longevity [9].

Flexible interconnects (Figure 5), such as aluminum wire bonds, were used to electrically interconnect the devices (component-to-component for point-to-point) and circuit (component-to-substrate for multi-point nodes). These flexible interconnects are able to absorb the thermal and mechanical stresses created when operating in harsh environments such as temperature and vibration/shock thus increasing robustness of the assembly. Elimination of secondary packaging, which facilitates bonding from component-to-component, decreases the number of failure opportunities in the system thus increasing overall reliability.

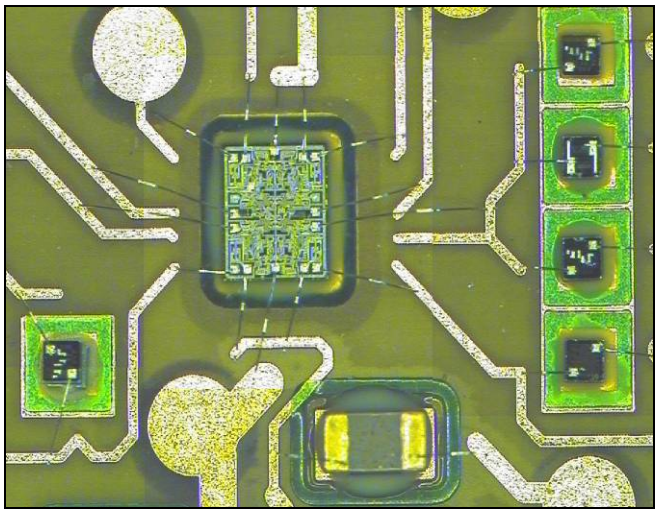

Figure 5. Wires bonded to electrically interconnect components on the prototype.

The IC/DT® prototype was analyzed and tested by SM-2 prime contractor Raytheon Missile Systems, which approved the prototype as flight hardware. This included finite element analysis (FEA) design modeling and prototype qualification testing per standard legacy performance requirements and overstress test requirements (extended temperature, humidity, vibration testing). In October 2007, the IC/DT® prototype's performance and robustness were demonstrated through a successful SM-2 flight test, thus advancing the IC/DT technology to TRL 8 status (TRL 8 Definition: Technology has been proven to work in its final form and under expected conditions. Examples include developmental test and evaluation of the system in its intended weapon system to determine if it meets design specifications. [10])

FUTURE DESIGNS

STI is currently designing four new layout concepts using IC/DT® that address SWAP – size weight and power reduction techniques that are suited for hi-reliability requirements. These designs utilize a number of different components and die that meet the requirement for the smallest form and fit factor devices available today. The idea is that one must utilize the smallest form and fit factor devices available in the market place today without their secondary packaging to be able to design the smallest form and fit factor circuit card assemblies. To that end, you will see below examples of bumped die and thin film passive devices that meet the overall system design objective size weight and power reduction. Integrating high density route out requires the use of imbedding interposer designed bumped die into a system card as seen in Figure 6.

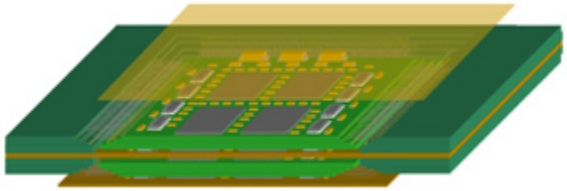

Figure 6. Bumped die, wire bonded die, and thin film passives integrated on a high density interposer imbedded within a system card.

The ability to minimize connector systems requires the ability to use rigid flex designs which allows one to fold up a system level card as seen in Figure 7. Integrating the smallest form factor parts available today is the design theme behind IC/DT and its ability to create the smallest system level electronic suite available.

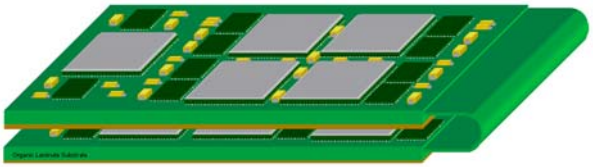

Figure 7. Bumped die, wire bonded die, and thin film passives integrated on rigid flex substrate to eliminate failure opportunities due to connector systems.

Today's designers now have a new design suite which provides them with the tools to design with SWAP as the objective and insure the end result meets environmental concerns, thermal management issues, size, weight and less power because they have the ability to model and simulate IC/DT® design guidelines while the individual PCB cards are being designed. The future of integrating microelectronics inside and alongside system level card designs is now available today. Today we hear about embedded passive and active devices by leading edge companies in Europe and Asia, and it is starting to filter into leading edge designs slowly. This is the infancy of a new design theory/technique which allows one to design microelectronics inside a standard FR4 organic laminate structure. IC/DT® is one of a few design techniques which is ready today to help shrink and make imbedding active

and passive devices a mainstream design guideline for future system level electronic suites.

CONCLUSION

The testing of the two test vehicles has demonstrated that Imbedded Component/Die Technology (IC/DT®) is a robust packaging technology for use in products that must operate in harsh environments [12]. The two test vehicles discussed in this paper have proven that the design guidelines, materials, and process parameters used to manufacture IC/DT® assemblies are capable of withstanding temperature, humidity, and shock stresses. Test Vehicle 1 (daisy-chain sample) survived over 3000 cycles of thermal shock exposure before a failure occurred. Test Vehicle 2 (mixed-signal prototype) was bench tested to meet and exceed legacy product performance specifications in order to qualify the prototypes as flight hardware. Lastly, a successfully flight test of the mixed-signal prototype in October of 2006 was paramount in demonstrating IC/DT's® ability to meet form, fit, and function requirements in a miniaturized robust package. *Originally published in the Proceedings of the SMTA International Conference, Orlando, Florida, August 17-21, 2008.*

Future designs requiring SWAP and hi-reliability requirements now have a design suite (IC/DT®) capable of meeting their requirements for future design objectives for lighter, smaller, and less power requirements. As shown earlier in technology prototypes, the test vehicles have proven their reliability characteristics by long term environmental testing as well as successfully being flown in actual systems. So the answer is "YES" to the question that IC/DT® is now ready for mainstream design engineering / applications.

ACKNOWLEDGEMENTS

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