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HIGH COMPLEXITY LEAD-FREE WAVE AND REWORK: THE EFFECTS OF MATERIAL, PROCESS AND BOARD DESIGN ON BARREL FILL

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ABSTRACT

The current "lead in solder" exemption for server and network infrastructure products in the European Union's RoHS legislation is currently scheduled to expire in 2014. Numerous studies have identified the interactions between wave solder process parameters and the various materials and chemistries currently in use. However, it is critical to confirm the capability of manufacturing large, high complex products in a lead-free environment, and to characterize the capability of existing equipment and material technologies. It is important to understand the factors which maximize hole-fill and more importantly identify gaps which may currently exist in order to allow time to address these challenges prior to the legislative deadline.

This paper focuses on the outcome of a development program which was designed to address the ability to maximize pin-through-hole solder joint quality and reliability performance for use in high complexity server/storage class hardware assemblies. Factors including alloy type, flux selection, surface finishes, atmosphere and wave nozzle configurations are studied. This program utilized both an internally designed test vehicle (TV), in addition to a product vehicle (PV). Actual product design points and connector technologies were integrated into the test vehicle design, in order to represent real-life design features throughout the experiment. In addition, various design features such as, pin-to-hole ratio, ground layer connections and thermal relief designs were incorporated into the test vehicle design, to understand the impact of board design on final barrel fill results and provide a data set to support any design for manufacturing (DFM) change recommendations.

Key words: High Complexity, Wave Solder, Rework, Lead Free, Barrel Fill, Design for Manufacturing

INTRODUCTION

To date, through the transition to lead-free assembly, successes have been made in terms of the ability to wave solder through-hole connections onto products which are in the low to medium complexity realm (Table 1). These successes have come through process optimization, wave nozzle improvements and flux chemistry evolutions made within the industry [1, 2]. In addition, challenges associated with reworking pin-through-hole (PTH) connectors on these product types have been addressed primarily through the use of alternative lead-free alloys, which exhibit lower copper dissolution rates compared to the commonly used Sn-Ag-Cu alloys (i.e. SAC305/405) [3, 4]. Future challenges with both the wave solder and PTH rework process are associated with the conversion of larger thermally challenging product types, such as server, industrial and telecommunication products. With the RoHS 2014 lead in solder for server exemption 7b approaching, it is critical to confirm the capability of manufacturing these larger, high complex products in lead-free, as well as realizing any gaps which may exist in order to be able to address them in time. This study was primarily designed to maximize PTH solder joint quality/reliability and primarily focused on factors affecting barrel fill analysis throughout.

Table 1. PCB Complexity Definition Chart

Characteristics	Low Complexity	Mid Complexity	High Complexity
Board Size (L x W)	Not a factor		
Thickness	< 0.093"	0.093" – 0.120"	≥ 0.120"
Total Layers	2 - 6	8 - 14	14 – 24
Total Ground Layers	0 - 2	3 - 6	7 - 12
Total Cu Weight	0 – 4 oz	5 – 9 oz	10 - 24 oz

OBJECTIVES

The main objectives of this multi-phased project were as follows:

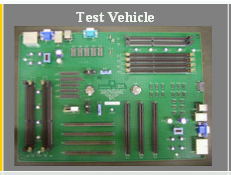
1. Through a Design of Experiment (DoE), study the impact of various lead-free wave solder alloys, flux chemistries, process elements and wave nozzle/atmosphere configurations on barrel fill.
2. Perform TV and PV validation builds to evaluate the capability of assembling a high complexity product type using optimal material/process and equipment settings obtained from the DoE analysis.
3. Study the challenges associated with reworking a high complexity, thermally challenging PCBA.
4. Understand the limitations of current design for manufacturing guidelines for PTH lead-free barrel fill,

and offer recommendations on amendments based on the results from this study.

TEST VEHICLE AND PRODUCT VEHICLE

The test vehicle was used as the main method of gathering data relating to the optimization of the wave solder process. In addition, it included certain Design for Manufacturing (DFM) elements, such as pin-to-hole ratio designs, ground layer/thermal relief design and pallet opening features among others which are further described in Design for Manufacturing Features Section of this paper. The connector technologies selected for the TV were based on commonly used connector types assembled on current server products. This allowed for an immediate transfer of knowledge of the lessons learned from this development activity directly to similar products which were transitioning to lead-free. The product vehicle used during this experiment was selected after researching a number of server products which fell into the category defined as "high complexity" within this program. The reason for including a PV in this study was to prove out the manufacturability of an actual representative "high complexity/thermal mass" product as well as to understand any remaining lead-free gaps, which may require additional development efforts to insure a smooth transition from tin lead assembly to lead-free. The PV assembly included PTH connector wave solder assembly but did not include any SMT component population, in-circuit test, or functional card testing.

Table 2. Test and Product Vehicle Characteristics

Test / Product Vehicle Characteristics	Test Vehicle 	Product Vehicle 
Board thickness	0.120"	0.096"
Dimension	11.0" x 16.0"	9.8" x 16.0"
Number of layers	20 layers	16 layers
Total Cu Weight	12oz	10oz
Surface Finish	HTOSP, ImmAg, LF HASL	HTOSP

DESIGN FOR MANUFACTURING FEATURES

In order to gather statistical data to support the impact of specific design features on aiding or impeding barrel fill, a series of DFM board features were included in the test vehicle design (Figure 1).

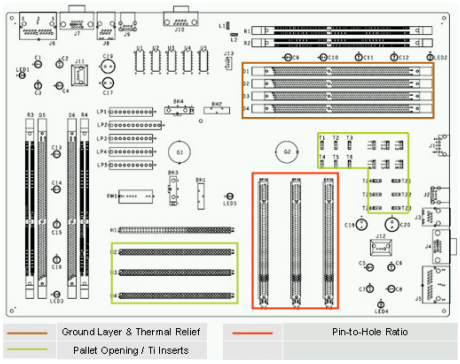


Figure 1. Pipeline Design for Manufacturing Board Features

Quantity of Ground Planes and Thermal Relief Design

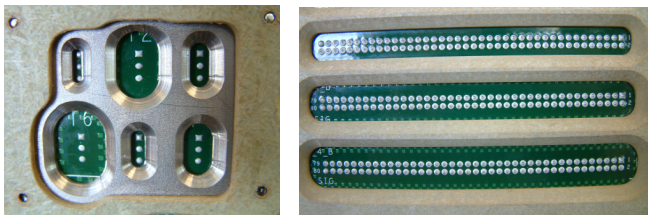
In order to quantify the impact of various ground connections, stack-up and thermal relief design variations on the ability to achieve barrel fill, a variety of designs were incorporated into the footprints of the four DIMM connectors on the board. In total, a combination of four different ground connections ranging from 4oz to 12oz total copper weight and four varying thermal relief designs were included. This thermal DoE was incorporated into each DIMM connector using standard grounding design practices to represent a typical DIMM design. Pin diameter was constant at 12mils, with a finished hole size (FHS) of 28mils.

Pin-to-Hole Ratio

In order to study the impact of pin-to-hole (P2H) ratio on barrel fill, a design of experiment was incorporated into the TV design using the PCI connectors. In total, six varying pin to copper wall spacing's were studied, ranging from 0.005" minimum to 0.030" maximum. There were a total of 36 pins per level included to study P2H ratio (12 pins per connector x 3 connectors). The PCI connector had 0.0098"x0.015" rectangular pins with the 0.018" diagonal dimension used to calculate P2H ratio. In order to remove second order interactions, all pins were designed with no ground connection.

Pallet Opening, Titanium Inserts and Orientation

A selective pallet was designed and made from epoxy resin material, and incorporated various opening sizes to study the impact on barrel fill. There were two locations which were designed to specifically measure the impact of pallet openings, the 1x3 and 2x40 pin header locations shown in Figure 2. Titanium inserts were incorporated into the 1x3 header designs also to understand the benefits on barrel fill. The rest of the pallet openings were designed based on current spacing design guidelines.



(a) **(b)**

Figure 2. Pallet Spacing Design **(a)** 1x3 Headers, **(b)** 2x40 Headers

The design of experiment using the 1x3 and 2x40 headers is shown in Table 3 and 4 respectively. A total of 6 varying copper-to-copper spacing levels from 0.050" to 0.300", were studied using the 1x3 pin headers and three levels were studied using the 2x40 header. The current lead-free DFM guideline recommends having at least 0.250" spacing. In addition to pallet opening size variations, the impact of connector orientation was studied. The barrels in this design were not grounded.

Table 3. 1x3 Pin Header Pallet Opening Design of Experiment

Levels	Levels					
	1	2	3	4	5	6
Cu-to-Cu Spacing (Wall-Cu Spacing)	0.050 (0.010)	0.100 (0.030)	0.150 (0.050)	0.200 (0.094)	0.250 (0.144)	0.300 (0.194)
Orientation	Parallel to Wave			Perpendicular to Wave		
Titanium Inserts	YES			NO		

Dimensions in inches

Table 4. 2x40 Pin Header Pallet Opening Design of Experiment

Levels	Pallet Wall to Annular Ring	Wall Thickness	Pallet Wall to SMT Pad	Cu-to-Cu Spacing
1	0.094	0.076	0.030	0.200
2	0.144	0.076	0.030	0.250
3	0.194	0.076	0.030	0.300

Dimensions in inches

INSPECTION STRATEGY

As the TV was designed with both "standard" and "DFM" features, the inspection strategy was divided into these two groups. The standard features on the board incorporated current design guidelines and the DFM features consisted of variations from the current recommendations, in order to validate these guidelines for lead-free soldering. For the purpose of studying and comparing the quality performance of each of the alternative alloys tested and board surface finish used within the validation builds 100% of the "standard" barrels were inspected and used in the statistical analysis.

An x-ray laminography inspection machine was used to measure the barrel fill percentage after assembly and rework. Two programs were created to support the statistical analysis of both the Design of Experiment (DoE) phase and Validation builds (Figure 3). A 5-slice program was used to analyze the DoE phase, taking measurements at 0%, 25%, 50%, 75% and 100%. This allowed for inspection of each barrel to be made based on a 50% (ground pins) and 75% (power/signal pins) pass/fail level, as per IPC-610D, Class 2 (Figure 3a) [5]. In order to obtain more granularity in the results to distinguish between the various factors studied, a 10-slice program was developed and all boards assembled during the validation phases were inspected using this program (Figure 3b).

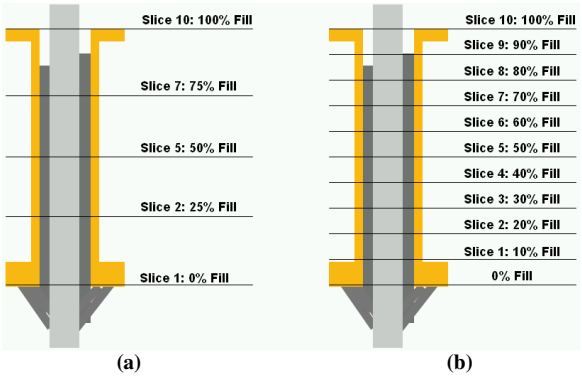


Figure 3. (a) X-Ray Program #1 for DoE Phase, **(b)** X-Ray Program #2 for Validation Phase

DESIGN OF EXPERIMENT

The intent of this phase of the study was to understand the individual effects each of the various factors included had on barrel fill (Table 5). The lessons learned from the DoE were applied to the validation builds. The intent was to establish that the capability of assembling a high thermally complex server type product exists inside current process parameters.

Table 5. Factors Studied within Design of Experiment

Factors	Levels		
Alloy	SAC405	Alloy A	
Flux (VOC)	VOC1	VOC2	
Flux (VOC-free)	VOCFree1	VOCFree2	
Flux (Water Wash)	WW1		
SMT to Wave Time (hrs)	24	72	
Surface Finish	HTOSP	ImmAg	LF HASL
Nozzle / Atmosphere	Lambda / Air	Lambda / N2 Hood	Wide Chip / N2 Hood

RESULTS: DESIGN OF EXPERIMENT

This study had a phased approach which included a full factorial DoE and a series of validation builds using the output from the DoE as guidance. This approach allowed the use of the same test vehicle to make broad comparisons between process materials and also allowed for more detailed analysis into the effects of board and fixture design. The following sections outline the statistical analysis methods used and results from the full factorial DoE.

Statistical Analysis Methodology

The primary design variables for the DoE are factorial in nature. The factors, "flux", "alloy", "waveform & atmosphere", "surface finish" and "delay from SMT" all exist in discrete levels rather than as continuous variables. This structure in the data requires the use of a specific statistical tool. Binary Logistic Regression (BLR), the tool of choice was developed to analyze the effect of embedded factors in large populations on the probability of a selected event [6]. In this case the event or response under study was success in filling the PTH hole to the IPC-610D, Class II criteria.

One efficient way to review the various levels of a single factor in a model is to use the "Odds Ratio". The reference level of all factors is embedded in a single constant and the relative difference of the other levels is generated by the software as an "Odds Ratio". If the level under study is not significant, then the 95% confidence interval for the odds ratio will contain "1". In general factors that do not contain at least one significant level were removed from the model and results compared. The goal was to produce the simplest model that defined all of the significant correlations in the data. Odds Ratios can be considered in much the same way that primary effects are. However, there is no strict equivalent to the "interaction effects" and for that reason several different sample sizes were selected and individual factors and the "Odds Ratios" associated with them were assessed to infer the interaction effects (Table 6).

Table 6. Samples Size Lots Selected for BLR Statistical Analysis

Samples	Number / Name	Size (N)	Description
1	All Pins	250,000	**All barrels** DFM or STD
2	All Standard (STD) pins	149,000	**Signal pins** that meet **DFM guideline** for pin to hole ratio. **Ground pins** that meet the **DFM guideline** for copper connection
3	Exclude WW1 Flux	119,000	All STD pins soldered with **no-clean** flux
4	VOC1 & VOC2	59,000	All STD pins soldered with **alcohol based** no-clean fluxes.

Analysis of Alloy

The SAC405 alloy exhibited a marked benefit in Samples 1 & 2 where the whole range of flux activity was present (Figure 4). The removal of the most active flux (WW1) reduced the benefit of the alloy. The separation of the water based fluxes from the alcohol based no-clean fluxes shows that the negative effect is dominant in one and not present in the other. In this data matrix Alloy A performed better than SAC405 when alcohol based fluxes were used.

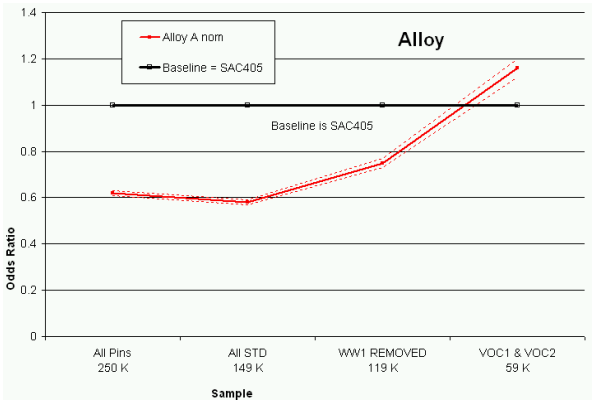


Figure 4. Odd Ratio Analysis: Alloy

Analysis of Flux Chemistry

Flux Chemistry exhibited very strong differences between individual levels in the data but the actual Odd Ratios do not change significantly over the various samples (Figure 5). The effect of flux activity represented by the selected fluxes was very consistent generating roughly parallel lines in the graphic. Flux activity remains one of the primary levers for hole fill improvement, generating consistent improvement across the wide variety of other factors, especially water wash flux.

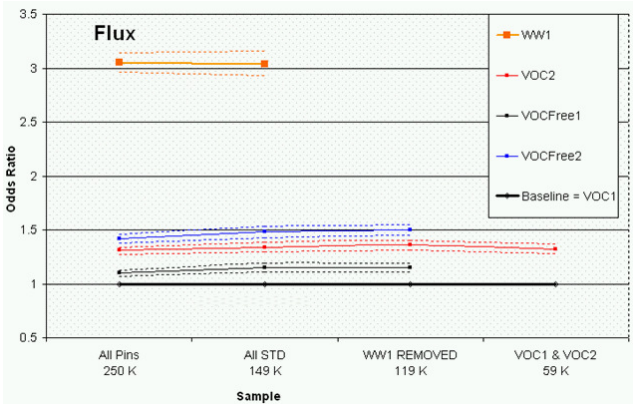


Figure 5. Odd Ratio Analysis: Flux Chemistry

Analysis of Waveform Nozzle and Atmosphere

Three levels of this factor were built into the DoE:

- Lambda wave form in standard atmosphere (Air)
- Lambda wave form with Nitrogen Hood
- Wide Chip nozzle with Nitrogen Hood

In this data set the two levels that include nitrogen under a closed hood were significantly better than the level in air and they were not significantly different from each other (Figure 6). There was overlap in the 95% confidence intervals in all samples except 1 and the nominal values of the Odd Ratios cross over as the activity of the fluxes decreased. Once again there is a noticeable difference between Sample 4 and 5. The effect of nitrogen was more pronounced when used with water based fluxes.

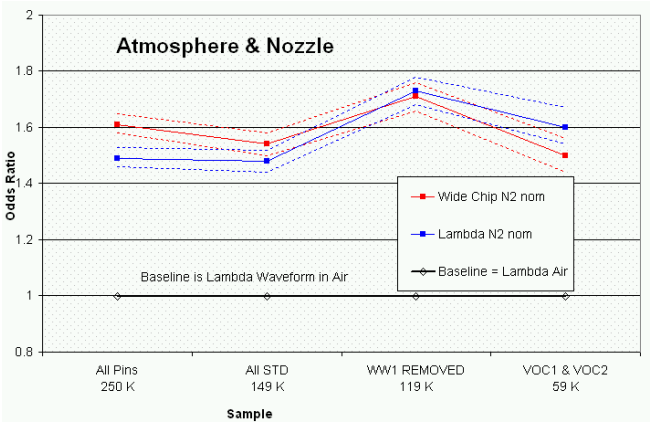


Figure 6. Odd Ratio Analysis: Atmosphere & Nozzle

Analysis of Surface Finish

There was a significant difference between HTOSP and both Immersion Silver (ImmAg) and LF HASL but the difference between HASL and ImmAg was indistinguishable (Figure 7). Note that the very strong benefit seen in the larger sample sizes was once again driven by the water based fluxes.

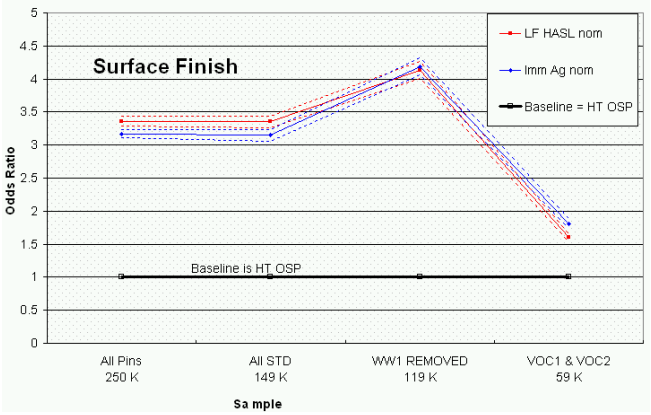


Figure 7. Odd Ratio Analysis: Surface Finish

RESULTS: TEST VEHICLE VALIDATION BUILD

Based on the results of the DoE, the following factors were selected to be used during the TV validation assembly builds. The builds were conducted in various locations

using production machines and so there was some accommodation for existing conditions. Optimum process parameters from the preceding DoE work were communicated but minor differences in set up are to be assumed. The SAC305 alloy was resident and therefore used for the SAC baseline alloy leg of the build. A separate location assembled two alternative alloys A & B. All boards were wave soldered using a Wide Chip nozzle only under a nitrogen inerting hood using the VOC1 flux, which was the flux used at Location A. The sample sizes and the factors used in each build are summarized in Table 7.

Table 7. Test Vehicle Validation Build Sample Size and Factors

Factors	Location A	Location B	
Board Sample Size	9 HTOSP	20 HTOSP 10 ImmAg 10 LF HASL	19 HTOSP
Alloy	SAC305	Alloy A	Alloy B
Flux	VOC1	VOC1	VOC1
Precondition Time (2X)	24hrs	24hrs	24hrs
Wave Configuration	Wide Chip + N2 Hood	Wide Chip + N2 Hood	Wide Chip + N2 Hood

DoE Statistical Analysis Methodology

As discussed, the TV validation phase consisted of larger lots of specific combinations. This phase was intended to confirm the findings from the DoE and provide a more consistent base matrix over which evaluation of specific PCB design features might be more informative. In order to calculate yield, the analysis within this Validation Section included only "Standard" barrel features, and not any of the DFM features which challenged the limits of design. The standard vs. DFM barrels were defined using current IPC-2222 specifications for copper ground connections and current standards for finished hole size.

The standard pin sample sizes of the various alloy/surface finish combinations built were tabulated below (Table 8). The full matrix was not built but there are full sets of samples to compare across reasonable sample sizes. When making comparisons between alloys, the HTOSP surface finish sub-lot was used and when making comparisons against surface finishes, the Alloy A sub-lot was used.

Table 8. Sample Size for TV Validation Build Analysis, Standard Pins

	HTOSP	HASL	ImmAg	ALL
SAC305	14499	0	0	14499
Alloy A	32220	16110	16110	64440
Alloy B	30609	0	0	30609
ALL	77328	16110	16110	109548

Yield Analysis

Wave solder yields were calculated by connector type, breaking down the yield results by alloy and signal/ground connections (Table 9). Yields were calculated based on the IPC-610, Class 2 specification, which states barrels attached to ground must have 50% barrel fill and signal pins require 75% solder fill to represent a pass. The yield results varied based on the connector type, with results as low as 2.5% on the 2-pin Gold Capacitors, largely due to an undersized finished hole size. The larger I/O connectors such as the DIMM and PCI connectors had yields ranging from 98.3% - 100%. Further discussions on yield results of each connector type are included in the following sections. With respect to the alloy performance, overall Alloy B performed the best in terms of yield, at 99.7%, with SAC305 second at 99.3% and Alloy A trailing at 98.7%.

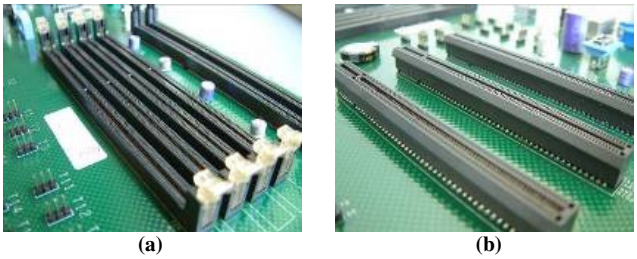
Table 9. TV Yield by Alloy, GND/SIG & Connector Type using IPC Standard Pins

Connector Type		SAC305		Alloy A		Alloy B	
Name	Code	GND	SIG	GND	SIG	GND	SIG
DIMM	D	98.7%	99.9%	94.7%	100.0%	98.7%	100.0%
PCI	P	NC	100.0%	NC	98.3%	NC	99.9%
E-Caps	C	-	75%	No Pop.			
Gold Caps	G	-	83.3%	-	2.5%	-	39.5%
LEDs	LED	-	75.6%	No Pop.			
Power Module	PM	-	100.0%	No Pop.			
PDIP	U	NC	100.0%	NC	94.3%	NC	99.2%
Edge Connectors	J	-	100.0%	-	99.6%	-	99.9%
Battery Holders	B	-	-	-	-	-	-
Total		98.7%	99.4%	94.7%	99.1%	98.7%	99.7%
Grand Total		99.3%		98.7%		99.7%	

NC: Not connected to ground ; - : Pins which violated IPC-2222, Section 9.1.2

DIMM and PCI Connectors

The DIMM (Figure 8a) and PCI (Figure 8b) connectors were further analyzed by reference designator and thermal relief designs to understand which factor(s) may have influenced final yield results.



(a) (b)

Figure 8. (a) DIMM D1-D4, **(b)** PCI Connectors

From Figure 9, it can be observed that the D5 connector experienced higher levels of barrel fill defects compared to all other DIMM connectors. The main reason for this was based on the fact that D5 was on the leading edge of the test vehicle (i.e. it came into contact with the wave first). The other DIMM connectors (situated on the trailing edge), each had the benefit of experiencing preheat conducted through the ground planes prior to being soldered. The entrance effect was also observed when analyzing the results by thermal relief design. Across each connector, the 4-spoke, 0.005" width design consistently had the worst barrel fill results. On the D1-D4 connectors, running perpendicular to the wave, this thermal relief design came into contact with the wave first (Figure 10). Finally, when analyzing the impact of quantity of thermal ground connections, it was interesting to see that the barrel fill results were not directly proportional to the increase in the "quantity" of layers. The 6-layer connection (D2) performed worse than the barrels connected to 8-layers of ground (D3). Both D2 and D3 connectors were connected to a total of 8 ounces of copper, however the stack-up for the 6-layer connection was situated on the upper half of the barrel. This indicated that the

presence of ground connections, on the lower half of the barrel, may have aided in providing heat to the barrel, improving the flow of solder during initial contact. The lack of bottom ground planes in the 6-layer barrels reduced the ability to conduct heat inside the board.

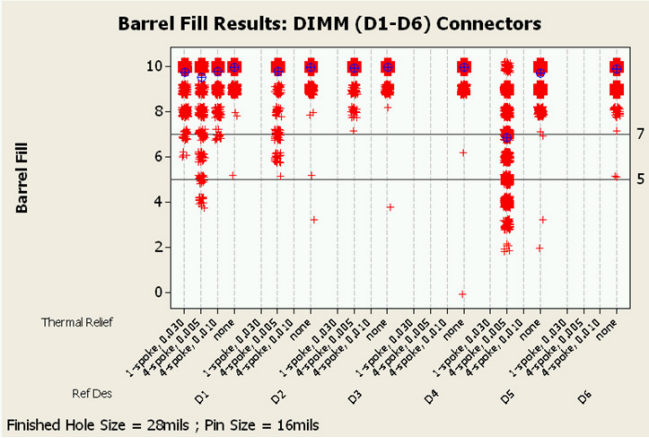


Figure 9. DIMM Connector Barrel Fill Results by Thermal Ground Connections

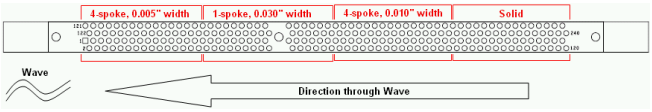
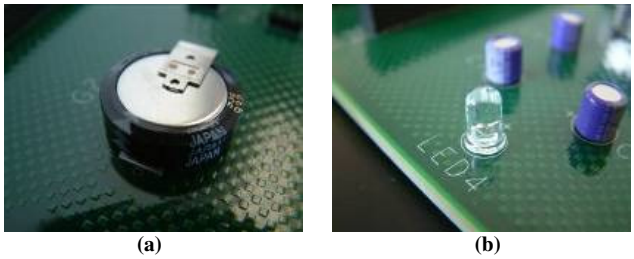


Figure 10. DIMM (D1-D4) Thermal Relief Designs and Direction Through Wave

The PCI connector was assembled with what is currently a standard finished hole size of 28mils (similar to the DIMM connector). However, in the case of the PCI connector, the lead size was slightly larger (18mils). This resulted in a minimum total clearance of 10mils. This amount of clearance was not sufficient and contributed to a high degree of barrel fill related defects.

E-Cap, Gold Caps, LEDs, Power Modules

Low I/O connectors were further analyzed by reference designator to understand which factor(s) may have influenced final yield results.



(a) **(b)**

Figure 11. (a) Gold Capacitors, **(b)** LED and E-Caps

On smaller I/O devices, such as e-caps, gold-caps, LEDs and 3-pin headers, a similar phenomenon was observed. In all cases, a slight improvement in hole fill was noticed in parts which were placed near larger I/O DIMM connectors which were connected to ground layers. It is suspected that the ground plane connections to the DIMMs, may have acted to conduct heat through to these lower I/O devices in turn aiding hole fill. This phenomenon is shown for the LED connector example in Figures 12-13.

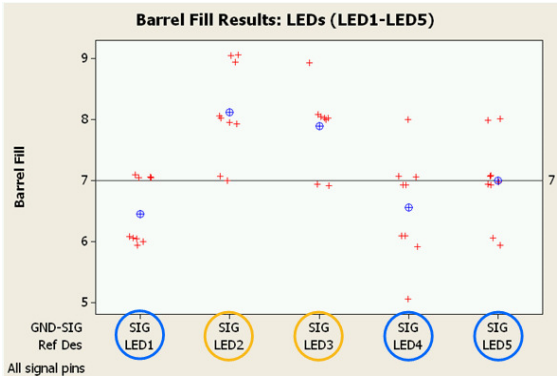


Figure 12. LED Barrel Fill Results by Reference Designator

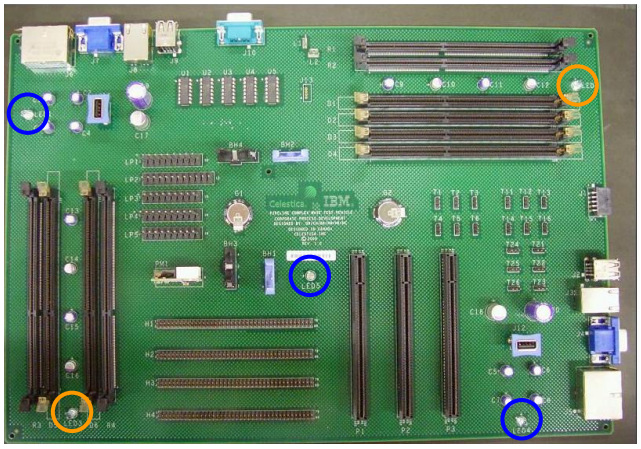


Figure 13. Internal Plane Heating Effect on Location of LEDs near DIMM Connectors

Impact of Alloy and Surface Finish

When analyzing the difference in performance between the various alloys and surface finishes tested, each was shown to have only a marginal impact on barrel fill results (Figure 14 and 15 respectively).

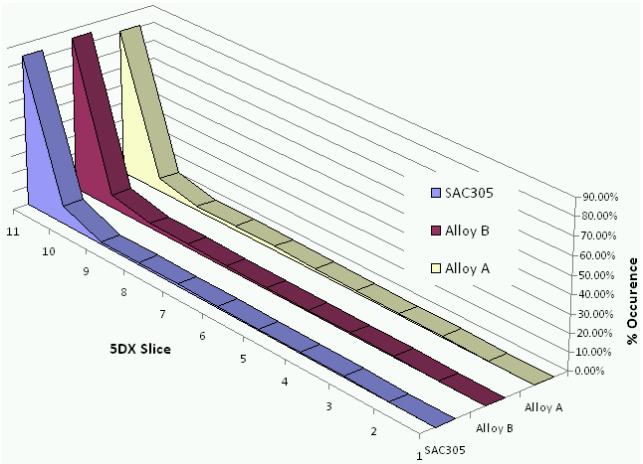


Figure 14. Occurrence of Barrel Fill Percentage by Alloy Type

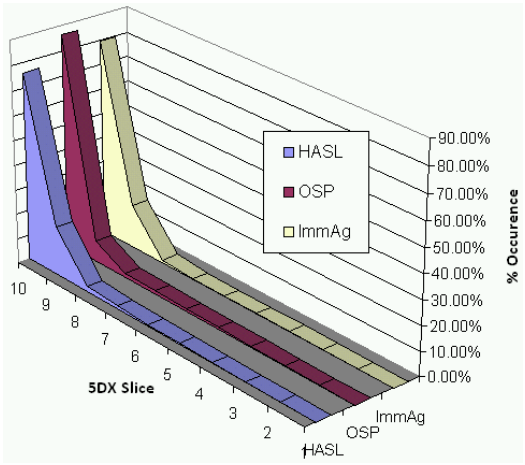


Figure 15. Occurrence of Barrel Fill Percentage by Surface Finish

RESULTS: PRODUCT VEHICLE VALIDATION BUILD

After the completion and analysis of the DoE and TV validation build, a final PV validation build was performed using the knowledge gained from previous phases. A total of 28 boards were assembled under the following final optimized conditions (Table 10). Similar to the TV build, Alloy A was used as the primary attach alloy. However, a change was made in the flux chemistry used and nozzle configuration. The data from the DoE indicated that the VOC2 flux provided the best performance out of the VOC containing fluxes and the impact of the Wide Chip nozzle on improving barrel fill in the case of the TV build was marginal. The strongest factor contributing to improving barrel fill was the existence of the N2 Hood. Therefore, the Lambda wave + N2 hood was used to validate the capability of using this standard nozzle type. All product vehicles had an HTOSP surface finish.

Table 10. Factors used during Product Validation Build

Factors	Prowl – Product Vehicle
Build Sample Size	28
Alloy	Alloy A
Flux	VOC2
SMT to Wave Time (hrs)	24
Surface Finish	HTOSP
Nozzle / Atmosphere	Lambda / N2 Hood

Yield Analysis

Overall yield for the PV was very similar to the TV validation build. There were specific issues that existed in both cases. The pin to hole clearance on pin 1 of the battery holder was very small relative to the other pins (Table 11). This pin was very difficult to fill and caused all of the low solder fill barrels on this connector. There was also a minor occurrence of low solder or low grey level on the headers which were much smaller than those that were present on the TV. The edge connectors presented a very interesting situation. The validation build on the TV was processed over the Wide Chip nozzle while the PV build used the Lambda wave configuration. The yield on the signal pins was reduced from 99.3% to 98.6% but the yield on the power and ground pins is increased and fill defects were eliminated.

Table 11. PV Yield by GND/SIG & Connector Type using IPC STD Pins

Connectors	Yield PWR/GND	Yield Signal Pins
Battery Holder	71%	100%
Edge Connector	100%	98.6%
Headers	99.8%	99.9%
USB Connector	100%	100%
Total	**98.3%**	**99.1%**
Grand Total	**98.8%**	

DESIGN FOR MANUFACTURING

The following section includes the analysis performed on the design for manufacturing features included in the test vehicle design. The DFM statistical analysis was based on the barrel fill results from the TV validation boards assembled (Table 12). Samples from the validation process lots allowed for the evaluation of both the interaction of FHS with surface finish in Alloy A assembly as well as the interaction of FHS with alloy in HTOSP lots.

Table 12. Board Sample Size for DFM Analysis

Alloy	SAC305	Alloy A	Alloy B
Board Sample Size	9 HTOSP	20 HTOSP 10 ImmAg 10 LF HASL	19 HTOSP

Quantity of Ground Planes & Thermal Relief Design

The "ground plane" and "thermal relief" experiment was embedded in the DIMM connector array (D1 – D4). The four DIMM connectors were divided into quadrants which incorporated variations in thermal relief design patterns (Table 13) and ground plane connections (Table 14). These patterns were applied to the ground pins in groups that were one fourth of the connector sequentially from the leading end to the trailing end. This spatial arrangement means that the entrance effect normal in this type of connector always occurred in condition A (Figure 16). The ground plane connections ranged from 4 layers to 10 layers. They each existed in only one of the connectors. The central two layers (10, 11) were two ounce and category 2 is not evenly distributed through the board.

Table 13. Thermal Relief Pattern Designs

Thermal Relief Patterns	
A	4 spoke, 0.005 inch wide
B	1 spoke, 0.030 inch wide
C	4 spoke, 0.010 inch wide
D	Solid connection

Table 14. Ground Connection Designs

Thermal Relief Patterns	
1	4 layer / 4 oz, layers 2, 8, 13, 19 (evenly distributed near the top and bottom)
2	6 layer / 8 oz, layers 2, 4, 6, 8, 10, 11 (all in the top 60% of the board)
3	8 layer / 8 oz, layers 2, 4, 6, 8, 13, 15, 17, 19 (all 1 oz layers evenly distributed)
4	10 layer / 12 oz, layers 2,4, 6, 8, 10, 11, 13, 15, 17, 19 (all layers)

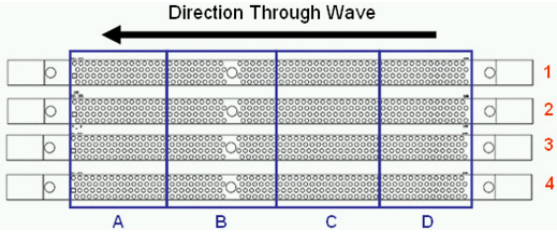


Figure 16. DIMM Connectors (D1-D4) Ground/Thermal Relief Design and Direction Through Wave

The thermal relief design categories in rank order from best performing to worst performing were: B > C > A > D (Figure 17). The obvious divergence from direct correlation to copper area is the A category which was affected in all cases by its spatial relationship which included the entrance effect of leading into the wave.

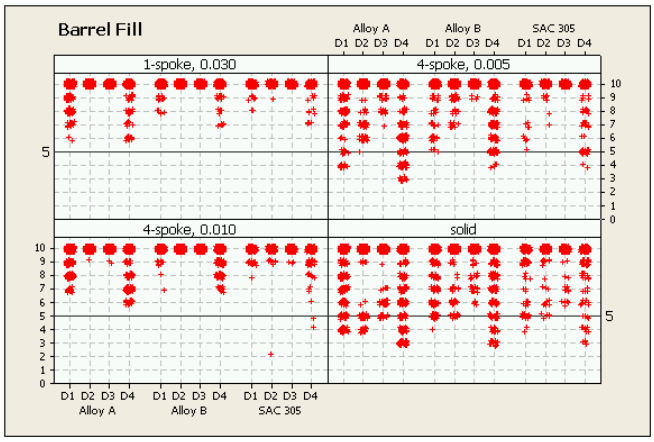


Figure 17. Impact of Number of Thermal Relief Design across Alloy Types

The ground connection categories in rank order from best performing to worst performing were: 3 > 2 > 1 > 4 (Figure 18). This suggests that moderate connection to internal copper is in fact helpful in transferring heat into the barrels and preventing nucleation of the solder. The relative strength of the effect driven by the two factors, thermal relief and multiple copper connections appear to be very similar.

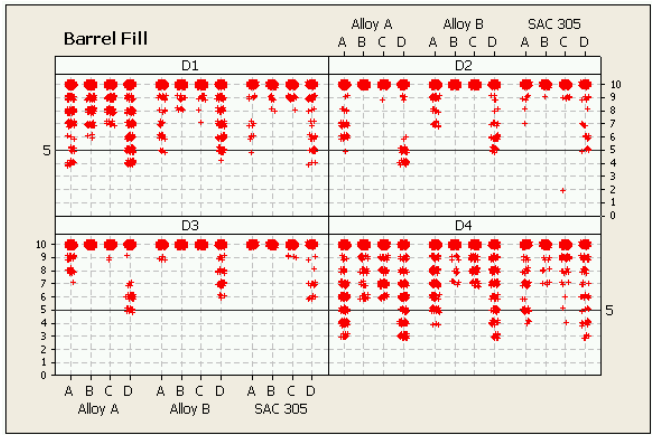


Figure 18. Impact of Number of Ground Connections across Alloy Types

Pin-to-Hole Ratio

The sample size of the barrels analyzed within the PCI connectors is shown in Table 15. The PCI connector had a diagonal pin dimension of 0.018". The FHS dimensions were 0.023", 0.028", 0.033", 0.038", 0.043" and 0.048". The resulting combinations are commonly referred to as Pin +5, through Pin +30.

Table 15. PCI Connector Sample Size for FHS Analysis

	HASL	ImmAg	OSP	All
SAC305	0	0	5400	
Alloy B	0	0	11400	
Alloy A	6000	6000	12000	24000
All			28800	

The correlation to FHS is unmistakable. Figure 19, clearly demonstrates that both the Pin +5 (0.023" FHS) and the Pin+10 (0.028" FHS) configurations generated significant unfilled portions in all three samples, while the Pin +15 (0.033" FHS) and larger configurations perform much better. There were some minor issues with the 0.048" FHS barrels that relates to their spatial location at the outboard end of both the connectors and whole assembly but the two smallest FHS categories contributed to almost 100% of sub 70% hole fill condition.

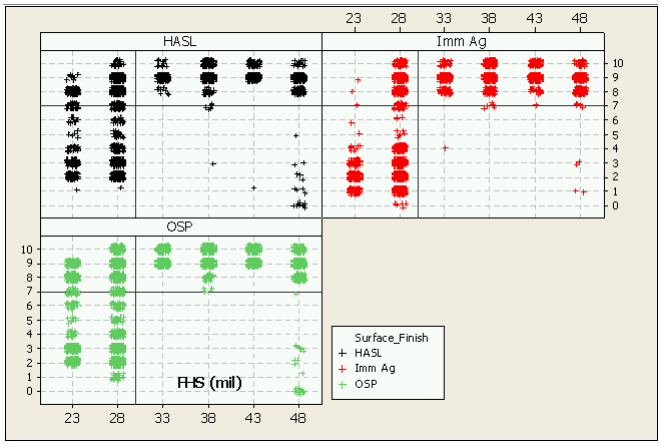


Figure 19. Distribution of Barrel Fill Across Various Surface Finish and FHS Dimensions

Pallet Opening

There were two wave solder pallet opening experiments, the first was embedded in the 80-pin 2x40 pin header connectors (Figure 20), the second utilized the 1x3 pin headers (Figure 22). There were three pallet openings within the 2x40 pin headers, (0.094, 0.144 and 0.194"). The opening sizes refer to the distance in inches from the pin to the pallet wall all around the connector. The corresponding copper-to-copper spacing was 0.200, 0.250 and 0.300", assuming a standard minimum pallet wall thickness of 0.076" and a pallet wall to theoretical shielded SMT component distance of 0.030". Comparisons were made across surface finish lots built with Alloy A and alloy lots built on HTOSP surface finish.

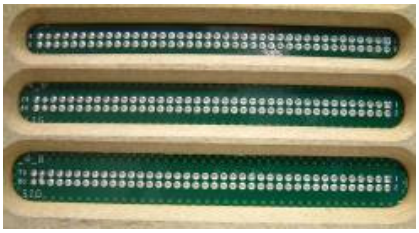


Figure 20. 2x40 Header Pallet Openings

These connectors were in the preferred orientation to the solder wave and have large pins which help with heat conduction. There were entrance and exit conditions evident in every lot. The lack of heat transfer from pin to pin down the connector was an important factor that was not present at the entrance to the wave and pressure changes at the exit from the wave creates some similar issues. The HTOSP surface finish exhibited the strongest entrance effect across all three finishes. Among the alloys Alloy A exhibited the strongest effect followed by Alloy B and then by SAC305 (Figure 21). It is evident that expanding the pallet to pin spacing to 0.300" was not a benefit in this case. It was less clear whether the 0.200" spacing was a benefit. It would appear that in these large pin connectors 0.100" spacing was sufficient for the side clearance but more end clearance might be helpful.

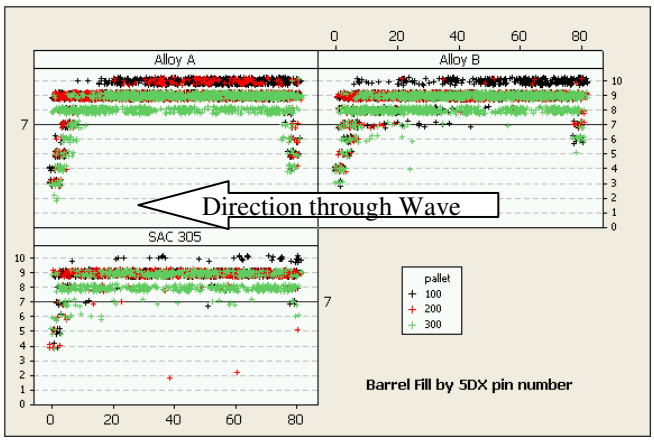


Figure 21. Barrel Fill Results by Pallet Opening and Alloy Type on 2x40 pin Headers

The 1x3 header experiment included six pallet openings in groups of three, and each group was defined by orientation to the wave solder direction and presence of a titanium insert (Figure 22). The copper-to-copper spacing's studied were 0.050", 0.100", 0.150", 0.200", 0.250" and 0.300".

A. Parallel to wave solder (Parallel)
B. Perpendicular to wave solder (Perp) – Note: This is the normal preferred option
C. Perpendicular to wave solder with a titanium insert (Perp Ti)

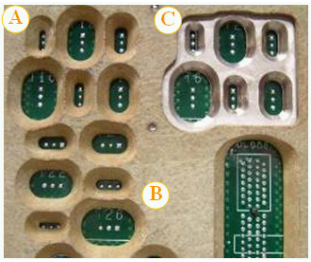


Figure 22. 1x3 Header Pallet Openings

As expected, the perpendicular pin headers with the Titanium inserts were always the best performer and parallel to the wave was always the worst performer. However, the differences were small and there were significant portions of low fill in all of the lots (Figure 23). This was in part due to the aspect ratio of the pallet openings. Even the very narrow openings were not significantly longer than wide. From observations made, there may be some alignment issues with the smallest openings which are in conflict with the tolerances of pallet registration. This was one detriment of having a pallet opening accommodating a copper-to-copper spacing as small as 0.050".

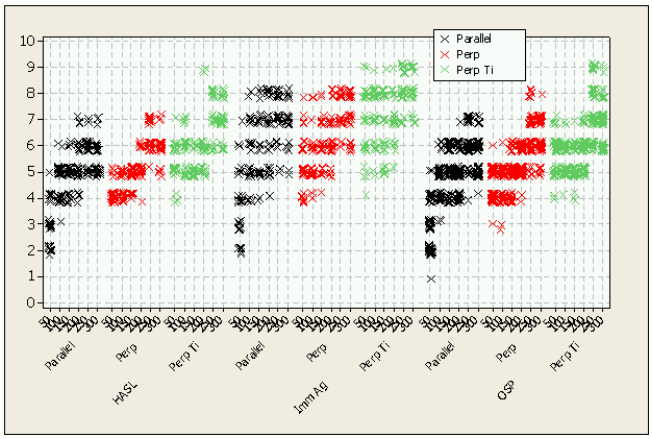


Figure 23. Pallet Spacing Results by Orientation, Ti Inserts and Surface Finish

FORCED REWORK

The study included forced rework operations of the 240 I/O DIMM (D3) and 31 I/O Ethernet (J6) connectors using Alloy A (Figure 24). A design of experiment was established to determine the impact of varying solder pot temperatures and solder contact times. The intent of this study was to validate the ability of 1X reworking a typical connector using current solder fountain equipment, chemicals and alloys available on the market.

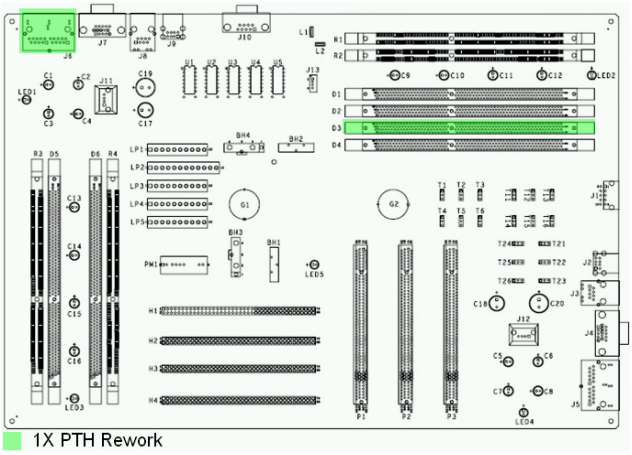


Figure 24. PTH Forced Rework Locations

A standard solder fountain was used to rework both the DIMM and Ethernet connectors with each board being preheated using a stand-alone convection oven which was located 3 meters away from the solder fountain. A tacky flux was applied to the rework location using a brush after preheat. Care was taken in selecting solder fountain nozzles which provided a sufficient degree of spacing around the connector. Early trials indicated issues in reworking the DIMM connector when using a nozzle which had a minimum spacing of 3mm. Any slight misalignment of this nozzle during rework would cause the nozzle wall to touch the outer pins, making the rework of the connector impossible. A second trial was performed using a slightly larger nozzle, which provided sufficient spacing to allow for a successful rework of the DIMM connector.

Design of Experiment

The design of experiment included the high I/O DIMM connector and an edge Ethernet connector (Table 16). Each connector had barrels connected to multiple ground layers, with typical thermal relief design patterns. Two different PCBA surface finishes were included, HTOSP and LF HASL, as well as two different sets of boards soldered with different alloys, SAC305 and Alloy A. Based on results from past studies, it was decided to rework all boards using Alloy A, as this alloy exhibited superior copper dissolution properties compared to the SAC305/405 alloys. The variables tested which were anticipated of having the largest impact on the rework results were pot temperature and solder contact time. The minimum pot temperature used was 270°C. It was also decided to include rework using a set-point of 290°C to understand the benefit that an additional 20°C would provide in the ability to remove and replace these connectors; keeping an eye on any board laminate damage during final inspection. With respect to contact time, three levels were used, which included a mix of cycled and continuous timed approaches. The current specification of 3 cycles x 8 second (Contact Time A) was included, as well as a maximum of 40 seconds, one level using a 4x10 second cycles (B) and the other level running the rework at a continuous 40 seconds (C).

Table 16. Rework Design of Experiment

Factor	Levels		
Connector Type	DIMM	Ethernet	
PCB Surface Finish	HTOSP	LF HASL	
Wave Alloy	SAC305	Alloy A	
Pot Temp. (°C)	270	290	
Solder Contact Time	A	B	C

Ethernet Connector Rework Results

The edge Ethernet connector was successfully removed and replaced across all levels of the DoE, with exception to the 270°C, 3 cycles x 8 second contact time attempt. The barrel fill and lab analysis results are summarized below for this connector. All boards reworked were x-rayed with the same 10-slice program which was used in the primary attach phase, in order to inspect for barrel fill %. The results from this inspection on the reworked Ethernet connectors were analyzed and compared against the final primary attach validation builds using Alloy A. As seen in Figure 25, the Ethernet barrel fill results achieved within the rework DoE were superior to that of the initial primary attach results. This connector type had difficulties achieving 50% barrel fill on the ground connections when wave soldering. This was a result of the challenging board design, in addition to the selective pallet opening. The ground connect design on this connector had 10 layers, 12oz copper, with a 1-spoke, 30mil width thermal relief – which offered a challenge in terms of barrel fill. The 1X rework process exposed the PCB to between 10-15 seconds of contact time when re-soldering the newly placed connector, where as the wave soldered connector was exposed to 8 seconds contact time. In addition, the wave soldered board utilized a selective solder wave pallet, which minimized the solder contact area. The rework board had a larger surface area exposed to the molten solder, helping to transfer heat through the PCB, improving solder wetting.

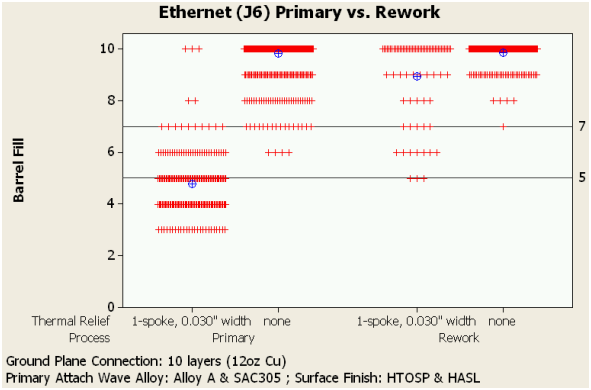


Figure 25. Ethernet (J6) Rework vs. Primary Attach, Minimum Barrel Fill% Results

Looking at the rework DoE in more detail, it can be seen from the chart below (Figure 26), that there were challenges when attempting the J6 rework when using a solder contact time of 3 cycles x 8 seconds (A). In the case of the 270°C, HTOSP, SAC305 wave alloy rework the physical removal and replace was not even possible. There was no visible difference between the benefits of using a 40 second cycled approach (B) or cumulative (C) contact time when

reworking the Ethernet connector. In addition, there was no difference between the two pot temperature settings used. There was a visible difference between the reworks of the Alloy A assembled boards between the HASL and HTOSP surface finishes. The presence of the LF HASL coating the barrels obviously aided in solder wetting during rework and the wetting performance of the SAC305 alloy used during primary attach was superior to Alloy A. However, regardless of this difference in performance all reworks passed IPC-610, Class 2 specification for barrel fill.

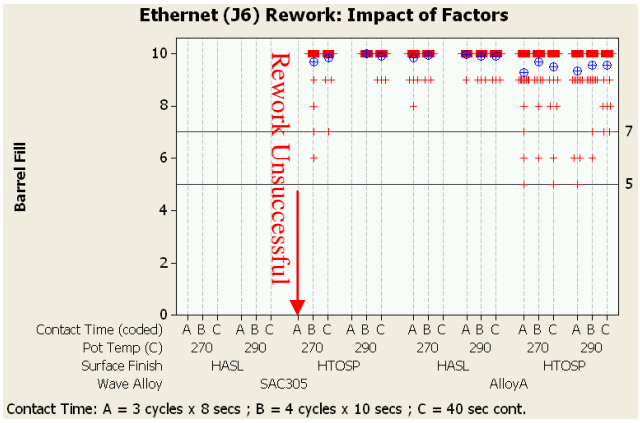


Figure 26. Ethernet (J6) Rework DoE Minimum Barrel Fill% Results

The samples selected for lab analysis included both extremes in pot temperature and cumulative contact time. Also, both HTOSP and LF HASL surface finishes were included. All samples were x-sectioned along the bottom row of barrels, which included the ground layers. The goal of the lab analysis was to confirm barrel fill, inspect for Cu dissolution and any signs of copper barrel cracking or laminate damage. From the 8 samples x-sectioned, 100% passed 2D x-ray barrel fill analysis, with a minimum barrel fill percentage of 50% (Table 17). The high pot temperature (290°C) and continuous contact time of 40 seconds resulted in a complete loss of the copper knee. The remainder of reworks within the DoE passed barrel fill and had acceptable levels of Cu dissolution (i.e. minimum of 0.50mils) [7].

Table 17. Ethernet (J6) Rework Lab Sample Results

Surface Finish	Preheat Temp (°C)	Pot Temp (°C)	Solder Contact	Remove / Replace	Pass.Fail	Min. Barrel Fill%	Min. Cu Thickness at Knee (mils)
HTOSP	120	270	3 cycles X 8 sec	Yes	Pass	50%	1.37
HTOSP	120	270	40 sec continuous	Yes	Pass	50%	0.78
HASL	120	270	40 sec continuous	Yes	Pass	90%	0.92
HTOSP	120	270	40 sec continuous	Yes	Pass	70%	0.72
HTOSP	120	270	4 cycles X 10 sec	Yes	Pass	60%	0.98
HTOSP	120	270	4 cycles X 10 sec	Yes	Pass	60%	0.44
HTOSP	120	290	40 sec continuous	Yes	Pass	70%	0.00
HASL	120	290	40 sec continuous	Yes	Pass	90%	0.00

DIMM Connector Rework Results

The DIMM connector rework offered some challenges with respect to rework, based on the high I/O count and challenging thermal ground design features. The connectors were successfully removed and replaced under a higher pot and preheat temperature. Lab analysis was performed to determine whether the resulting reworks passed IPC-610 Class 2 specifications for barrel fill and to confirm the acceptability of the level of Cu dissolution and laminate integrity due to the increased temperatures used. With respect to the DIMM connector rework results, Figure 27 shows the comparisons against the primary attach build results. As seen, the final barrel fill results from the rework of nine DIMM (D3) connectors were similar to the results obtained from the wave solder, primary attach. In the case of primary attach, the barrels which failed IPC 610, Class 2 were those which were connected to a solid ground connection (not recommended). The rework boards showed a scattering of defects occurring on barrels which were connected to solid ground, but also on barrels with no ground connections.

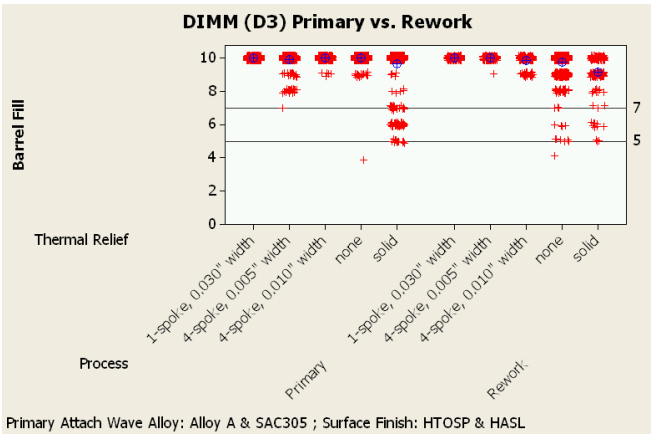


Figure 27. DIMM (D3) Rework vs. Primary Attach, Minimum Barrel Fill% Results

A sample of DIMM connectors reworked, were selected for 2D x-ray verification and x-sectional analysis. The samples were x-sectioned at the locations which showed the worst case barrel fill. In all cases, this was at the edge of the DIMM (D3) connector which was designed with a solid ground connection. From the x-section, barrel fill was confirmed and the copper thickness at the knee of each barrel measured. From the samples x-sectioned, 100% passed 2D x-ray barrel fill analysis, with a minimum barrel fill percentage of 50%. However, a few barrels exhibited marginal Cu dissolution levels which fell below the specification limits (Figure 28).

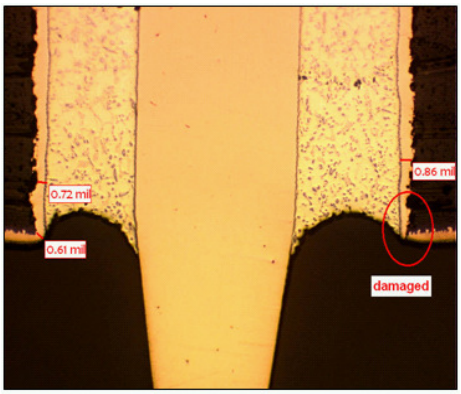


Figure 28. D3 X-Section, Copper Dissolution

CONCLUSIONS

The main objectives of this project were to verify the capability of and understand the challenges associated with assembling and reworking PTH connectors on a high complexity server type product, through the use of test and product vehicles. The final results of this program produced information based on quantitative data which verifies the factors which contribute to a successful assembly of PTH connectors, and also highlights challenges which require additional study. These lessons learned, recommendations and remaining challenges are summarized below.

Design for Manufacturing

In summary, the following DFM data points / trends ascertained from this study are listed below:

***Finished Hole Size*:** Pin to hole clearance appears to be the primary design feature that either restricts or enables good barrel fill.

- Recommended to increase the pin-to-hole clearance > 10mils on high I/O devices
- Recommended to increase the pin-to-hole clearance on low I/O devices

***Ground Plane and Thermal Relief Designs*:** Ground plane design had a significant impact on barrel fill results, in addition to stack-up design.

- A solid connection, regardless of quantity of layers connected resulted in poor barrel fill results and difficulties in reworking and should be avoided.
- All 3 thermal relief designs tested provided barrel fill > 50% in an array of DIMMs
- Entrance effects are still visible even on thermal relieved barrels

***Selective Pallet Openings*:**

- 100mil pallet spacing sufficient for side clearance but more end clearance is required
- Titanium inserts improved barrel fill results on spacings < 150mils
- The perpendicular pin headers with the Titanium inserts were always the best performers
- Parallel to the wave was always the worst performer - however, the differences were small.

Design of Experiment

- From the DoE phase, process factors having the largest statistical impact on barrel fill performance in rank order were (1) Flux Chemistry, (2) Surface Finish and (3) Alloy
- The water wash flux used within this study (WW1) provided the best overall barrel fill results, however is not a necessity to provide acceptable final yield results when considering the benefits from the other factors included in the study.
- The VOC fluxes included provided reasonable results, however on-going study of future developed flux chemistries is recommended to aid in improving the barrel fill performance
- With respect to alloy performance there was minimal difference in barrel fill results between the SAC305/405 alloys vs. Alloy A and B.
- There was a minimal difference between the performances of all three surface finishes tested on barrel fill.

Validation Builds

Process yield data from both the Test Vehicle and the Product Vehicle confirmed that current parameters can result in reasonable yields on “standard pin configurations”. However the design alterations and deviations from design guidelines in current product can pose real problems relative to barrel fill. Pin-to-hole clearance appears to be the primary design feature that either restricts or enables good barrel fill. Multiple parallel barrels make heat flow along internal plane layers resulting in better overall results. Isolated components with very low pin counts (E-caps, LEDs and 3 pin headers are examples) require much larger hole sizes for the same pin diameter because there is no parallel internal heating to enhance the flow of energy.

Forced Rework

Forced PTH lead-free rework of high I/O connectors on high thermally massive PCBs continues to be a challenge when using existing solder fountain equipment technology. The current solder fountain does not provide sufficient heating options to maintain board core temperatures during the rework of a high complex PTH connector. Proper thermal relief designs are necessary to improve the ability of rework. Solid ground connections are not recommended.

FUTURE WORK

The preliminary results relating to the rework of the DIMM connector on the test vehicle have proven to be challenging. Process optimization work using the standard solder fountain rework equipment has indicated some improvements in the success rate of reworking this connector type. However, the improvements were a result of increasing pot and preheat temperatures higher than typically recommended. Even with this the process window still remains relatively small, resulting in inconsistent results when reworking a large high I/O type connector using standard solder fountain equipment, preheat methods and currently available flux/alloy chemistries. It is apparent when reworking these larger I/O connectors on a high thermal massive PCB, that an increase in the board’s core temperature is necessary throughout the rework in order to increase the available process window. Therefore, further work is required to investigate alternative rework equipment solutions which will aid in maintaining preheat of the PCB surface/core during the rework operation. In addition, further investigations into the benefits of increasing pin-to-hole clearance, will be performed.

AKNOWLEDGEMENTS

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