

# **Hi Pot Dielectric Breakdown Automated Verification How-To**

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## **Abstract**

The Printed Circuit Board (PCB) builds get ever more complex. With this the layer counts climb but the overall thickness remains the same. From this the cores of the build are reduced and the dielectric layers are reduced. When this happens there are more concerns regarding how these stack-ups can withstand higher voltage with the thinner cores. OEMs are making stronger requirements regarding dielectric withstanding. This paper will outline how the Electrical Test industry combats these requirements and provides solutions to adhere to these ever changing requirements. IPC states methods, ie TM-650 and IPC-6012 but these are guidelines. This paper will elaborate around these requirements regarding Condition A and Condition B from the TM-650 specification.

The paper will also outline the opportunities around testing Dielectric Breakdown or HiPot. The paper will outline:

HiPot Manual Testing

HiPot Fixture Assisted Testing

HiPot Full Automation Testing

Voltages, dwell, ramp and current cutoffs will be explored.

The paper will further extrapolate to educate OEMs the full guidelines regarding what HiPot testing is designed for and the difference for high potential individual net testing.

Reference Specifications:

IPC-6012

IPC-TM-650

IPC-9252A

## **Abstract 2 Automated Verification**

This paper will outline the opportunities for automating the manual verification of Electrical Test Faults from Bare Board Electrical Test Equipment. In many cases the faults from Electrical Test Equipment require manual verification. With this it may introduce vehicles for error. Manual verification can introduce variables that an automated solution can cancel. Automated Verification implements a combination of Grid Test Machines and Flying Probe to fully verify faults identified without the need for human intervention. This alleviates the element of manual intervention. This paper will elaborate on the flow of an automated test solution where Grid Machines can be complimented with Flying Probe Equipment to provide a

fully data driven automated test solution. Barcodes are used to tie the Grid Test Machines to the Flying Probes. The solution uses operators to move the product from one machine to the other but a databases controls the pass/fail of the product. This ensures product is moved through the operation efficiently and the equipment validates the product without any human intervention.

This paper will outline an automated solution for any test operation to ensure efficiency. Specifics of the solution will be only a block or flow diagram. Specifics on equipment and/or process shall be the determination of the OEM or individual operation. Generics of the solution will only be presented.

### **Hi-Pot Dielectric breakdown**

Dielectric Breakdown, Hi Pot, Insulation Test. These are all acronyms of the same basic test. Can the PCB withstand the voltage stress applied to it?

However, we must understand the difference between Hi-Pot (Dielectric Testing) and standard High Voltage Test.

Hi-Pot or Dielectric Withstanding testing is designed to validate the insulation between atypical plane or potential layers. Typically this is VCC and GND layers or combinations of split planes. A distinction must be made here regarding the test of dielectrics vs the high voltage test of individual nets. Hi-Pot by definition via TM-650 is the test of insulation of atypical potential layers, aka power and ground. When this test is indicated the industry provides 3 venues for accomplishing this.

- A) Manual testing – Probes to pairs
- B) Semi-Automated Test – via wired fixture
- C) Fully Automated – via Flying Probe

Per the IPC specifications there are two basic conditions for Hi-Pot Testing: Condition A and Condition B

The main parameters to consider are: Voltage, Ramp Time and Dwell Time.

Voltage= The potential to apply to the test. This could be both AC or DC as indicated

Ramp Time = The time in seconds to bring the voltage to the required level

Dwell Time = The time to maintain the voltage at the required level

IPC recommends Ramp time to be 1 second/per 100V required

Dwell shall be as recommended 30 seconds

So How Shall We Test?

As in all contract review the procurement document or master drawing will take precedence. If this is not indicated the default IPC Condition A shall be applied:

Test Voltage: 500VDC

Ramp Time 5 Seconds (1 second per 100 Volts)

Dwell Time 30 Seconds (Time to hold at potential)

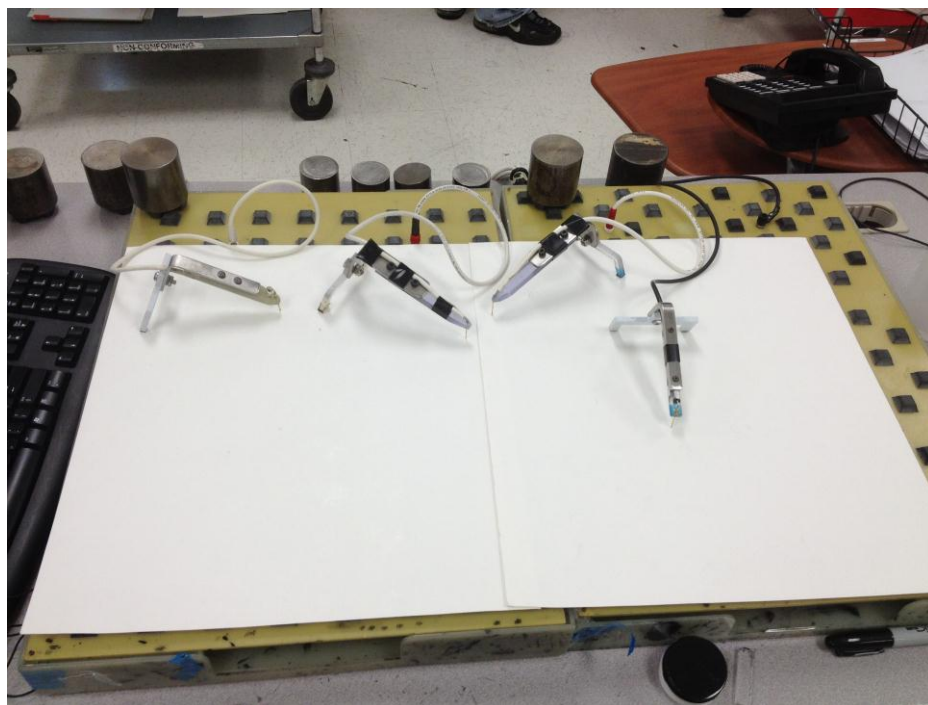
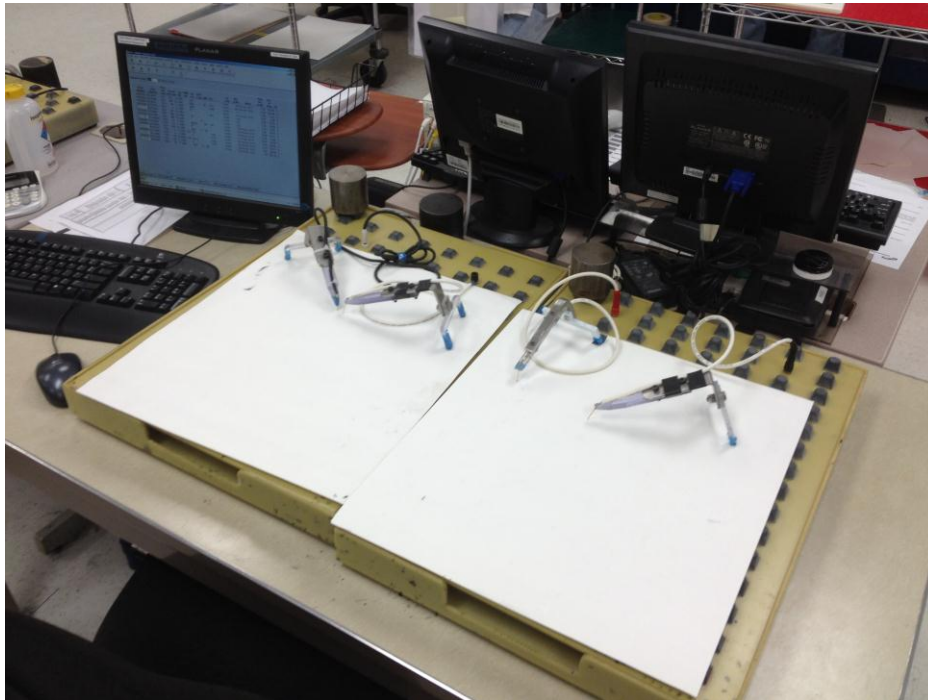
(IPC Condition B is 1000VDC with Ramp and Dwell remaining same)

Please remember that other parameters can be stipulated via the procurement document and/or Master Drawing and will supersede the IPC recommendations.

Now with that said, what are our options for performing this test? There are 3 main methods; manual probing which requires full operator activity to move probes between the pairs; fixture testing that allows the analyzer to sequence the pairs without operator intervention; and full automation where a Flying Probe tests all pairs automatically.

**Manual Testing:**

This method requires the operator to manually program the analyzer to test the pairs on at a time. Voltage, ramp and dwell have to be manually programmed. Figure 1 indicates this type of test. Note the manual probes to be used to probe the PCB.



**Figure 1**

An enhancement to this process is Hi-Pot fixture testing. This incorporates a drilled fixture that is wired for the pairs requiring test. This allows the analyzer to automatically switch between the pairs that require test. This is advantageous when multiple pairs are required. The operator only needs to place the board on the fixture and initiate the test. The analyzer then automatically sequences between the pairs and the operator does not need to move probes. Figure 2 depicts the fixture solution.

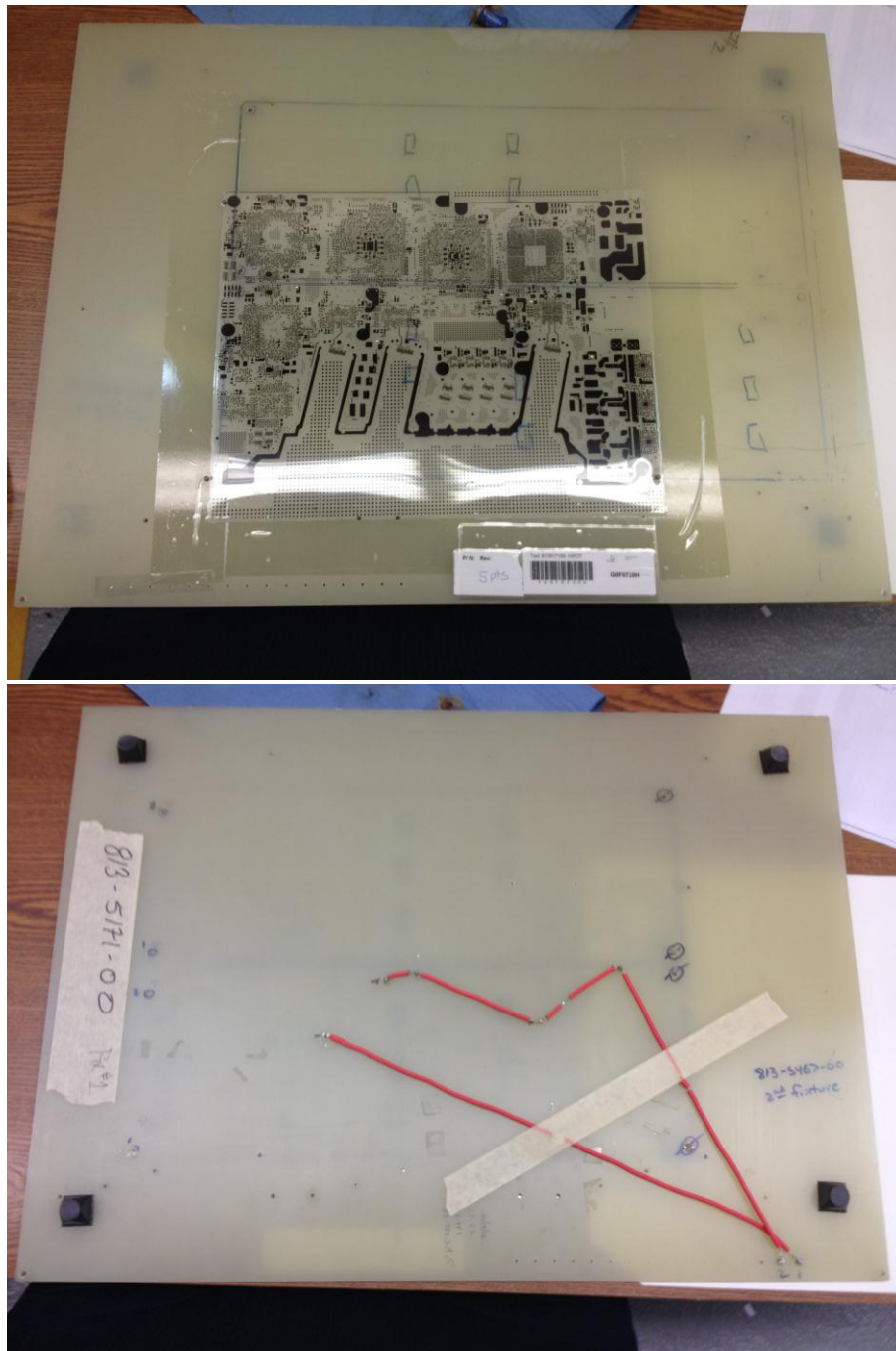


Figure 2

The final solution is the fully automated test. This is provided by a Flying Probe Machine. The pairs are programmed in an adjacency method for the Flying Probe. With the proper programming interface to the Hi-Pot Analyzer this test can reduce much time. In this case the operator only needs to load the board to the machine and initiate the test.

The amount of pairs requiring test is irrelevant as the machine performs all tests automatically. This allows the operator to perform other tasks as indicated to improve efficiency of the overall operation. Figure 3 is the automated solution.



Figure 3

### Summary Hi-Pot

#### Dielectric Test is Plane Layers

Does NOT include Net to Net Testing. This designation should not be synonymous with high voltage testing of individual nets. This has been an industry problem on Master Drawings with regard to voltage requirements. Dielectric or Hi-Pot is related to only the insulation test of cores between plane layers. For high voltage tests on specific nets (Military common with this) it should be designated specifically as High Voltage Tests and not Hi-Pot. There is a difference.

#### **Automated Verification**

In the arena of Electrical Test the verification of faults has become very important. The manual verification of errors introduces the possibility of error. Grid test machines or Flying Probes report errors from their perspective tests which require manual verification.

Methodologies exist today where Grid Test Machines are able to catalog their errors to a common data server. From this Flying Probe Machines can read these data files and retest the PCB specific to the errors reported.

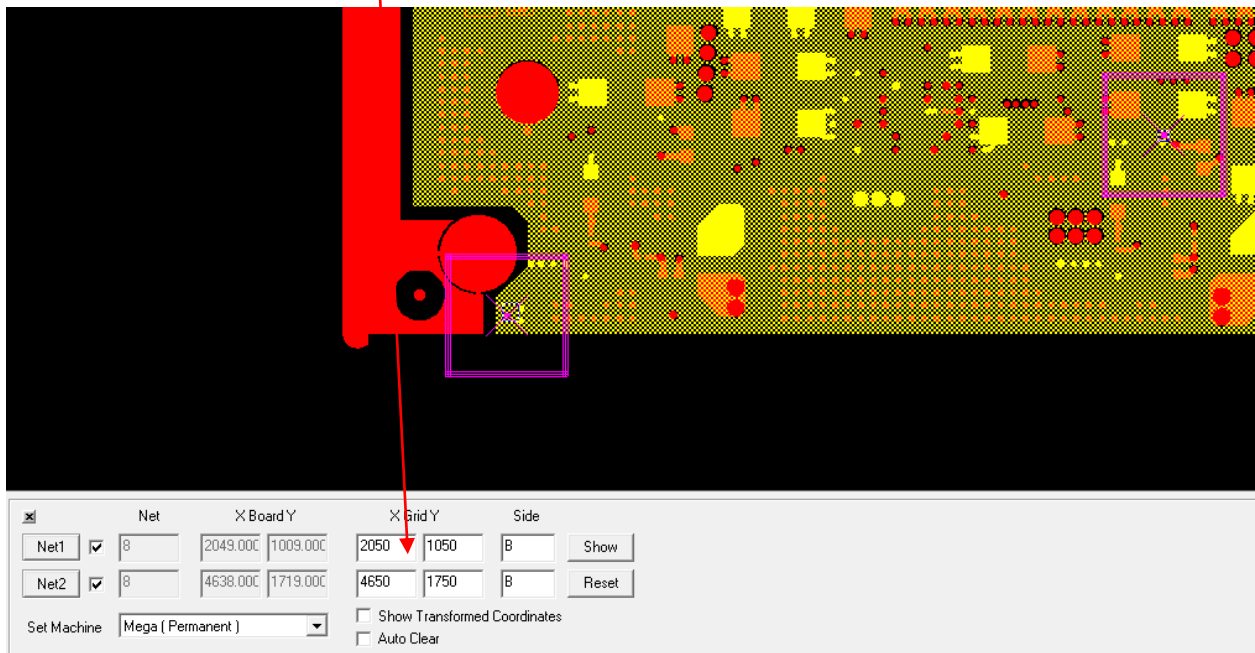


Scenario:

Grid test machine tests and reports the following errors:

```
;MDF02.00
$B0000741
XC
R490036++G0D4152+0000741Q
C0
JG0D4152
S490036
D2011/11/14 14:52:52
Oundefined
P2.00e+01 1.00e+07 1.00e+02 1.00e-01
T1 2048/1009 4637/1718
G1 2050/1050 4650/1750
T1 2048/1009 6570/2953
G1 2050/1050 6600/3100
T1 2048/1009 6806/3853
G1 2050/1050 6800/4000
T1 2048/1009 4078/5173
G1 2050/1050 3550/4950
T1 2048/1009 5678/5454
G1 2050/1050 6000/5200
T1 2048/1009 9593/8303
G1 2050/1050 9800/8800
T1 2048/1009 12989/11637
G1 2050/1050 12900/11900
T1 2048/1009 7482/13793
G1 2050/1050 7500/13800
T1 2048/1009#7712/4834
G1 2050/1050#7900/4900
T1 2048/1009#8989/5029
G1 2050/1050#8850/4850
T1 2048/1009#7806/5334
```

3



This is also printed on an error tag with a barcode. This tag can be scanned by the Flying Probe which will read the above error list and test specifically the errors reported by the grid machine. This eliminates the human intervention and thus reduces the possibility of verification error. Graphic software tools can then be used by a verification operator to validate the actual faults which eliminates the possibility of false pass scenarios.

#### Conclusion & Take-Away

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- ✓ Hi-Pot test is for test of dielectrics and core insulation
- ✓ High Voltage Test is for net to net testing
- ✓ IPC TM-650 notes two conditions for Hi-Pot, A- 500V and B-1000V
- ✓ 3 options for test, Manual, Fixture and Full Automation
- ✓ Automated Verification
- ✓ Removes operator intervention
- ✓ Security against escapes
- ✓ Increased efficiency