As originally published in the Pan Pacific Symposium Proceedings.

EMERGING SUBSTRATE TECHNOLOGIES FOR PACKAGING

Henry H. Utsunomiya
Interconnection Technologies, Inc.
Suwa City, Nagano Prefecture, Japan
henryutsunomiya@mac.com

ABSTRACT

This presentation will outline the market dynamics driving the development of advanced substrates in today's industry landscape. Technological advancements have shifted from Personal Computers to Mobile Applications like Cellular phones, MPEG players, etc. An overview of the technology revolution of substrates and their corresponding packages will be discussed in terms of technology supply chain matching: assembly technology, substrate technology and system technology. Advanced substrate technology roadmaps of leading Japanese suppliers will be reviewed. The evolution of buildup substrates, which have standardized under the direction of CPU & FPGA manufacturers will be explained. The two technological directions of substrates for advanced electronic packages will be mapped out: miniaturization and functional integration, and explained in terms of "More Moore" and "More than Moore", respectively. Fine pitch wiring on substrates can be combined with embedded active and passive devices and has been proven as a technology. Examples/ illustrations of advanced substrate applications in servers, hand -helds, and high end servers and communication equipments will be reviewed: PoP, Embedded Active Devices, Si interposers and Wafer Level Packages, etc.

Key words: Packaging substrate, Embedded Active Devices, Si Interposer, Wafer Level Package, PoP

INTRODUCTION

Worldwide printed wiring board production in 2008 was estimated 51,530 million US$ and Japan was produced 11,561 million US$ (22.4 %) by WECC (World Electronic Circuits Council) Global PCB production Report. And worldwide packaging substrate production in 2008 was estimated 8,925 million US$. In 2008, Japan produced 4,414 million US$ packaging substrate and total share was 49.5 %. Taiwan is second large production of packaging substrate with 2,316 million US$ and Korea followed Taiwan with 1,410 million US$ [1].

Japanese domestic packaging substrate production amount in 2008, buildup structure substrate shares 55.4 % and rigid structure substrate shares 20.1 %, while tape structure substrate including TAB (Tape Automated Bonding) and COF (Chip on Film/Flexible) shares 19.3 %. Package substrate production in 2009 is expected to be divided as follows; rigid substrates are estimated to be 35.6 Billion ¥, 11.7 % share, buildup substrates are estimated to be 190.0 Billion ¥, 62.5 %, and the tape substrate share is estimated to be 61.2 Billion ¥ or 20.1 % share [2]. In addition, Japanese packaging substrate manufacturers expect a CAGR of 11.9 % (2009 to 2013) for next 5 years. Figure 1 and figure 2 are illustrated Japanese packaging substrate production amount progress and Japanese printed wiring boards production amount progress respectively.

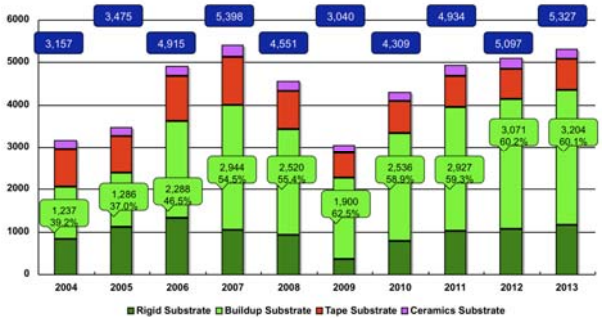

Figure 1. Japanese Packaging Substrate Production Amount Progress (Unit: 100 Million ¥) [2]

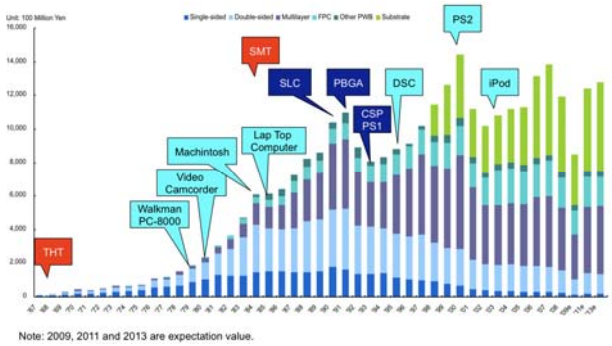

Figure 2. Japanese PWB Production Amount Progress (Unit: 100 Million ¥) [2]

Figure 3 and figure 4 are shown printed wiring board products production amount share in 2007 and average growth rate of 2005 – 2007, and PWB production amount share in 2008 and CAGR 2005 - 2008 respectively.

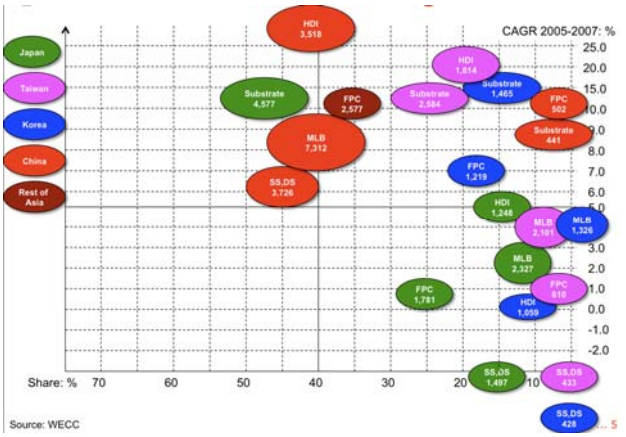

Figure 3. PWB Production Amount Share & CAGR in 2007 (Unit: Million US$) [3]

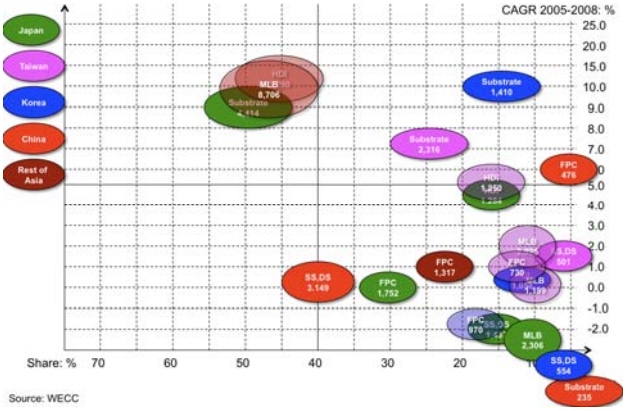

Figure 4. PWB Production Amount Share & CAGR in 2008 (Unit: Million US$) [3]

BACK GROUND OF PACKAGING SUBSTRATE ROADMAP

Actual scaling of semiconductor is more accelerated than ITRS roadmap and 32 nm technology nodes was announced by Intel and IBM such as SRAM using 19 billion transistors and 22 nm SRAM development in 2008 and 2009 respectively. To accomplish 32 nm technology nodes, several challenges on reducing power consumption, improving signal speed and external data transmission speed are required for reduced leakage current, reducing coupling for minimized signal propagation delay, and increased data bus width by increased number of I/O terminals. Scaling of semiconductor enable to reduce gate delay, while interconnect delay increasing exponentially due to resistivity increased by narrower wiring and increased length of global wiring. In addition, I/O terminal pitch should be decreased to less than 125 μm to assure power integrity. Figure 5 is shown performance bottleneck by interconnect delay and figure 6 is shown technology innovation by data bus width.

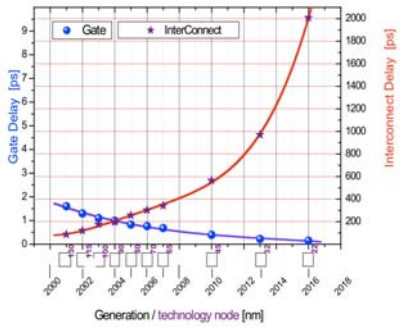

Figure 5. Performance Bottleneck by Interconnect Delay [4]

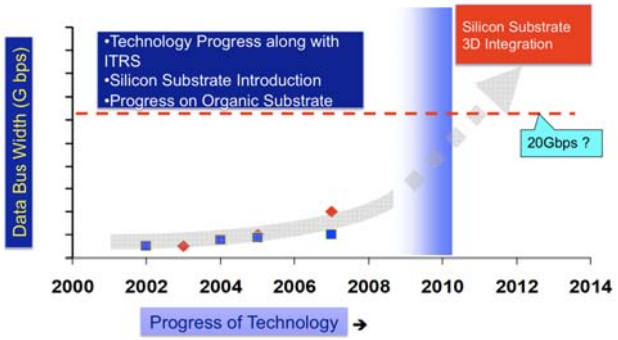

Figure 6. Technology Innovation by Data Bus Width [5]

For flip chip package, organic substrate is difficult to adopt high bump account and less than 100 μm bump pitch with economical cost due to difficulty on 15 - 10 μm via hole diameter generation with existed laser drilling process. More over difficulty on 5 μm line width and space generation with 50 μm via diameter by current CO_2 laser drilling. In addition, in small form factor portable products required 150 μm solder ball pitch for motherboard in 2011. For very fine pitch chip package bonding, alternative technology such as silicon interposer with TSV is one of candidate technology to solve finer wiring and via diameter for high-end applications. And fan-out CSP can ease to solder ball pitch for portable products. In addition, embedded devices into substrates, motherboards and module boards will enable to solve these issues. Table 1 is shown chip to package interconnect technology requirements and Table 2 is shown package to board interconnect technology requirement.

Table 1. Chip to Package Technology Requirements [6]

Item		Unit	2009	2010	2011	2012	2013	2014	2015	2018	2020
Au Wire Bond	Single in-line	μm	35	30	30	25	25	25	25	25	25
	Two-row Staggered Pitch		40	35	35	35	30	30	30	30	30
	Three-tier Pitch		50	50	45	45	40	40	35	35	35
	Wedge		20	20	20	20	20	20	20	20	20
Cu Wire Bond	Single in-line	μm	50	45	40	40	35	35			
	Dual-row		60	50	45	45	40	40			
Chip on Film		μm	25	20	20	15	15	10	10	10	10
Flip Chip	Area Array: Low End	μm	210	210	200	200	180	180	150	150	150
	Area Array: Mobile Products		150	135	120	110	110	100	100	95	95
	Peripheral: Mobile		60	50	50	40	40	40	40	35	35
	Area Array: Notebook	μm	150	135	120	110	110	100	100	95	95
	Area Array: High Performance		160	150	150	130	130	120	120	110	110
	Flip Chip: Harsh										

Table 2. Package to Board Technology Requirements [6]

Item		Unit	2009	2010	2011	2012	2013	2014	2015	2018	2020
Solder Ball Pitch	Low Cost, Handheld	mm	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50	0.50
	Cost-Performance		0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50	0.50
	High-performance		0.80	0.80	0.65	0.65	0.50	0.50	0.50	0.50	0.50
	Harsh		0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50	0.50
Small Portable Products	Low Cost, Handheld	mm	0.65	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
	Harsh		0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50	0.50
	CSP Area Array Pitch		0.20	0.20	0.15	0.15	0.15	0.10	0.10	0.10	0.10
	QFP Lead Pitch		0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
	SON Land Pitch		0.40	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
	QFN Land Pitch		0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
	P-BGA Ball Pitch		0.80	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65
	T-BGA Ball Pitch		0.65	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
	FBGA Ball Pitch		0.30	0.30	0.20	0.20	0.20	0.20	0.20	0.15	0.15
	FLGA Land Pitch		0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30

Generally, motherboard design rule is define one line between via holes and major mounted device package is fine pitch BGA, while packaging substrate design rule is defined two or three lines between via holes. For 0.15 mm pitch solder ball F-BGA requires 40 μm via diameter on 75 μm land diameter with 25 μm line width/space, generally. In case of flip chip bump pitch of 100 μm, 30 μm to 50 μm via diameter on 70 μm land diameter with 6 μm line width/space is needed for 2 lines between via holes and 3 μm line width/space is needed for 3 lines between via holes with same via land diameter. For 30 μm via formation, it is capability limitation of UV-YAG laser and it may require Excimer laser. However, through put of Excimer laser is not enough for huge number of via holes formation. Table 3 is shown general design rules on motherboard and substrate.

Table 3. General Design Rules for Motherboard & Substrate [7]

Item	Mounted Device	# of Lines/ Via	Pad Pitch (mm)	Space Width (μm)	Line Width (μm)	Space Width (μm)	Land Diameter (μm)	Via Diameter (μm)
Mother-board	FBGA (CSP)	1 Line/Via	0.50	75	75	75	275	150
			0.40	60	75	60	200	100
			0.30	50	50	50	150	75
			0.20	30	40	30	100	50
			0.15	25	25	25	75	40
			0.10	18	18	18	50	30
Substrate	FC	2 Lines/Via	0.18	18	18	18	90	60 - 50
			0.15	15	15	15	75	40 - 30
			0.13	15	15	15	50	30 - 20
			0.10	15	10	15	30	15 - 10
		3 Lines/Via	0.18	10	10	10	90	60 - 50
			0.15	8	10	8	75	40 - 30
			0.13	8	10	8	50	30 - 20
			0.10	5	5	5	30	15 - 10

Semi-additive Process Required UV-YAG Laser, Excimer Laser Required

SUBSTRATE TECHNOLOGY ROADMAP

For packaging substrate roadmap, we classified technology difficulties into 6 categories such as “Low Cost”: P-BGA for conventional consumer products with conventional technology, “Hand-held”: FBGA (CSP) for portable products, “Mobile Products”: SiP and PoP for smart phone and mobile PC, “Cost Performance”: Buildup substrate P-BGA for CPU, GPU and game processor, “High Performance High End” Buildup substrate P-BGA and Silicon interposer BGA for high end routers, and “High Performance”: LTCC BGA for routers and servers.

Table 4 is shown typical package type of each application.

Table 4. Description of Typical Package Type by Application [6]

Category	Package Type	Max. Body Size: mm	Typical Body Size: mm	Max. # of Pins	Typical # of Pins	Typical Substrate Materials	Max. # of Layers
Low Cost	P-BGA	35×35	27×27 31×31	1000	676 900	High Tg FR-4	4
Hand-held	F-BGA	15×15	10×10 12×12	400	300 360	High Tg FR-4	6
Mobile Products	SiP (F-BGA)	21×21	10×10 12×12 15×15	800	300 360 400	High Tg FR-4	6
Cost Performance	P-BGA	42.5×42.5	30×30 35×35 37.5×37.5	1300	300 360 400	High Tg FR-4 + Epoxy	3+4+3
High Performance	P-BGA S-BGA	70×50	45×45 50×500	2500	2500	High Tg FR-4 + Epoxy Silicon	6+6+6 6 8 10
High Performance	C-BGA	51×51	45×45	2500	1800	Al_2O_3	20

In mobile products application, the combination of high glass transition temperature FR-4 and epoxy film is dominant today.

Minimum line width/space of 20 μm/20μm today will decrease to 15μm/15μm in 2012 and it will expect to less than 10 μm in 2018. However, micro via diameter scaling

is moderate and 80 µm today will expect to down to 50 µm in 2018, due to economical reason such as maintain via formation process cost and save capital investment for new laser drilling system. Table 5 is shown mobile product substrate roadmap.

Table 5. Mobile Products Substrate Roadmap [6]

Mobile Products (SiP, PoP)	unit	2009	2010	2011	2012	2013	2014	2015	2018	2020
Parameter										
Chip to Substrate Interconnect Land Pitch	µm	50	50	50	50	50	50	50	50	50
Min. Finished Substrate Thickness	mm	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Core Material Tg	°C	180	180	180	210	210	210	210	210	210
Core Material CTE (X-Y)	ppm/°C	14	14	14	13	13	11	11	11	11
Core Material CTE (Z)	ppm/°C	40	35	35	30	30	30	30	30	30
Core Material Dk@1GHz	-	4.2	4.2	4.2	4.2	4.2	4.0	4.0	4.0	4.0
Core Material Df@1GHz	-	0.013	0.013	0.013	0.013	0.013	0.010	0.010	0.010	0.010
Core Materials Young's Modulus	GPa	24	24	24	24	24	24	24	24	24
Core Material Water Absorption	%	0.10	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07
Buildup Material Tg	°C	156	156	156	166	166	166	166	177	200
Buildup Material CTE (X-Y)	ppm/°C	13	13	13	12	12	12	12	12	12
Buildup Material CTE (Z)	ppm/°C	46	40	40	40	40	40	40	30	30
Buildup Material Dk@1GHz	-	3.4	3.4	3.4	3.0	3.0	3.0	3.0	3.0	3.0
Buildup Material Df@1GHz	-	0.012	0.012	0.012	0.010	0.010	0.010	0.010	0.010	0.010
Buildup Materials Young's Modulus	GPa	4	5	5	5	5	5	5	5	5
Buildup Material Water Absorption	%	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Min. Line width/Space	µm	20/20	18/18	18/18	15/15	15/15	12/12	12/12	8/8	5/5
Min. Conductor Thickness	µm	25	25	25	20	20	15	15	10	8
Min. Through Via Diameter	µm	100	100	100	80	80	80	80	70	70
Min. Through Via Land Diameter	µm	250	250	250	200	200	200	200	150	150
Min. Micro Via Diameter	µm	80	70	70	60	60	60	60	50	50
Min. Micron Via Land Diameter	µm	150	130	130	120	120	120	120	100	100
Min. Through Via Pitch	µm	300	300	300	275	275	275	275	250	250
Min. Solder Mask Opening	µm	80	80	80	60	60	60	60	50	50
Min. Solder Mask Opening Tolerance	µm	20	20	20	18	18	18	18	15	15

Most of CPU, graphic processing engine and game processor are using flip chip interconnect today and it expect to use flip chip until 2020 for cost performance application. Since flip chip bump pitch will decrease from 150 µm today to 80 µm in 2018 due to die size shrinkage are happen for each technology nodes, minimum line width/space have to reach 5µm/5µm with 30 µm via diameter with UV-YAG laser or excimer laser. One of biggest issue on buildup material is residues are remain on the bottom of via holes after desmear process and it affects interconnect reliability. To accomplish sub ten micron wiring together with finer via diameter, material improvement including lower CTE with less fillers, very smooth surface morphology such as less than 100 nm average flatness for finer circuit, lower dielectric loss and optimized Young's modulus are necessary within next 5 years. Table 6 is shown cost performance substrate roadmap.

Table 6. Cost Performance Substrate Roadmap [6]

Cost Performance (CPU, GPU, Game Processor)		2009	2010	2011	2012	2013	2014	2015	2018	2020
Parameter	unit									
Chip to Substrate Interconnect Land Pitch	µm	150	150	150	125	125	125	100	80	50
Min. Finished Substrate Thickness	mm	1.1	1.1	1.1	1.1	1.1	1.1	1.1	0.8	0.8
Core Material Tg	°C	180	180	180	210	210	210	210	210	210
Core Material CTE (X-Y)	ppm/°C	10	10	10	8	8	8	8	8	8
Core Material CTE (Z)	ppm/°C	20	20	20	10	10	10	10	10	10
Core Material Dk@1GHz	-	3.2	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Core Material Df@1GHz	-	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
Core Materials Young's Modulus	GPa	24	24	24	24	24	24	24	24	24
Core Material Water Absorption	%	0.10	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07
Buildup Material Tg	°C	200	200	200	210	210	210	210	210	210
Buildup Material CTE (X-Y)	ppm/°C	13	13	13	12	12	12	12	12	12
Buildup Material CTE (Z)	ppm/°C	46	40	40	40	40	40	40	40	40
Buildup Material Dk@1GHz	-	3.4	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Buildup Material Df@1GHz	-	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Buildup Materials Young's Modulus	GPa	4	5	5	5	5	5	5	5	5
Buildup Material Water Absorption	%	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Min. Line width/Space	µm	18/18	15/15	15/15	12/10	12/10	10/10	10/10	5/5	3/3
Min. Conductor Thickness	µm	25	25	25	20	20	15	15	10	5
Min. Through Via Diameter	µm	100	100	100	80	80	80	80	70	70
Min. Through Via Land Diameter	µm	250	250	250	200	200	200	200	150	150
Min. Micro Via Diameter	µm	60	60	60	60	50	50	50	30	30
Min. Micron Via Land Diameter	µm	150	130	130	120	100	100	100	70	70
Min. Through Via Pitch	µm	300	300	300	275	275	275	275	250	250
Min. Solder Mask Opening	µm	60	50	50	50	50	50	40	40	30
Min. Solder Mask Opening Tolerance	µm	10	10	10	8	8	8	5	5	5

With the semiconductor die size becoming larger, matching of thermal expansion coefficient between the die and packaging substrate becomes critical for high-end high performance application. At present, 8 - 10 ppm/°C is required for core material and 16 ppm/°C for buildup layer material with reinforcement material such as SiO_2 fillers and/or glass yearns. In 2010, most tightest flip chip bump pitch become 125 - 100 µm, silicon interposer with polyimide redistribution layers will introduce to this application. And dielectric material for redistribution layer and/or functional layer materials will change to meso-porous silicon dioxide materials to adopt smaller CTE, mechanical strength and finer circuit in 2015 for tera bit scale data transmission package. One of potential solution is existed for current ultra low κ material for less than 32 nm technology node semiconductors.
Table 7 is shown high-end high performance packaging substrate roadmap.

Table 7. High-End High Performance Substrate Roadmap [6]

High End High Performance		2009	2010	2011	2012	2013	2014	2015	2018	2020
Parameter	unit									
Typical Materials	-	FR-4	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon
Typical Buildup Materials	-	Epoxy	PI	PI	PI	PI	PI	SiO_2	SiO_2	SiO_2
Max. Layer Counts	#	6+6+6	6+2	6+2	6+2	4+2	4+2	4+2	4+2	4+2
Typeical Layer Count	#	6+6+6	6+2	6+2	6+2	4+2	4+2	4+2	4+2	4+2
Min. Finished Substrate Thickness	mm	1.0	1.0	1.0	1.0	0.6	0.6	0.5	0.5	0.5
Typical Finished Substrate Thickness	mm	1.0	1.0	1.0	1.0	0.6	0.6	0.5	0.5	0.5
Core Material Tg	°C	180	1410	1410	1410	1410	1410	1410	1410	1410
Core Material CTE (X-Y)	ppm/°C	8	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Core Material CTE (Z)	ppm/°C	10	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Core Material Dk@1GHz	-	2.8	12	12	12	12	12	12	12	12
Core Material Df@1GHz	-	0.002	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005
Core Materials Young's Modulus	GPa	5.5	185	185	185	185	185	185	185	185
Core Material Water Absorption	%	1.40	0	0	0	0	0	0	0	0
Buildup/RDL Material Tg	°C	200	300	300	300	300	300	700	700	700
Buildup/RDL Material CTE (X-Y)	ppm/°C	16	16	16	16	16	16	3	3	3
Buildup/RDL Material CTE (Z)	ppm/°C	20	20	20	20	20	20	16	16	16
Buildup/RDL Material Dk@1GHz	-	3.3	3.3	3.3	3.3	3.3	3.3	2.0	2.0	1.8
Buildup/RDL Material Df@1GHz	-	0.038	0.038	0.038	0.038	0.038	0.038	0.003	0.003	0.001
Buildup/RDL Materials Young's Modulus	GPa	4	5	5	5	5	5	10	10	10
Buildup/RDL Material Water Absorption	%	1.1	2.0	2.0	2.0	2.0	2.0	0.01	0.01	0.01
Min. Line width/Space	µm	12/10	8/8	8/8	8/8	5/5	5/5	3/3	3/3	1/1
Min. Conductor Thickness	µm	15	10	10	10	8	8	5	5	3
Min. Through Via Diameter	µm	180	180	180	150	150	100	700	70	70
Min. Through Via Land Diameter	µm	350	300	300	250	250	200	150	150	150
Min. Micro Via Diameter	µm	60	60	60	50	50	50	30	30	30
Min. Micron Via Land Diameter	µm	100	100	100	90	90	90	60	60	60
Min. Through Via Pitch	µm	350	300	300	275	275	275	250	250	250

PACKAGING SUBSTRATE TECHNOLOGY ROADMAP

Packaging substrate manufacturers in Japan are expects minimum line width and space of 7.5 µm/7.5 µm volume production will start in 2010 and 5.0 µm/5.0 µm volume production will start in 2014 according to survey results of Jisso Technology Roadmap 2009 edition, as shown in figure 7.

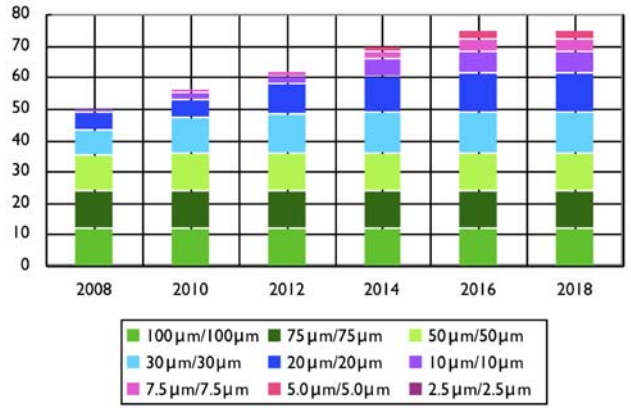

Figure 7. Minimum Line Width/Space for Packaging Substrate Volume Production Behavior (unit: μm) [7]

For printed wiring board roadmap, Jisso Technology Roadmap classified technology difficulties into 3 categories such as "Class A": conventional consumer products with conventional technology, "Class B": portable and cost performance products with leading edge technology and "Class C": highest performance independent cost with state-of-the-art technology.

In "Class C" buildup structure substrate, high-end Field Programmable Gate Array requires minimum line width/space of 5 μm/5 μm in 2010, and "Class B" for CPU and GPU will start volume production of minimum line width/space 5 μm/5 μm in 2014. Table 8 is shown minimum line width/space roadmap for substrate.

Table 8. Minimum Line Width/Space Roadmap for Packaging Substrate (unit: μm) [7]

Structure	Class	2008	2010	2012	2014	2016	2018
Rigid	A	35/35	35/35	35/35	30/35	30/30	30/25
	B	25/25	25/20	20/18	15/18	15/15	15/15
	C	20/15	20/15	15/10	15/10	15/10	12/7
Buildup	A	15/15	10/10	10/10	7/8	7/8	7/8
	B	10/10	7/8	7/8	5/5	5/5	5/5
	C	7/8	5/5	5/5	5/5	5/5	5/5
Tape	A	25/25	25/25	25/25	20/20	20/20	20/20
	B	20/20	20/20	20/20	15/15	15/15	15/15
Ceramics	A	50/50	30/30	25/25	25/25	25/25	20/20
	B	30/30	25/25	25/25	20/20	15/15	15/15
	C	25/25	25/25	20/20	15/15	15/15	15/15

Minimum via diameter below 30 microns is one of technical challenges for packaging substrate manufacturers. Conventional CO_2 gas Laser can fabricate via diameter around 50μm, and below 50μm via diameter UV-YAG Laser is adopts for fabrication. Below 20μm via diameter, Eximer Laser can form, however improvement of through put is required for commercial volume production. Figure 8 is shown volume production behavior survey results on Japanese substrate manufacturers for "Laser Drilling".

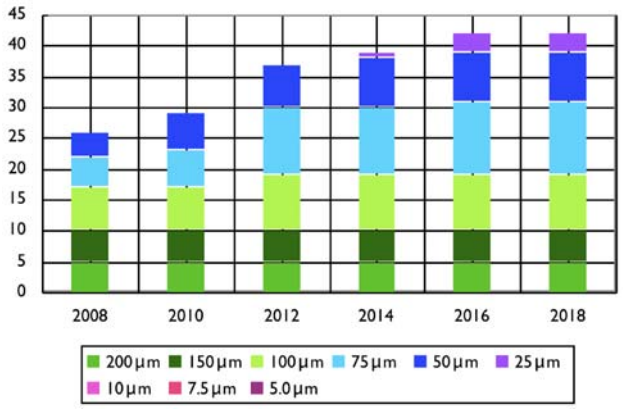

Figure 8. Laser Drill Volume Production Behavior [7]

As for rigid structure substrate, mechanical numerically controlled drilling is commonly uses for 100μm diameter. Incase of 50μm drill bit diameter, rotating speed must increasing to 500,000 rpm to 550,000 rpm while 100μm diameter hired 300,000 rpm. Thus capital investment for new mechanical drilling equipment is necessary to use less than 50μm drill bit diameters. For "Class B" substrate laser drilling, CO_2 gas laser will adopt major process technology toward 2018. Table 9 is shown minimum through via diameter/land diameter roadmap for "Class B" products.

Table 9. Minimum Through Via Diameter/Land Diameter Roadmap for "Class B" Substrate (unit: μm) [7]

Method	Structure	2008	2010	2012	2014	2016	2018
Mechanical Drill	Rigid	100/190	100/160	100/160	75/160	75/160	75/160
	Buildup	100/140	80/120	80/120	80/120	80/120	80/120
Laser Drill	Rigid	60/130	50/120	50/120	50/110	50/110	50/110
	Buildup	80/120	60/120	60/100	50/90	50/90	50/90
	Tape	80/160	60/110	60/110	50/100	50/100	50/100
Punching	Tape	150/200	150/200	150/200	150/200	150/200	150/200
Ceramics		30/30	25/25	25/25	20/20	15/15	15/15

In case of "Class C" buildup substrate, 20μm via diameter was in production in 2008 and 30 μm via diameter also in volume production in 2008 for "Class B" buildup layers. In 2014, 10μm via diameter will start production for high-end applications. Table 10 is shown minimum micro via diameter, land diameter and via pitch.

Table 10. Minimum Land Diameter, Land Diameter and Via Pitch Roadmap for Substrate (unit: μm) [7]

Structure	Description	Class	2008	2010	2012	2014	2016	2018
Buildup	Min. Micro Via/Land Diameter	A	60/100	50/90	40/80	40/80	30/70	30/70
		B	30/70	30/60	30/60	20/50	20/50	20/50
		C	20/60	20/50	20/40	10/40	10/30	10/30
	Min. Via Pitch	A	130	120	110	110	100	100
		B	100	90	80	70	70	70
		C	80	70	60	60	50	50

EMBEDDED ACTIVE DEVICES INTO PACKAGING SUBSTRATE

Embedded active devices and passive devices into packaging substrate as well as motherboard is one of potential solution to filled the gap between semiconductors and printed wiring board wiring density. And it is already start volume production in several manufacturers in Japan, Korea and Taiwan.

Figure 9 is shown categories of embedded passives and actives.

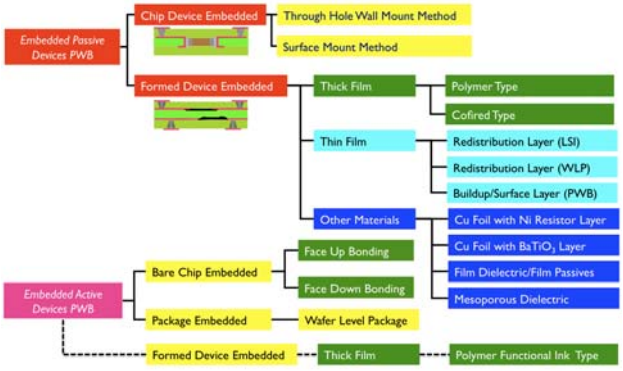

Figure 9. Categories of Embedded Passive Devices and Embedded Active Devices [7]

Regarding on embedded passive devices, there is two major technologies has been used in Japan. One is embedded discrete components such as 0603 (0.6 mm by 0.3 mm) resistors and capacitors with Cu plated terminals are mounted on to printed wiring board inner layer with surface mount equipment, then buried by prepreg or buildup layer materials. The other method is using printed wiring process technologies such as photolithography, etching and plating to form resistor and capacitor functions during PWB fabrication process. Embedded active device is hiring almost same technology of embedded discrete components, however placement of bare die has two directions such as face up and face down.

In the near future, formed active device by functional ink with carrier mobilities of 1 - 10 cm^2/Vs will be introduced. Thick film printed methods using gravure, flexography, screen, offset lithography, inkjet will be adopted for functional ink on a substrate. Table 11 is shown example of current status of active device embedded.

Table 11. Current Status of Embedded Active/Passive Devices [8]

Manufacturers	PWB Technology	Embedded Devices	Applications	Status
Dai Nippon Printing	B²it	LSI (Flip Chip), Passives (Chips)	Camera Module One Segment Module Finger Print ID Module	Volume Production
Toppan NEC Circuit Solutions	Buildup	WLP	One Segment Module	Volume Production
Clover Electronics	B²it	LSI (Flip Chip)	One Segment Module	Volume Production
Taiyo Yuden	EOMIN	Passives (Chip)	Power Supply Module	Volume Production
CMK	Buildup	WLP	TV Tuner Module	Volume Production
Oki Printed Circuit	B²it	WLP	RF Module	Volume Production
Denso	PALAP	LSI, Passives (Chips)	Car Navigation	Volume Production
Panasonic Electronic Device	SIMPACT	WLP, Film Passives	Car Navigation	Volume Production
Fujikura	Polyimide MLB	WLP, Film Passives	Camera Module RF Module	Prototype
Meiko	Thin Core Buildup	WLP, Passives	RF Module, Camera Module	Production in 2010
Imbera DaeDuck	Integrated Module Board (Imbera)	LSI (Flip Chip), Passives (Chip)	Cellular Phone	Volume Production
Samsung Electro Mechanics	Buildup	LSI (Flip Chip), Passives (Chip)	Cellular Phone	Volume Production

SUMMARY

In the next 5 years, the technology of packaging substrate will drive by flip chip interconnection technology with significant higher pin counts and embedded active and passive devices for System in Package. As a result, organic substrate will face technology limitation and silicon interposer or glass substrate will be introduced for high-end applications. In addition, organic substrate using buildup layers will approach minimum line width/space of 5 μm/5 μm with less than 30μm to 5μm via diameter. Table 12 is addressed very advance PWB business structure comparison between last 5 years and next 5 years.

Table 12. Advanced PWB Business Structure [3]

Index of Change	2005-2010	2010-2015
R&D Theme (Min. Line Width)	30μm - 15μm Flip Chip, EAD/EPD, WLP	10μm - 7μm - 5μm - 3μm Flip Chip, EAD/EPD, Silicon Interposer
Via Diameter	75μm - 50 μm	30 μm - 5 μm - 3μm
Capital Investment	$0.15 Billion - $0.20 Billion	US$ 0.20 Billion - US$ 0.50 Billion
Design Parameter	Distributed Constant	Distributed Constant
Major Process	Semi Additive	Semi Additive, Silicon Technology, LCD Technology (Glass Substrate)
Bus Frequency	800 MHz - 1.2 GHz	> 10 GHz
Package Technology Driving Force	SiP/PoP, Embedded Actives/Passives, Wafer Level Package	Embedded Actives/Passives, Fanout WLP, TSV
PWB Type	Buildup PWB, FPC, FRPC	Silicon & Glass Interposer, Buildup PWB
Market Driver	Cellular Phone, Digital Home Appliances, Broad-band Internet	Digital TV, Super Smart Phone, Digital Home Appliance
Profit Structure	High Value Added & Differentiate	High Value Added & Differentiate
Business Model	Core Competence +Horizontal Division of Labor	Core Competence + Strategic Alliance + New Concept

The difficulty of advanced PWB business is capital investment that is tremendous huge for finer wiring board production such as 200 million US$ to 500 million US$ for 50,000 m^2 out put /monthly production factory from scratch. However, active devices embedded into printed wiring boards have potential solution to increase functional density without ultra finer wiring. Both finer wiring technology and integrated function into board level will be coexisted in next 5 years. To accomplish this scheme, infrastructural enhancement of materials, manufacturing technologies, quality assurance and modeling and simulation to advanced packaging substrate as well as embedded active devices are necessary.

REFERENCES

[1] WECC Global PCB Production Report
[2] Electronic Circuits Industrial Survey Report 2008 Edition, JPCA
[3] World Electronic Circuit Council Global PCB Production Report for 2008
[4] Fraunhofer IZM
[5] Toshihiko Nishio, Substrate Technology need by next generation high performance package, 28 Jan., 2009
[6] 2009 International Technology Roadmap for Semiconductors
[7] 2009 Jisso Technology Roadmap, JEITA
[8] H. Utsunomiya, KPCA International Symposium, 20 Nov., 2009