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Embedding Passive and Active Components: PCB Design and Fabrication Process Variations

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Abstract
Embedding components within the PC board structure is not a new concept. Until recently, however, most embedded component PC board applications adapted only passive elements. The early component forming processes relied on resistive inks and films to enable embedding of resistor and capacitors elements. Although these forming methods remain viable, many companies are choosing to place very thin discrete passive components and semiconductor die elements within the PC board layering structure. In addition to improving the products performance, companies have found that by reducing the component population on the PC board's surface, board level assembly is less complex and the PC board can be made smaller, The smaller substrate, even when more complex, often results in lower cost. Although size and cost reductions are significant attributes, the closer coupling of key elements can also contribute to improving functional performance.

This paper focuses on six basic embedded component structure designs described in IPC-7092. The process variations define the structure, depending on whether components are passive or active, placed and/or formed and if they are on one side of the PC board base-core or both. The formed and placed components may be located on any number of layers, however, formed components are generally assigned to dedicated layers. The layering description actually becomes part of the type designation that is very similar in describing an eight layer (2-4-2) HDI board and the naming indicates whether the base-core represents a final assembly or is simply a mounting base onto which additional layers are sequentially added.

Background
The electronic industry is recognizing that to maximize the products potential the printed circuit can no longer act only as a platform for mounting and interconnecting electronic components on the outer surfaces. Many companies have determined, for their products, many of the component elements initially supplied for surface mounting can be efficiently embedded within the circuit layer structure of the boards. The interconnect platform can become a key enabler in developing a system level product. A significant number of semiconductor packaging specialists have already developed multiple die component interposer structures utilizing embedded component technologies on a large scale. Both passive and active component elements are candidates for embedding. In addition to minimizing the components outline, embedding one or more active die in the interposer structure enhances performance due to the shorter interconnect length between active die elements. The embedding process has also resulted in reducing power consumption and increases signal speeds. Expanding the technology to board level products typical of that illustrated in Figure 1 has become very attractive for a number of performance driven products. Both commercial and aeronautic products have become prime candidates for applying embedded component technology but the decision in selecting specific components for embedding, must be made early in the design process.

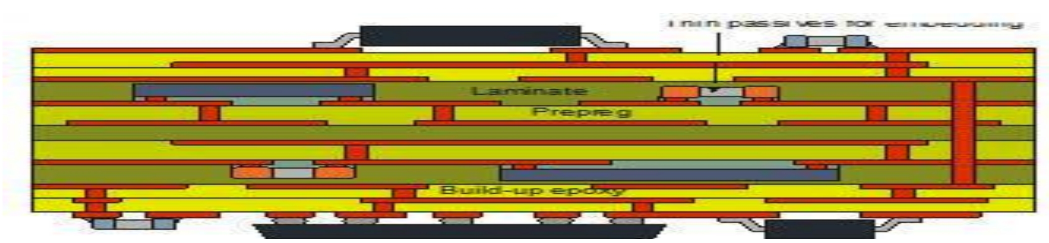


Figure 1- Embedded component PCB
(Example source: AT&S)

Even though a majority of PC board fabrication specialists have the skills to embed a significant number of passive elements, many decline to provide this capability due to its limited application for their existing or mainstream customer base. Because these same suppliers have avoided the development of embedded component processes, customers are aggressively seeking sources that are willing to work with them to produce the next generation of smaller, high performance electronic products.

Planning the Embedded Component PCB
The most mature and economical process developed for embedding passive components is defined as *'forming'*. Using various ink formulations, copper foil based materials and filled dielectric composites, a broad range of resistor and capacitor elements are currently being distributed within the layering structure of the printed board. Inductor elements can be furnished

as well by chemically etching a narrow copper conductor pattern within the circuit. Careful planning is paramount. When planning to embed passive components the designer must consider the tolerance range for the embedded parts. Drift limits following thermal shock or humidity exposure can be an issue as well as the aging behavior of dissimilar materials.

Formed Resistors- Methods utilized in forming resistor elements utilize either a printing or etching process. The printed resistor materials are described as a 'thick-film' composite formulated to furnish a wide range of primary values that enables screen-printing the elements directly onto the pre-patterned land terminations on the circuit board layer (Figure 2).

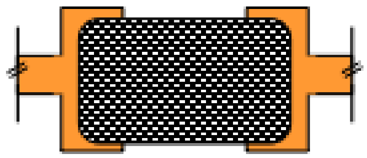


Figure 2- Formed thick-film resistor element
(Example source: IPC-7092)

Several 'thin-film' resistor technologies are also available. Thin-film resistive material is supplied in sheet form with resist values that range from 25Ω per square area to 1kΩ per square area. Thin- film laminates are comprised of a layer of resistive material deposited onto copper foil (Figure 3-1). The foil is then laminated onto the B-stage base material (Figure 3-2) with the resistor surface side facing the base laminate. Following the first stage chemical etching process to define the overall circuit pattern (Figure 3-3) a second etching process selectively ablates a portion of the copper to expose the resistor element (Figure 3-4).

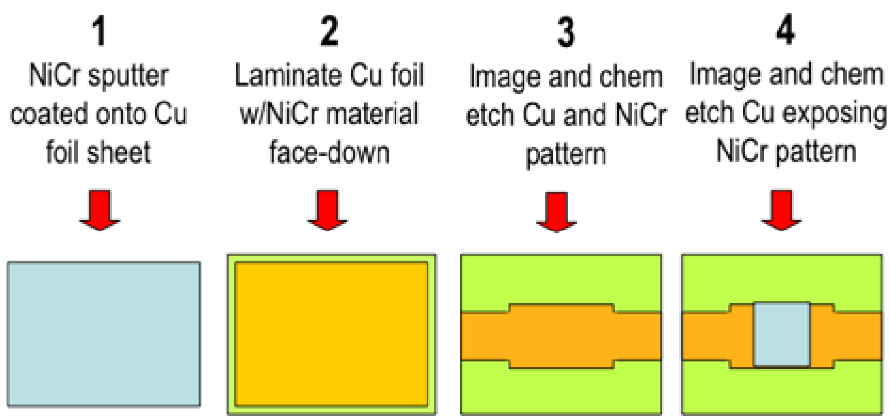


Figure 3- Thin-film resistor process sequence
(Example source: IPC-7092)

When selecting the components for embedding with either thick-film or thin-film process, the designer must first select a base value that can enable the widest number of resistor elements. Thick-film and thin-film materials are available in a number basic resistance values. The paste-like polymer thick film (PTF) material is available in resistance values that range between 1 ohm and 1 meg ohm per square while the ceramic thick film (CTF) materials value will range between 10 ohms and 10K ohms.

Thin-film NiCr or NiCrAlSi material (sputter coated onto Cu foil sheet stock) is furnished in 25, 50, 100 and 250 ohms/square sheet resistivity. Basic sheet resistor tolerance is stated to be +/- 5% but, laser trimming can be used to improve resistor tolerance. Any trimming of the elements, however, must be performed before lamination of additional circuit layers.

Formed Capacitors- Forming a capacitor element within the multilayer circuit structure is somewhat more complex. There are two primary techniques for fabricating embedded capacitors;

1) A planar capacitor is produced when dielectric material is laminated between opposing copper circuit layers. The planar capacitor basically separates parallel copper foils. These foils generally provide the power and ground layers of the substrate.

2) Discrete formed capacitors are made by depositing a pattern of thick-film dielectric material directly onto a copper land pattern using a screen-printing process forms the basic discrete capacitor element. After curing the dielectric material a conductive layer of material is printed or laminated over the dielectric to complete the capacitor function. Both planar and discrete capacitor variations are illustrated in Figure 4.

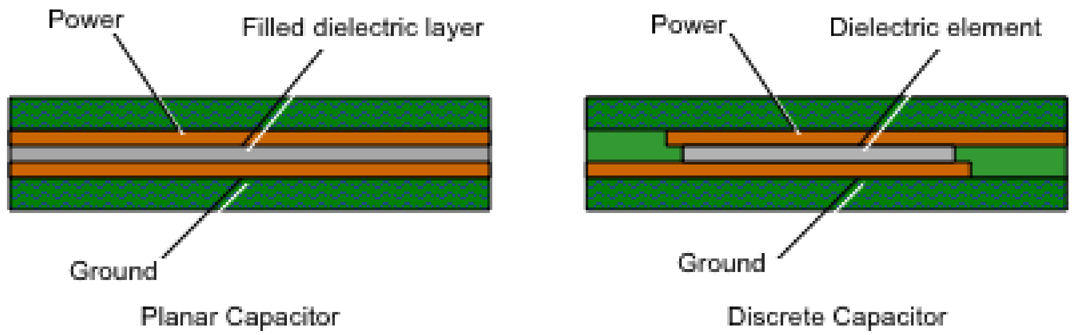


Figure 4- Planar and discrete capacitor elements
(Example source: IPC-7092)

Formed Inductors- Forming discrete inductor elements within the copper foil circuit layers, although limited in value range, is most economical. Unlike formed resistors or capacitors, formed inductors require no special materials or special fabrication processes. Inductors are generally designed to resemble a spiral-like form-factor that is created during the copper etching process (Figure 5). The inductance value is determined by the total conductor length, spacing between conductors and the number of turns in the spiral. The spacing between turns will determine the resonant frequency of the inductor. A wider spacing for example, will typically reduce capacitance and raise the inductance frequency.

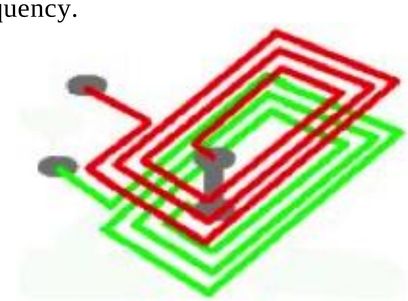


Figure 5- Two level spiral inductor configuration
(Example source: Pulsonix)

Placing Discrete Passive Component Elements

When placing discrete component elements within the printed board structure, both device outline and thickness must be considered. Several companies are now able to furnish very thin, small outline resistors and capacitors that are proving to be ideal for embedded component applications. The outline of the currently available components are as small as 0.4mm x 0.2mm (01005) and 0.6mm x 0.3mm (0201). Discrete thick-film and thin-film resistors are offered in a very thin .015mm profile (Figure 6). Although these devices have a relatively low power rating, the operating temperature range, resistor values and tolerances specified are the same as the larger resistor variations.

Figure 6- Small outline resistors
(Example source: MuRata)

Discrete capacitors are also available with the same outline dimensions as the resistors but due to the dielectric volume, thicknesses can vary somewhat. The body thickness for 01005 capacitors, for example, is specified as 0.20mm while the 0201 outline component thickness can increase to 0.30mm. Additionally, the dielectric type and working voltage will impose limits on capacitor value range for these smaller device outline families. The 01005 and 0201 type capacitors with a C0G dielectric, for example, are available in a value range between 5.0pf and 100pf. While the X7R dielectric capacitors, on the other hand can furnish a value range 68pF to 470pF for the 01005 outline capacitor and 68pF to 10,000pF for the 0201 variation. These value ranges may vary somewhat between suppliers (Figure 7).

Figure 7- Ultrathin, small outline capacitors
(Example source: AVX)

New families of miniature inductors that may be considered for embedding are available from a number of leading suppliers. Components have been developed with a small outline and low profile using thin-film metal patterns on a ceramic base material. These smaller outline inductor elements range in size from 1.6mm x 0.8mm x 1.0mm thick down to 0.61mm x 0.31mm x 0.28mm thick. Manufacturers claim that the miniature inductors furnish up to twice the rated current and half the DC resistance of comparable ferrite inductors. The value range for the small outline discrete inductor elements, however, is somewhat limited.

Placing Active Semiconductor Elements

Technologists have found that embedding the semiconductor on an inner layer directly in- line with a related semiconductor package mounted on the outer surface often enhances product performance because the interface length between die elements can be minimized. There are several methods used for embedding semiconductor elements but the die bond-sites will require some preparation. An active device that is placed within the layers of the primary interconnect substrate must have terminals that have plating that is compatible with the interconnect process selected (wire-bond, flip-chip, micro-via).

Because the bond sites are generally furnished with an aluminum plating for traditional gold wire bond interconnect, a number of secondary plating and coating processes must be performed while the die elements remain in the wafer format. In addition, higher I/O elements may require a redistribution of the edge located bond sites to a uniform array format to enable more efficient circuit board interconnect. The primary alloy selected for bond site preparation and surface redistribution is copper. The copper alloy is more compatible with other plating and contact forming processes. Illustrations furnished in Figure 7 are examples of common contact preparation methodologies employed for terminating uncased die elements.

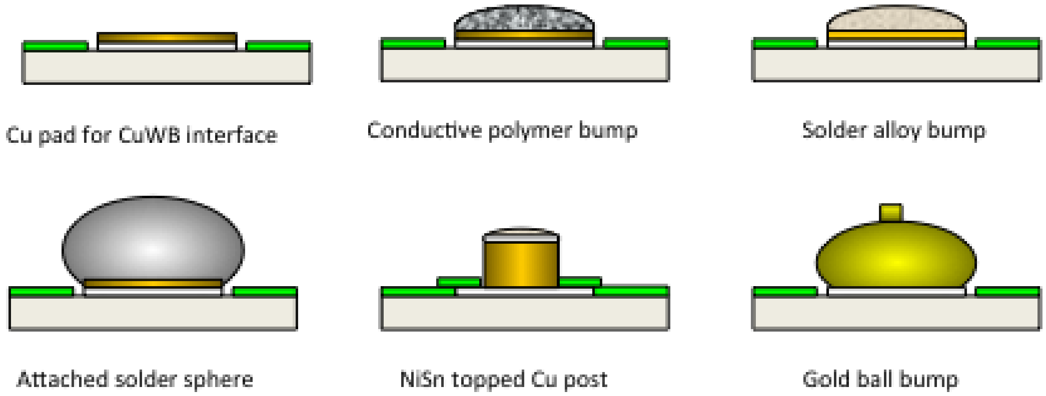


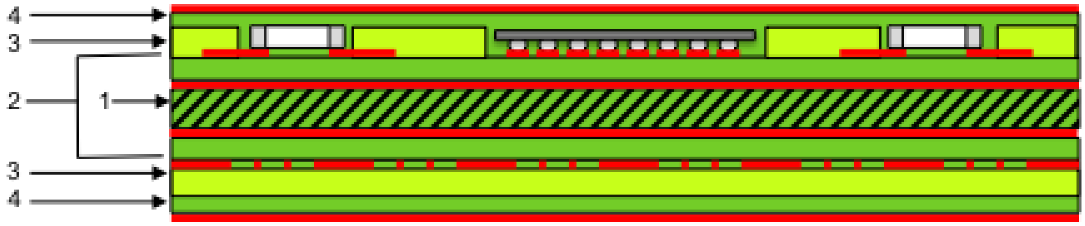
Figure 7- Semiconductor terminal variations for embedding
(Example source: STC)

Embedded Component Circuit Fabrication
Although there are unlimited techniques and process sequences that could be applied to fabricating the embedded component circuit board, technologists working in this area have developed the IPC-7092, Design and Assembly Process Implementation for Embedded Components. This document furnishes a level of guidance to those exploring embedded component technology for their products and describes the design and assembly challenges for embedding passive and active components, formed or placed, into a printed board.

There are six basic embedded component structures described in the document. These structures have been generalized in order to simplify the communication between the designer and the manufacturing facility. The generalization is based on whether the components are passive or active, placed and/or formed and whether they are on one side of the base-core or both. The mounting locations may be on any number of layers, however, the location selected for each component element must be defined (similarly to indicating the conductive layers of a multilayer board). As previously noted, the layering description becomes part of the type designation very similar to describing a 12 layer multilayer board (3-8-3) and the naming indicates whether the base-core represents a final assembly or is simply a base-core onto which additional layers are sequentially added. The IPC-7092 standard defines the following six embedded component structure designs:

- **Type A base-core** configurations consist of either active or passive components, or both, on one side of a mounting base.
- **Type B base-core** configurations consist of either active or passive components, or both, on both sides of a mounting base.
- **Type C base-core** configurations consist of either active or passive components, or both, on one side of a mounting base that contains formed passive components.
- **Type D base-core** configurations consist of either active or passive components, on both sides of a mounting base that contains formed passive components..
- **Type E base-core** configurations consist of a pre-manufactured mounting-base that contains formed passive components unto which additional layers have been added in order to produce an HDI multilayered base-core. The process sequentially adds RCC layers and microvias for interconnection.
- **Type F Embedded Core** process is really considered a 'coreless' assembly variation based on a 'face down' component mounting technology. The 'Type F' structure relies on a combination of HDI micro via technology, a ultra-fine-line, semi-additive plating process and a unique 'component first' assembly technology.

Five of the embedded component structures have multiple base core variations. The Type A base core, for example includes three configurations. The Type A-1 has passive chip components "placed" on one side of the mounting base, Type A-2 illustrates active semiconductor die elements "placed" on one side of the mounting base and Type A-3 includes passive chip and active semiconductor die elements to be "placed" on one side of a mounting base (Figure 8).



1-Copper clad (2 side) core; 2- Component mounting base; 3-Cavity modified prepreg; 4-Copper clad dielectric

Figure 8- A3 Base-core example with placed passive and active components on one side
(Example source: IPC-7092)

Combining both formed and placed components within the circuit board structure is feasible as well. The IPC document describes the Type C3 base-core configuration, for example, as having one or more active semiconductor die components and one or more passive chip components mounted on one side of a pre-manufactured mounting-base that contains formed passive components. The mounting base and its formed passive components is a completely processed base structure made ready for mounting the uncased semiconductor die and passive discrete components.

Face-down component placement- Once the components have been attached to the mounting base a dielectric material is placed over the components. This may be prepreg or a B-stage reinforced dielectric. The surface directly over the bare die and passive chip components, should remain planar prior to the lamination of additional circuit layers. If the component thickness is too great, it may require cavity features in the dielectric material typical of that shown in Figure 9.

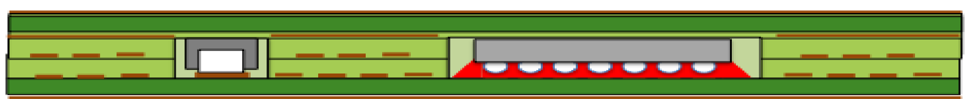


Figure 9- Cavity mounted components

(Example source: IPC-7092)

Face-up component placement- When one or more thinned semiconductor element are to be mounted face-up onto a copper plane it is common practice to ablate cavity features in the dielectric material using a C02 laser before or after the initial lamination process. The example shown in Figure 10-A illustrates two 'face-up' cavity mounted die elements. A common process would employ a thermally conductive adhesive compound for die attach. After curing the adhesive, the partially assembled substrate is transferred to the lamination system to apply the copper-clad dielectric layer. Following lamination, micro-via holes are ablated at each contact site and plate to fill and close the vias to complete the interface between the component 'build-up' circuit layers (Figure 10-B).

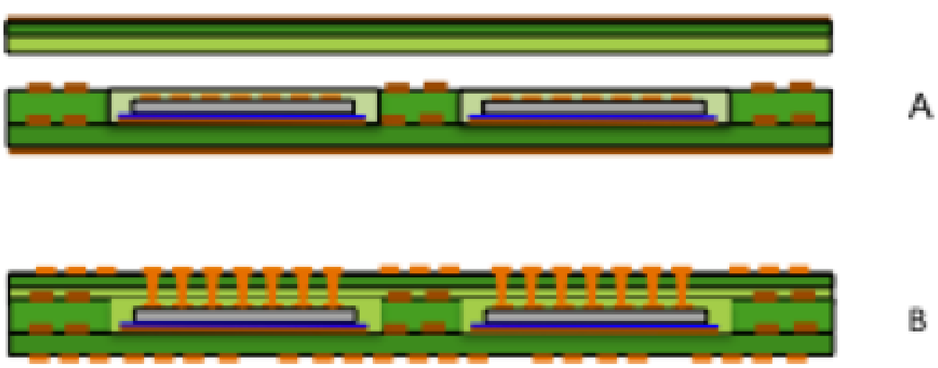


Figure 10- Face-up, in-cavity die attach for micro-via interface
(Example source: IPC-7092)

Following via plating and circuit etching processes, additional circuit layers are typically processed sequentially onto both sides of the base-core. When completed the outside layers commonly include component mounting land patterns furnished with a surface plating that is compatible with traditional SMT assembly processing.

It is recommended that any base-core structures have balance, meaning that the same material set (both dielectric and copper foil) are added to both sides of the mounting-base This laminating operation is often accomplished in one press cycle. An alternate method uses similar dielectric embedding and balance material and electroless copper deposition to image the outside conductive surfaces after the microvias have been ablated. After the base-core is completed further layering can be accomplished by adding copper clad dielectric or resin coated copper layers. As noted, a key issue is balanced construction. The base-core should always be balanced in pairs (2-4-6) so additional build-up layering can be duplicated on both sides of the core.

Embedded Core Fabrication Process

The F1 and F2 embedded core structure was developed through the HERMES, a European industry and academia consortia. The process that evolved in the program is based on a 'face down' uncased semiconductor component technology that employs a combination of HDI fabrication and micro via ablation and plating, ultra-fine line semi-additive pattern plating technology. The assembly methodology adapts both discrete passive and active components that have been configured with copper terminals for embedding. The process described by the developers begins with laser marking fiducial targets on the surface of an ultra-thin copper foil base layer. A pattern of adhesive material that is slightly larger than the component outline is deposited onto the copper surface and partially cured to furnish a stable surface for device attachment. Using the laser formed fiducial target features on the copper surface as a guide, the component(s) are placed into the partially cured adhesive pattern with the terminal features facing down. A thermal curing process follows to complete the bonding of the components to the copper foil base.

The next step is applying a pre-punched or laser ablated FR-4 fine-glass reinforced prepreg material onto the surface of the copper foil followed by a layer of FR-4 prepreg. The pattern in the non-clad material is only slightly larger than the component outline(s). The composite is finally laminated using a conventional multilayer vacuum press and made ready for the next process stage. Following the press lamination process the die element incased in the prepreg material is flipped over for laser ablation of the via sites.. (Figure 11).

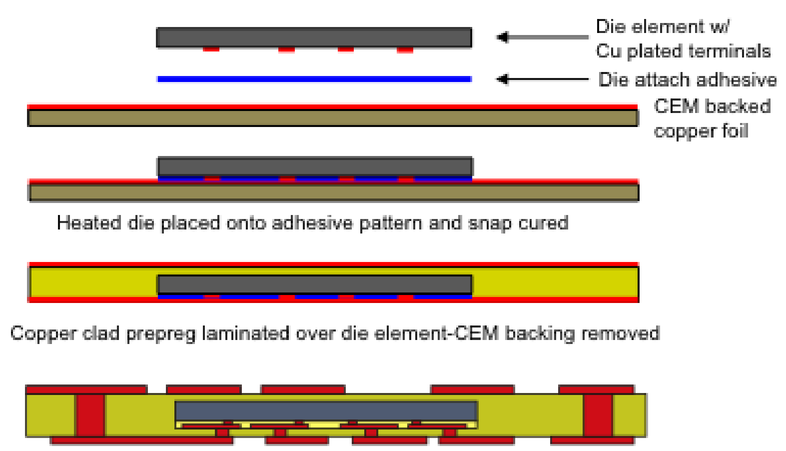


Figure 11- Embedded core fabrication sequence
(Example source: AT&S)

After via hole cleaning the laser ablated holes are filled using a copper plating process. A semi-additive copper plating process is then employed to build-up the circuit pattern on the outer surface of the thin foil base. To accommodate plating, a high-resolution photoresist is laminated onto the copper foil surface followed by imaging of the resist to define the circuit pattern. The resist is finally developed and the exposed Cu circuit patterns are built-up by galvanic plating. After the photo resist is stripped the remaining ultra-thin copper foil that is exposed after the resist stripping is removed by flash etching. The core with the embedded components is then ready to be coated with a solder mask and finished with conventional surface finishes or made ready for laminating additional build-up circuit layers to enable the mounting of additional components on the outer surfaces.

Supply Chain for Embedded Component PCBs

A reliable infrastructure must be in place to accommodate the embedded component PC board manufacturing processes. A growing number of PCB suppliers with experience in build-up circuits are involved in embedding both passive and active components. A majority of these companies currently furnishing embedded component substrates in high volume are located in Europe and Asia but there are number of capable North American suppliers as well. Providing formed resistors and capacitors within the circuit structure is the most economical process with the least level of risk. Although value range and tolerance control are more limited than the placed discrete components, the processes for forming passive components is well within the capability of most printed circuit fabricators. Placing components on the other hand, is likely outside the realm of the average circuit board supply chain. The process for placing discrete components may require specialized assembly systems that are more common to OEMs and assembly service providers that manufacture electronics. In preparation for high volume production, the fabricator will need to establish in-house component placement and attachment capability, establish component sources or develop partners for the procurement of components that have been prepared for embedding (copper terminals). They will also need to determine which systems and methodology will be required for applying attachment and termination materials (conductive polymer or solder), systems that can ensure precise placement of components, systems needed for curing polymers or reflowing solder and any specialized systems required for electrical testing during the progressive stages of the fabrication process.

Electrical testing- Testing the embedded component assemblies with mixed function die remains a serious concern. One key issue is ownership, especially for the embedded 'active die' elements. Due to the number of process steps involved throughout the embedded component fabrication operations, the component parts will be subjected to conditions that may result in physical damage. The fabricator may be capable in testing a conventional multilayer PCB but testing components on board layers at each stage of the lamination process is not familiar ground. So how to test and what to test and what features are needed to enable test are issues that will need to be addressed when transferring the design to the fabricator. The unique semiconductor testing requirements of dissimilar functions can be a roadblock for many users as well. Embedding known good die (KGD) will remove one of the more significant yield concerns from the process but, procuring fully tested semiconductor elements may not be possible from all sources.

Summary and Conclusions

The IPC-7092 standard suggests that the first decision the developer must address is whether or not to consider embedding components. Depending on the application, cost, performance, or some other metric, the cost for adoption will likely influence this decision. Several materials properties must be considered as well; the availability of passive and active components intended for placement, and implementation of new processes. Although cost of materials and additional process steps can be an issue, 'formed' component processes are mature, economical and well within the process capability of most circuit board fabricators. Manufacturers recognize, however, that values and tolerances of the formed components can shift significantly as the board materials age or when the product is exposed to severe assembly or environmental conditions. On the other hand, with the availability of smaller passive device outlines from a wide supply base, many companies, although reluctant to embed active semiconductor components, will see the practical advantage for embedding discrete passive elements. For resistor elements especially, the value range is broad and the tolerance will remain stable.

Embedding the semiconductor is where many companies may find a significant concern. Procurement of semiconductors in a wafer format and outsourcing metallization and thinning of the wafer is not always possible. Additionally, micro-via termination processes used in circuit board manufacturing requires component parts to have copper plated bond sites. The good news is, a growing number of foundries, are already preparing their wafers for the emerging copper wire-bond users. The originating companies may elect to bring together the two primary suppliers; the circuit board fabrication specialist and the assembly service provider with both assembly and test capability. Some PC board fabrication companies may have already established both of these capabilities in-house but others will need to develop partnerships. These partnerships must be willing to adjust their portion of the generated revenue against the overall process yield. That includes the sharing of losses from fabrication process defects and damaged components.

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