As originally published in the IPC APEX EXPO Proceedings.

Embedded Components: A Comparative Analysis of Reliability

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Abstract
In light of new process and product technologies in the field of embedded components, questions arise with respect to advantages and potential disadvantages to standard SMT component placement when considering reliability.
The fact that components are embedded in the substrate opens up new variables in terms of drop test resistance and thermal cycle test.

- One may expect fundamental qualitative differences to galvanized bonds within a laminate framework in comparison to current external solder joint performance.
- One may expect variations in the component thermal integrity of an embedded component within a substrate and that of a soldered component when subjected to TCT test conditions.

This paper aims at analyzing and confirming the reliability performance (in terms of the above identified test criteria) of embedded components compared to that of standard SMT components through usage of embedded and SMT soldered component test vehicles. These analyses make use of the process technologies and methodologies of the currently running EU-funded project "Hermes".

Introduction
The decision to carry out this comparative analysis was instinctive. Given new technologies in embedding components, what advantages/disadvantages would be apparent when compared to the "traditional" method of surface mount technology (SMT)?
Of course to explore all performance indicators (electrical, mechanical, thermal) and all possible interactions between various materials and components would deserve a more intensive research program, such as the current HERMES project (an European Union funded multi-company project), but in this instance the target was to find a more practicable approach to a tangible problem: connective reliability under stress.
Drop test and thermal cycle test (TCT) were chosen as 2 indicative (albeit not exhaustive) reliability test methods. The test vehicle (a more detailed description can be found in the paper) was designed to be as "standard" as possible and the components chosen were selected based on their commonplace application in the SMT world. Furthermore the test board, by including the SMD and embedded components on the same vehicle, was designed to ensure that both sets of components were subjected to the same stress elements during testing.
The hypothesis of the experiment was twofold:

- Drop test – Due to the locative nature of the embedded components, i.e. embedded between layers of pre-preg in the PCB core and therefore closer to the center point of the PCB construct, and the plastic nature of the resin surrounding the component, it was hypothesized that the drop test performance would exceed that of the standard SMT component, which exposed to higher energy potentials on the outer layer.
- TCT – It was hypothesized that the TCT performance of the embedded components (EC) would at least be par to if not exceed that of standard SMT components.

The results, as the paper will demonstrate, essentially cover the original hypotheses and therefore may serve as a basis of understanding the EC concept and some possible applications. Furthermore, the results may be seen as a basis for additional and more complex investigation (comparative or singular).
In terms of orientation, the paper is divided into three basic sections: Test Preparation, Reliability Testing and Evaluation.

Test Vehicle
As there is currently no standard test vehicle for testing reliability of embedded components, an attempt was made to base the vehicle as much as possible on the standard JEDEC drop test vehicle design (figure 1).

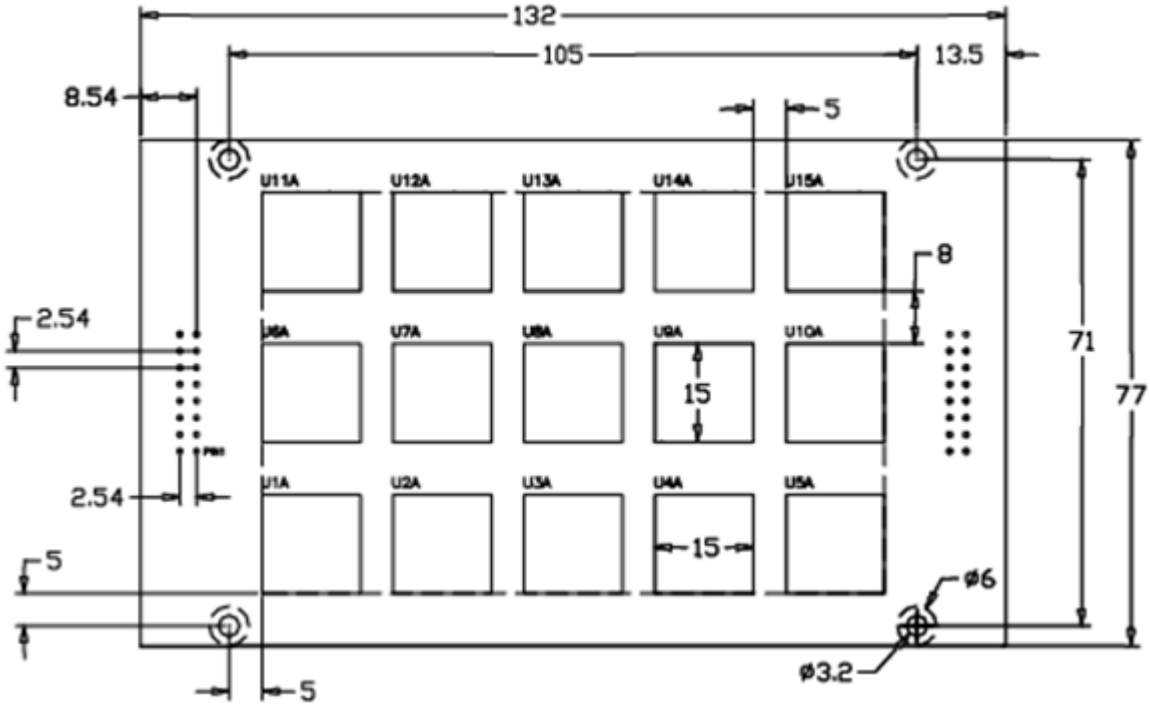


Figure 1 – JEDEC Standard no. 22-B111 Chapter 5.2.1 "Preferred board construction, material and design"

The embedded components test board (we will refer to as REL2000ec) retains the same outer dimensions (132mm x 77mm) and thickness (1mm) as the standard JEDEC vehicle. There were changes made to accommodate for some of the features of our test. This includes changing the standard BGA test pattern to a two-terminal contact pad configuration to account for the mounting of 0402 resistors instead of BGA components. The circuit patterns were configured to supply a daisy-chain test pattern in order to offer better event traceability during and after testing (figure 2). This pattern is essentially mirrored on the inner layer embedded pattern, but with the one distinction the daisy chain 9 and 11 on outer layer and daisy chain 4 and 6 on the embedded layer were not superimposed over each other in order to assess any possible performance influence between components stacked over one another (figure 3). The 16 PTH test terminals at each end of the board were left in the design, but not all were utilized as illustrated in figure 3.

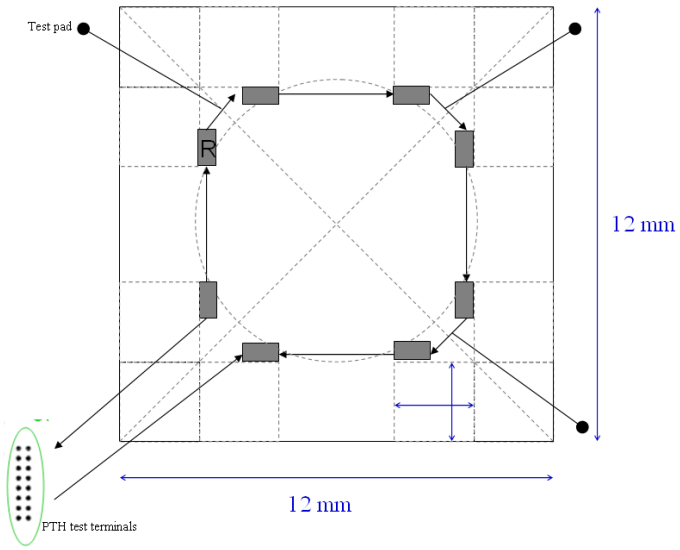


Figure 2 – Daisy chain test pattern on REL2000ec

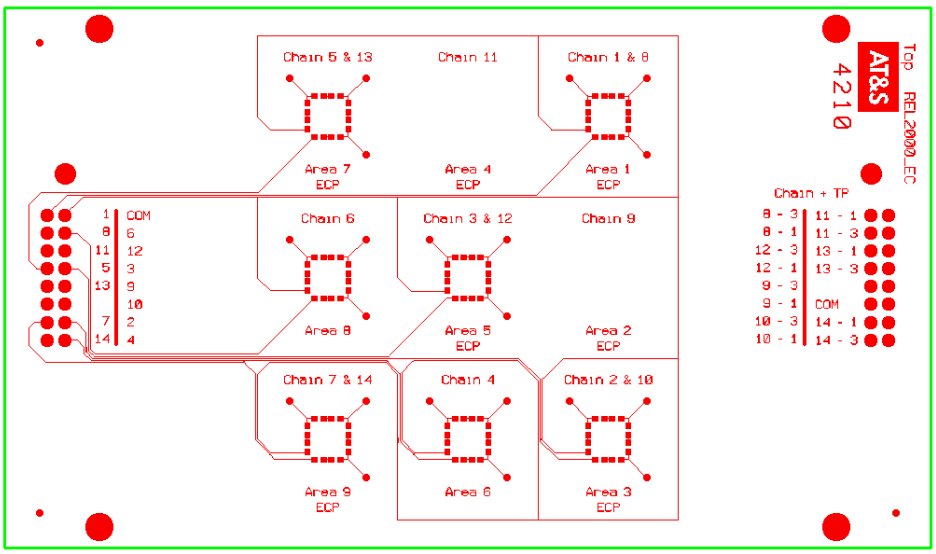


Figure 3 – Outer layer circuit pattern of REL2000ec

The build for the PCB was an 8 layer multi-layer (figure 4). The unused copper on all inner layer was "hatched", which means they were not full copper surfaces. This is standard practice in PCB design to achieve stable thermal and therefore thermo-mechanical performance (i.e. warpage control). The material chosen for the PCB was Panasonic R1551W (halogen free epoxy resin based prepreg). This material reflects a standard material in HDI application and is by no means a material with specialized characteristics for embedding components.

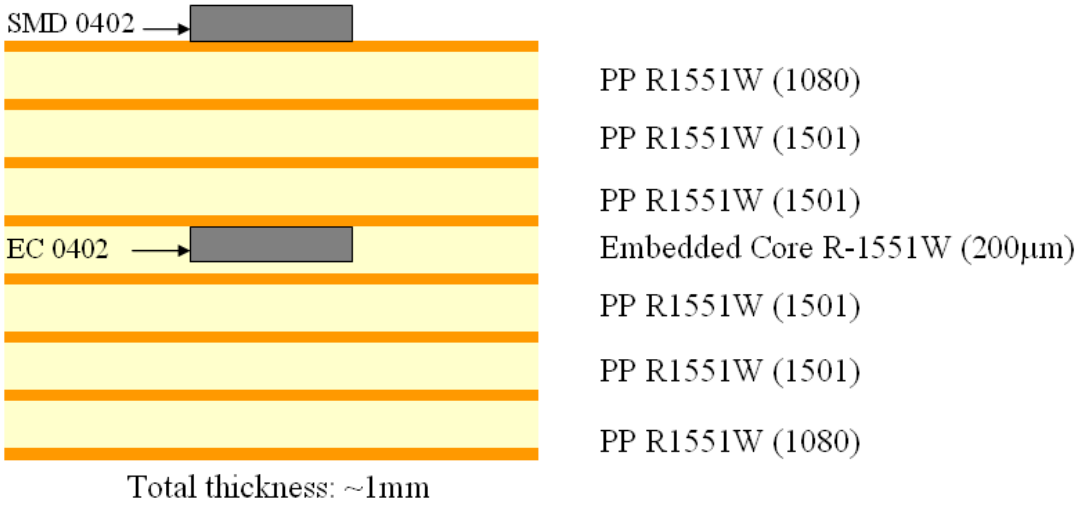


Figure 4 – Build of REL2000ec

Components

In general, it was decided to create this vehicle using passive components (resistors in this case) due to the simplicity of testing without excessive manufacturing performance variability. In other words, active components carry additional testing and performance aspects which require a more devoted research scope and a broader array of test types and participants. Such research is certainly ongoing elsewhere (e.g. with the EU-funded HERMES project, as mentioned above), but the target of this experiment was to set up a practical illustration using as many standards (tests, material, design, etc) as possible.

Standard 10 Ohm 0402 resistor SMD components were chosen for outer layer assembly based on their commonality in both SMT manufacturing and the current embedded component manufacturing at the facility where the test vehicle was produced. The choice should represent a practical application, but is certainly not the only choice which could have been made.

The embedded components are 0402's in terms of the x and y axis (figure 5) and the electrical function matches that of the SMD component. The Z-axis differs in that it is thinner than the standard SMD 0402 (figure 6). The same component manufacturer was used for both SMD and embedded components.

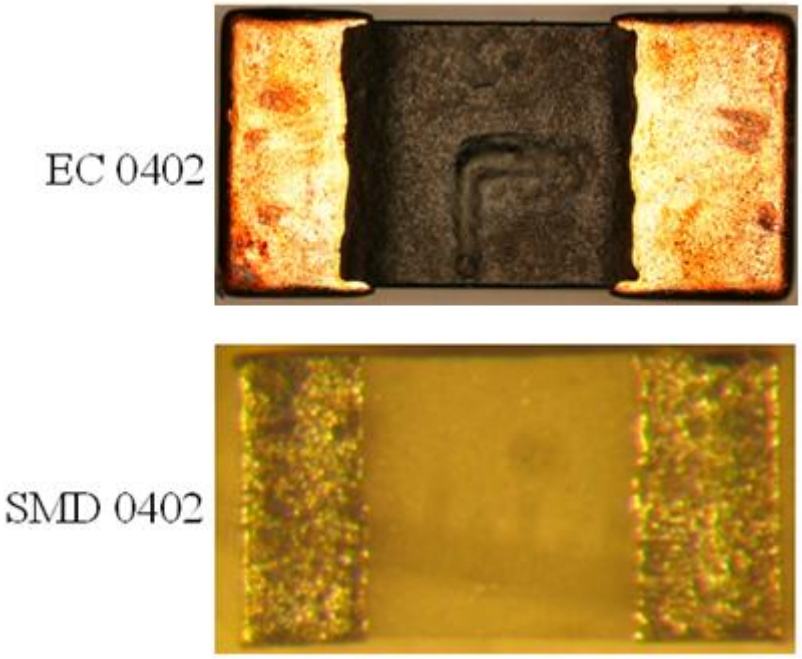


Figure 5 – EC and SMD 0402s have same x and y axis dimensions

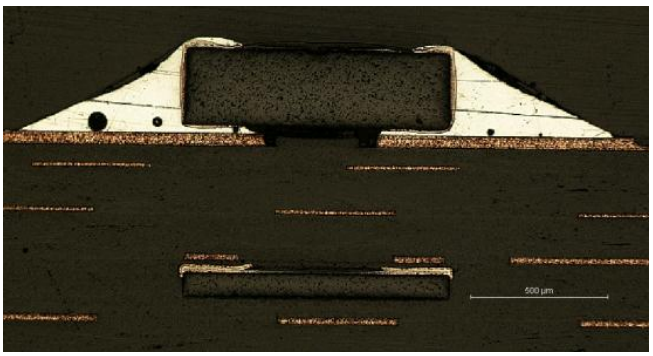


Figure 6 - EC and SMD 0402s vary in z-axis dimension

Due to the nature of the varying methods of achieving connectivity, the terminals of the components also vary. The SMD component is metal grazed (tinned terminals) for the SMT assembly process, whereas the EC has copper terminals. The background and application of the copper terminals will be evident in the "Production" section of this paper.

Production

Production of the test vehicle used in this experiment was carried out in Austria, using the AT&S facility for embedded PCB manufacturing and Flextronics for SMT assembly.

The 10 Ohm EC resistors were assembled at the core layer of the build and are essentially encased in prepreg.

The core copper layers were subsequently processed with photo dry-film and DES (Develop Etch Strip) to reveal the final core layer circuit patterns.

Connectivity to the copper plane and therefore the test circuitry to the PTH test terminals was achieved by forming laser vias (µ-vias) from the copper cladding of the core to the copper terminal of the embedded component and copper plating the µ-via subsequently (see figure 7). The diameter of the vias is **80µm.**

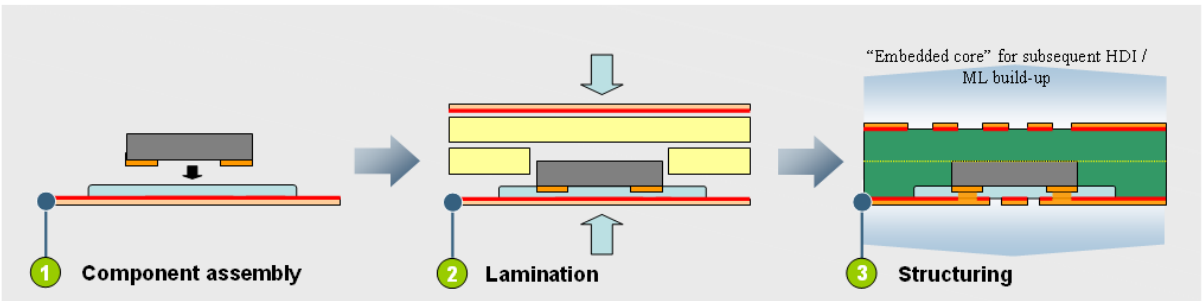


Figure 7 – Basic assembly method of the embedded core

This laminated “embedded core” underwent 3 further standard pressing cycles to achieve the final 8 layer construct.

Reliability Testing

One of the more obvious characteristics of embedded components (pertaining to the manufacturing method discussed here) is the fact that they are encased within the PCB, therefore surrounded by the resin and glass fiber of the prepreg. Any stress from an external would theoretically be distributed within the whole construct and less on the component itself, as opposed to an SMD component and solder joint system, which being on the outer layer is directly exposed a stress source. The central location of the embedded components is also more neutral when considering mechanical stresses to the planar rigidity of the PCB. Furthermore, the mode of connectivity present in the applied manufacturing method (see Production) would theoretically be less stratified in metallurgical terms (compared to a component/solder alloy/copper pad system as present in SMT).

Drop test and TCT were chosen as possible verifying reliability test methodologies of this hypothesis due to their common usage within the PCB manufacturing and OEM industries. In this section we will handle each test separately and supply the results accordingly. The evaluation of the results shall follow in the “Evaluation” section of the paper.

Drop Test

The drop test specification was based on the JEDEC JESD22-B111 (see table 1). The test vehicle REL2000ec was soldered at the test terminal PTHs as demonstrated in figure 8 below. Test events were monitored online as opposed to post hoc testing and verification.

Table 1 – Drop Test Specifications

DT Device	Teknopaja
AT&S Spec	TI GR PH-LAB-33EG
International Spec	JEDEC JESD22-B111
Acceleration:	1500g ± 10%
Pulse Duration:	0,5ms ± 10% (peak width at 10% of maximum pulse height)
Cpk:	> 1,3
Measurement Current:	1,0 mA
Voltage:	1,0 V
Resistance:	1000 Ohm
Tested Structures:	SMD and EC – daisy chains (assembled cards)
Pass/ Fail – Criteria:	Minimum acceptance criterion for components is 10 drops of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.

Figure 8 – Drop Test Device and Test Terminal Set-up

The test vehicle was not prepared in any other relevant manner beyond the soldering of the test terminals to the event recording wire bundle. 18 cards were tested according to the above mentioned test specifications (table 1). The cards were dropped until a resistance value of >1000 Ohm was registered (an "event"). Thereafter, approximately five additional drops were carried out to verify the >1000 Ohm resistance change. Once verified, the location of the exact component (SMD or EC) was determined using the terminal PTHs and the test pads. Once the component has been identified, a cross section analysis was carried out to determine the failure mode.

Drop Test Results

The results of the drop testing yielded the following results, which are also depicted in table 2. 17 out of 18 test vehicles revealed SMD related defects before 1000 drops, while one test vehicle demonstrated 1000 successful drops without SMD failure. There was one out of 18 vehicles which registered an EC related failure before 1000 drops.

The earliest drop failure for SMD was recorded at 304 drops. The highest recorded drop count failure for SMD was 974. The earliest drop failure and thereby only failure for ECs was recorded at 832 drops. Table 2 provides an overview of the drop test results. Figure 9 displays the positions of the component daisy chains and highlights the failure frequency for each chain: red depicts most frequent, orange second most frequent. Each chain was manufactured with either SMDs directly over ECs, only SMDs or only ECs (figure 9).

Table 2 – Drop Test Failure Occurrence Overview: SMD vs. EC (green signifies earliest failure per technology)

		SMD							ECT						
Card	**First Failure**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
3		974			562										
5					734										
7			971		372										
8					678										
9				707	344										
10					512										
11				912	508										
12					908										
13					534										
15					707										
16	**ECT - 832**				684										832
17				906	491			929							
18					547										
19					451										
20															
21					610										
22					519										
23	**SMD - 304**				304										

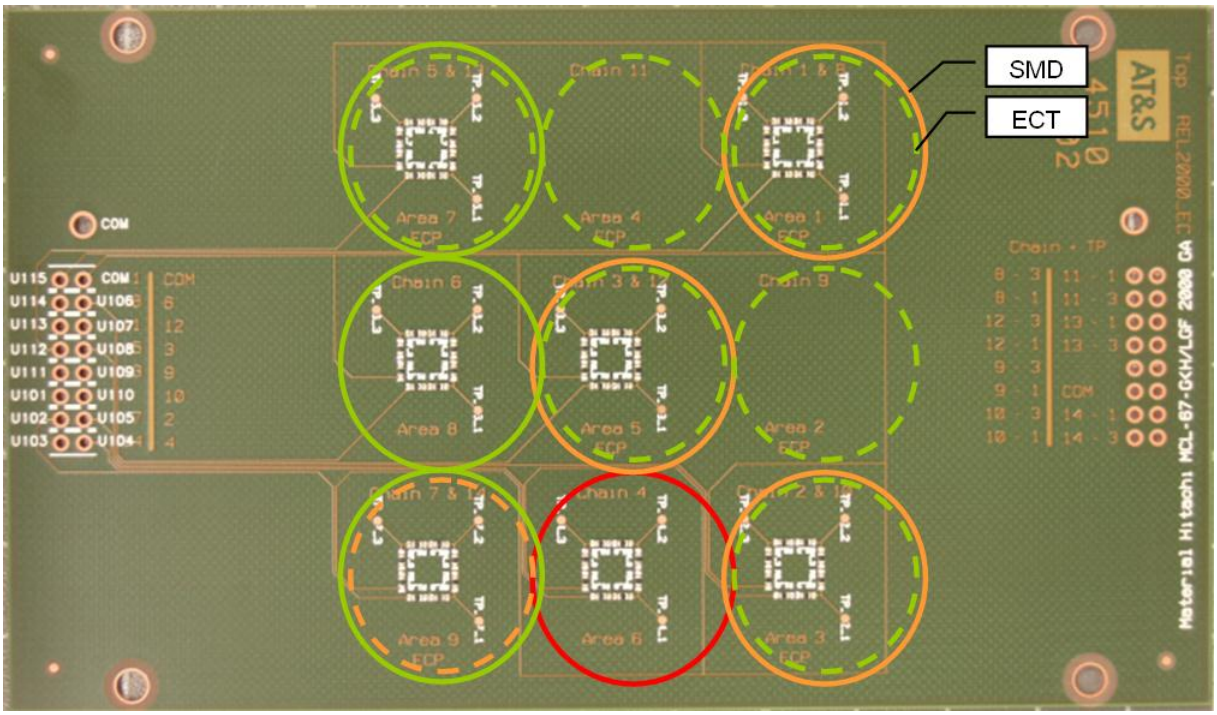


Figure 9 – Overview of component positions: Solid circle indicates SMD in that daisy chain, broken circle indicates an EC daisy chain inside the PCB.

One can see a prevalence of failure in SMD chain 4 (marked in red in figure 9). A possible mechanism behind this failure frequency will be discussed in the "Evaluation" section of this paper.

Drop Test Failure Modes

As discussed above, the SMT variant demonstrated a comparatively low drop test performance vs. the ECs. There were 2 basic failure modes for the SMT failures: trace breakage and component crack.

The trace breakage occurred most frequently and was consistently located on the trace between two SMD components (figure 10).

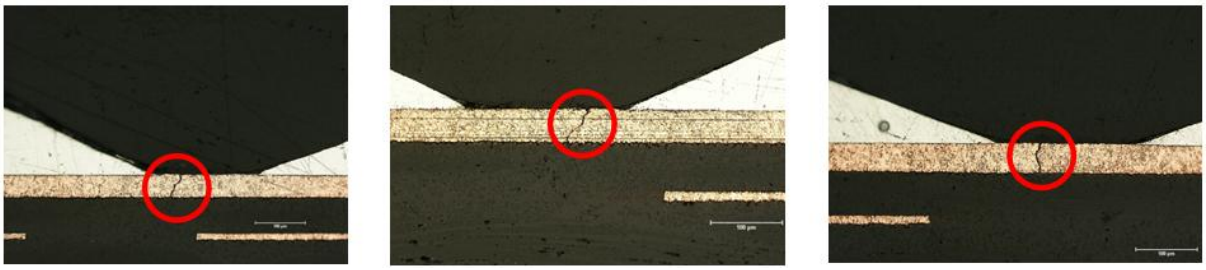


Figure 10 – Examples of drop test failure mode "trace breakage" between SMDs

The second failure mode for SMD was component crack. This occurred in two components and resulted in a complete crack through the component itself (figure 11).

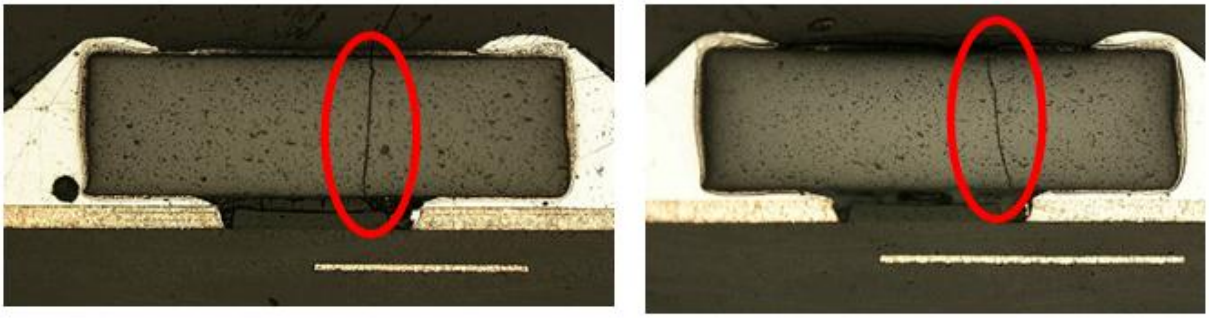


Figure 11 – Drop test failure mode "component crack"

As mentioned above, there was a single failure occurrence from the embedded components. The event was registered from daisy chain 8 (inner layer ECs) at 832 drops. A further 5 drops were carried out thereafter to confirm. Extensive

cross sections were made on all components within this particular daisy chain to find the failure mode, but no obvious evidence could be found in either component (i.e. cracks) or µ-via interconnect (figure 12).

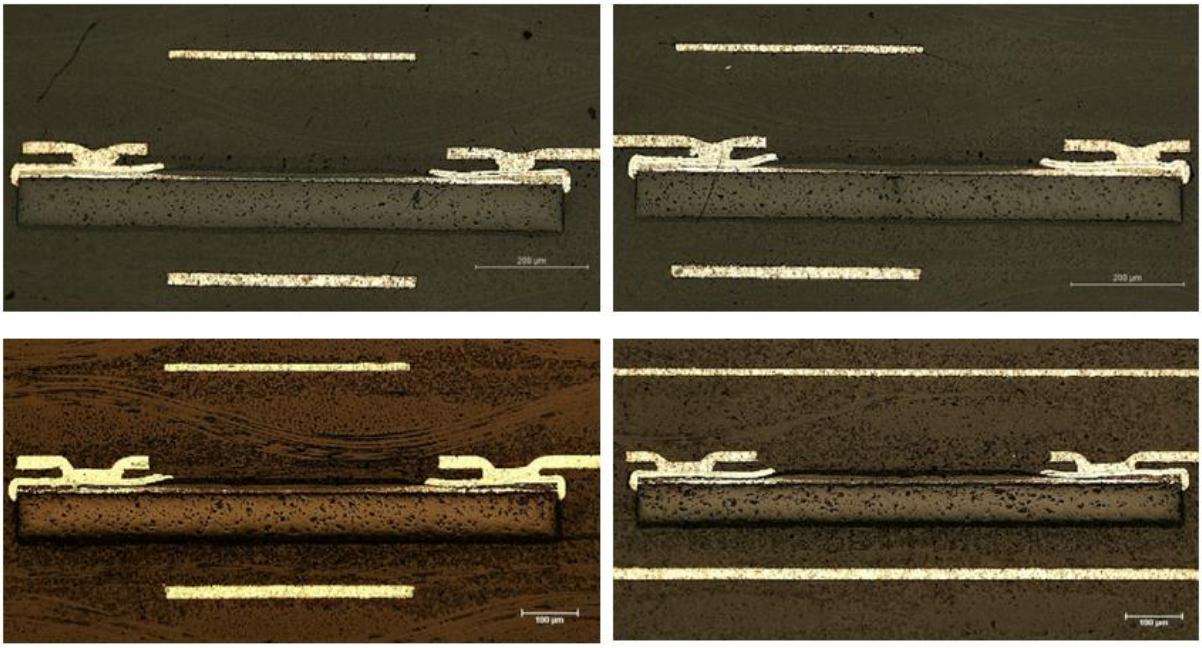


Figure 12 – Examples of cross sections made from registered EC failure at 832 drops: no defect evident at component or interconnect

Further attempts were made to locate the failure source within the PTH and inner layer traces, but no obvious source could be found.

TCT (Thermal Cycle Test)

The TCT specification was based on the JEDEC JESD22-B111 (see table 3). The test vehicle REL2000ec was soldered at the test terminal PTHs. Test events were monitored online as opposed to post hoc testing and verification (figure 13).

Table 3 – TCT specifications

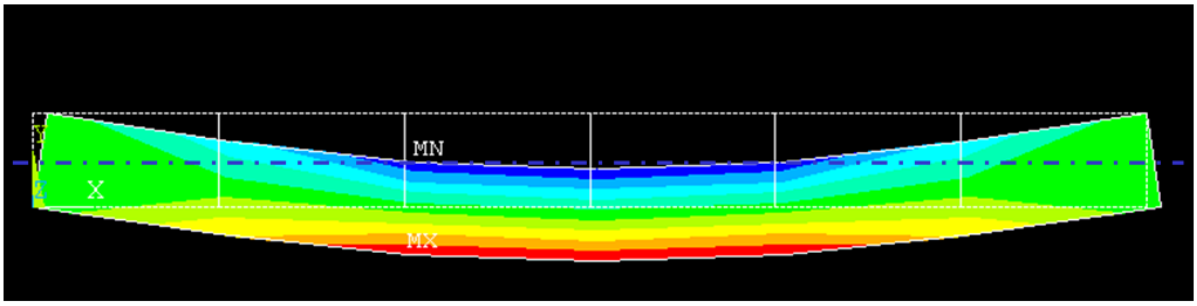
<table>
<tr><td>TCT Device</td><td>CTS CS-70/500-17</td></tr>
<tr><td>AT&S Spec</td><td>TI GR.PH-LAB-51EG</td></tr>
<tr><td>International Spec</td><td>JEDEC JESD 22-A104C, Test Condition G,2,C</td></tr>
<tr><td>Chamber:</td><td>one chamber design</td></tr>
<tr><td>Chamber parameter :</td><td>
<table>
<tr><th>Step per cycle</th><th>Chamber</th><th>Sample Temperature</th><th>Min. Soak Time</th><th>Cycle count[3]</th></tr>
<tr><td>1</td><td>Cold</td><td>-40 +0/-10°C</td><td>5min</td><td rowspan="4">1000</td></tr>
<tr><td>2</td><td>Heat-up</td><td>-</td><td>-</td></tr>
<tr><td>3</td><td>Hot</td><td>+125 +15/-0°C</td><td>5min</td></tr>
<tr><td>4</td><td>Cool-down</td><td>-</td><td>-</td></tr>
</table>
The heating and cooling rate has to be set in such a way that in total 2 cycles per hour are achieved.
</td></tr>
<tr><td>Measurement System:</td><td>Event Detection</td></tr>
<tr><td>Resistance limit:</td><td>1000 Ohm</td></tr>
<tr><td>Tested Structures:</td><td>SMD and EC – daisy chains (assembled cards)</td></tr>
<tr><td>Pass/ Fail – Criteria:</td><td>Assembled cards: Minimum acceptance criterion for components is 500 cycles of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.</td></tr>
</table>

Figure 13 – Online test event registration

5 REL2000ec test vehicles were tested, each with 7 SMD daisy chains and 7 EC daisy chains (14 chains per card in total). Total sum of tested daisy chains was 70: 35 SMD and 35 EC. In each daisy chain there were 8 components.
The boards were subjected to a constant change in temperature in the range of -40°C ↔ +125°C in a one chamber test device. The amount of cycle deemed as target was 1000 cycles.
An event is registered as a failure after demonstrating a resistance change of >1000 Ohm. In all constellations (SMD and EC) the test vehicle passed 1000 cycles without failure. No further cross sections or analyses were made due to the lack of any relevant failure.

Evaluation
Many efforts were made in this experiment to base the board design, test methods and components on existing standards to achieve increased objectivity and comparability. Considering the aim of identifying general performance variations in reliability between the traditional SMT and embedded components (manufactured in such a form as described here), the test vehicle design and test methodology proved effective. Certainly improvements to board and test design must and will be considered in further steps.

The drop test results were the least surprising considering the mechanics of the test itself and the location of the embedded component within the PCB itself. In PCB level drop testing there is no impact on a hard surface (as with some device level drop testing), rather the board is suspended on the four corners and accelerated towards a halting point. This being considered it is clear why the daisy chain number 4 (signified by the red circle in figure x) could have demonstrated the lowest performance. When the board reaches the nadir of its fall in the test device, the four suspended corners remain fixed and the board center exhibits a downward expansion. The position of chain 4 is at the most extreme curvature of this tension. In other words, the outermost point during the drop (where chain 4 is found) is farthest from the neutral axis, whereas the ECs remain closer to this axis (figure 14).The result for SMD is, given good solder joints and copper adhesion, a trace breakage between solder joints.



Neutral Axis

MN – Minimum tension

MX – Maximum tension

Figure 14 – Model of tension distribution at drop test nadir. Embedded components would be found in the area indicated with green.

The component breakage noted in the drop test results section of this paper are also likely a product of similar stresses. A drop test with actual surface impact, of course, may reveal varying results in regards to component breakage, but it remains clear that the components deviation to the neutral axis in not advantageous when the rigid PCB is subjected to planar modifications.

The root cause for the single failure at 832 drops with one embedded component has yet to be determined. There was no obvious evidence of any physical component nor was there any interconnect damage to be found within the scope of the analysis. Had there been an increased failure level, certain commonalities could have perhaps been drawn. However, a single failure as such is by nature hard to configure into any fundamental thesis or probability model (Weibull, for example).

Thus the embedded components in this experiment provided clear superiority in terms of reliability under board level drop testing conditions. It could be extrapolated that the usage of such components may provide certain advantages to SMDs given a PCBAs or device's exposure to similar environments as those simulated in the drop test.

Regarding the results of the TCT testing, it is difficult to reach a final statement other than the fact that both the SMDs and the ECs provided comparable results and can therefore be deemed both suitable to environments which are meant to be simulated with the TCT test methodology. This statement may be further drawn out to conclude the compatibility of both components towards one another in the same PCB construct; i.e. ECs do not appear to be detrimental to the success of SMDs during testing and vice versa.

As the TCT test is mainly used to test reliability during thermal fluctuation (automotive, aerospace, industry, etc.), the CTE match of material and components is certainly a criterion for successful withstanding of the test. The larger the component is and the larger the number of interconnects between component and PCB, the more influence the CTE of the individual constituents will take. As the 0402 components are relatively small and have only two interconnect terminals (compared to the BGAs on a standard JEDEC test board), one may expect less component relevant failure in general.

To summarize, there were visible reliability advantages for embedded components under the production and testing methods described. These advantages, at least with these components and array, are mainly found in reduction of deviation to a rigid board's neutral axis. In terms of thermal reliability there were no disadvantages for ECs seen in these tests.